



Serial Input PLL with 2.0-GHz Prescaler

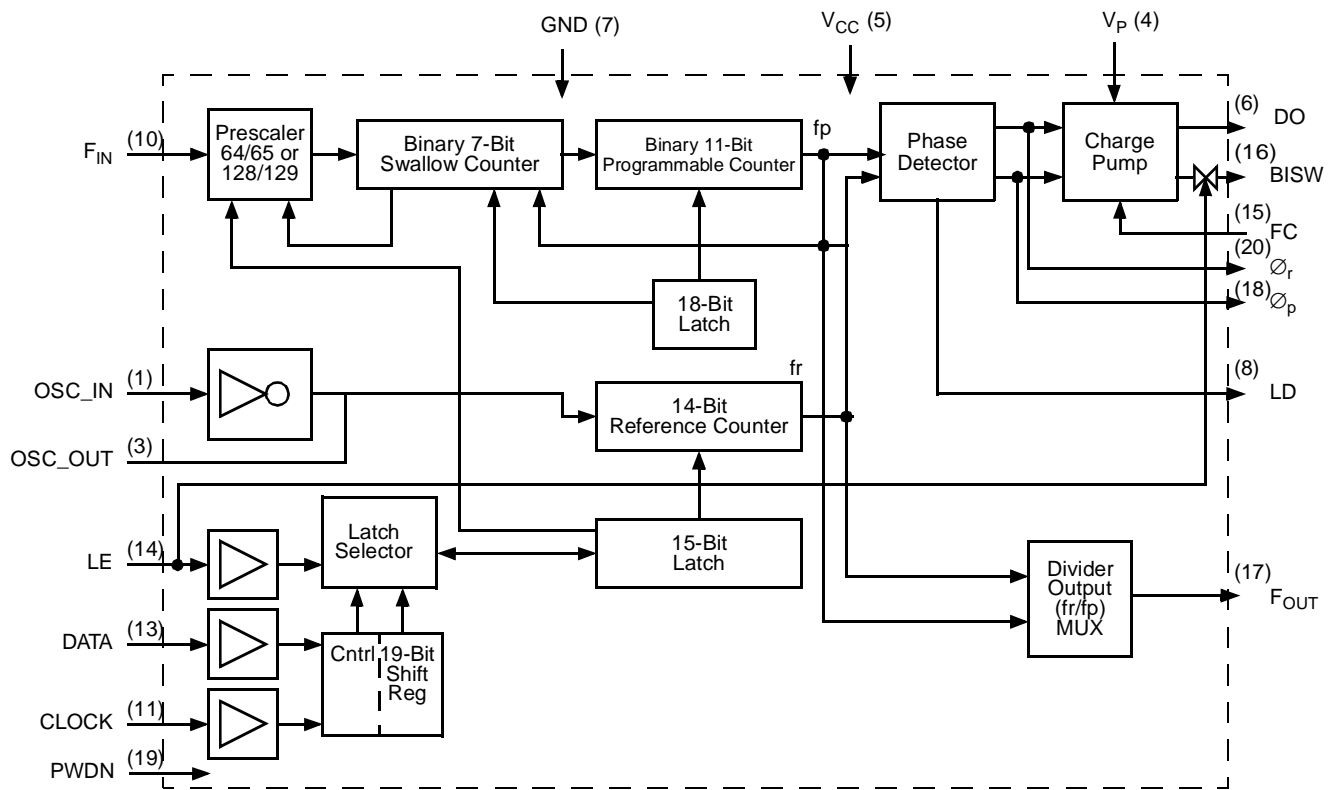
Features

- Operating voltage 2.7V to 5.5V
- Operating frequency: up to 2.0 GHz with prescaler ratios of 64/65 and 128/129
- Lock detect feature
- Power-down mode
- 20-pin TSSOP (Thin Shrink Small Outline Package)

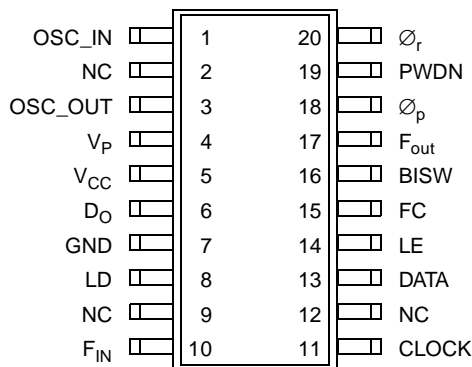
Applications

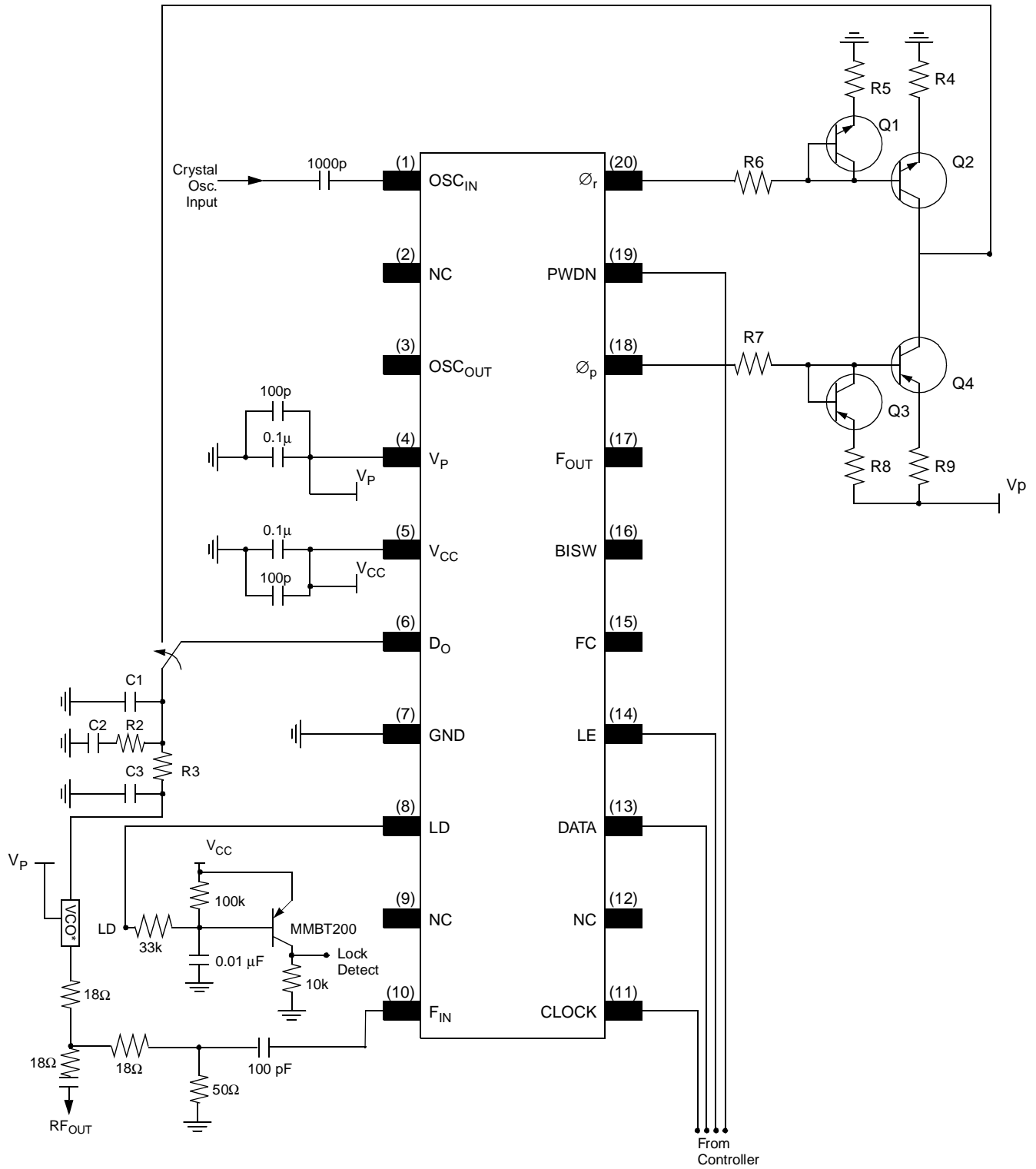
- Wireless LAN
- Wireless communication handsets
- Base Stations
- Microcells

CYW2320 PLL Block Diagram



Pin Configuration





**Figure 1. Application Diagram Example - CYW2320 2.0-GHz PLL**

**Pin Definitions**

Pin Name	Pin No.	Pin Type	Pin Description
OSC_IN	1	I	<b>Oscillator Input:</b> This input has a $V_{CC}/2$ threshold and CMOS logic level sensitivity.
NC	2		<b>No Connect</b>
OSC_OUT	3	O	<b>Oscillator Output</b>
$V_P$	4	P	<b>Charge Pump Rail Voltage:</b> This supply for charge pump. Must be $> V_{CC}$ .
$V_{CC}$	5	P	<b>Power Supply Connection for PLL:</b> When power is removed from $V_{CC}$ all latched data is lost.
$D_O$	6	O	<b>Charge Pump Output:</b> The phase detector gain is $I_P/2\pi$ . Sense polarity can be reversed by setting FC LOW (pin 15).
GND	7	G	<b>Analog and Digital Ground Connection:</b> This pin must be grounded.
LD	8	O	<b>Lock Detect Pin:</b> This output is HIGH with narrow LOW pulses when the loop is locked.
NC	9		<b>No Connect</b>
$F_{IN}$	10	I	<b>Input to Prescaler:</b> Maximum frequency 2.0 GHz.
CLOCK	11	I	<b>Data Clock Input:</b> One bit of data is loaded into the Shift Register on the rising edge of this signal.
NC	12		<b>No Connect</b>
DATA	13	I	<b>Serial Data Input</b>
LE	14	I	<b>Load Enable:</b> On the rising edge of this signal, the data stored in the Shift Register is latched into the counters and configuration controls.
$F_C$	15	I	<b>Phase Sense Control for Phase Detector with Internal Pull-up:</b> When pulled LOW, the polarity of the Phase Detector is reversed.
BISW	16	O	<b>Analog Switch Output:</b> Connects to output of charge pump when LE is HIGH.
$F_{OUT}$	17	O	<b>Monitor Point for Phase Detector Input</b>
$\emptyset_P$	18	O	<b>External Charge Pump Output:</b> Open drain N-Channel FET, pull-up resistor required.
PWDN	19	I	<b>Power Down Pin with Internal Pull-up:</b> When pin is HIGH, device is in normal state. When pin is LOW, device is in power-down mode. When device enters power-down mode the charge pump is in the three-state condition.
$\emptyset_R$	20	O	<b>External Charge Pump:</b> (CMOS logic output).

### Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating

only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
$V_{CC}$ or $V_P$	Power Supply Voltage	-0.5 to +6.5	V
$V_{OUT}$	Output Voltage	-0.5 to $V_{CC}+0.5$	V
$I_{OUT}$	Output Current	$\pm 15$	mA
$T_L$	Lead Temperature	+260	°C
$T_{STG}$	Storage Temperature	-55 to +150	°C

### Handling Precautions

Devices should be transported and stored in antistatic containers.

These devices are static sensitive. Ensure that equipment and personnel contacting the devices are properly grounded.

Cover workbenches with grounded conductive mats.

Always turn off power before adding or removing devices from system.

Protect leads with a conductive sheet when handling or transporting PC boards with devices.

If devices are removed from the moisture protective bags for more than 36 hours, they should be baked at 85°C in a moisture free environment for 24 hours prior to assembly in less than 24 hours.

### Recommended Operating Conditions

Parameter	Description	Test Condition	Rating	Unit
$V_{CC}$	Power Supply Voltage		2.7 to 5.5	V
$V_P$	Charge Pump Voltage		$V_{CC}$ to +5.5	V
$T_A$	Operating Temperature	Ambient air at 0 CFM flow	-40 to +85	°C

**Electrical Characteristics:**  $V_{CC} = 3.0V$ ,  $V_P = 3.0V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , Unless otherwise specified

Parameter	Description	Test Condition	Pin	Min.	Typ.	Max.	Unit
$I_{CC}$	Power Supply Current		$V_{CC}$		7		mA
$I_{PD}$	Power-down Current	Power-down, $V_{CC} = 3.0V$	$V_{CC}$		6	100	$\mu A$
$F_{IN}$	Maximum Operating Frequency		$F_{IN}$	2.0			GHz
$F_{OSC}$	Oscillator Input Frequency	No load on OSC_OUT	OSC_IN			60	MHz
						25	MHz
$PF_{IN}$	Input Sensitivity	$V_{CC} = 2.7V$	$F_{IN}$	-15		4	dBm
		$V_{CC} = 5.5V$		-10		4	dBm
$V_{OSC}$	Oscillator Input Sensitivity		OSC_IN	0.5			$V_{P-P}$
$I_{IH}, I_{IL}$	Oscillator Input Current			-100		100	$\mu A$
$V_{IH}$	High Level Input Voltage	$V_{CC} = 5.0V$	DATA, CLOCK, LE	$V_{CC} * 0.8$			V
$V_{IL}$	Low Level Input Voltage					$V_{CC} * 0.3$	V
$I_{IH}$	High Level Input Current			-10	1	10	$\mu A$
$I_{IL}$	Low Level Input Current			-10	1	10	$\mu A$
$V_{OH}$	High Level Output Voltage		$F_O/LD$	2.2			V
$V_{OL}$	Low Level Output Voltage					0.4	V
$ID_{O(SO)}$	$ID_O$ , Source Current	$V_P = 3.0V, VD_O = V_P/2$	$D_O$		-3.2		mA
		$V_P = 5.0V, VD_O = V_P/2$			-3.8		mA
$ID_{OH(SI)}$	$ID_O$ High, Sink Current	$V_P = 3.0V, VD_O = V_P/2$	$D_O$		3.2		mA
		$V_P = 5.0V, VD_O = V_P/2$			3.8		mA
$\Delta ID_O$	$ID_O$ Charge Pump Sink and Source Mismatch	$VD_O = V_P/2$ $[ ID_{O(SI)}  -  ID_{O(SO)} ] / [1/2 * ( ID_{O(SI)}  +  ID_{O(SO)} )] * 100\%$			5		%
$ID_O$ vs T	Charge Pump Current Variation vs. Temperature	$-40^{\circ}C < T < 85^{\circ}C, VD_O = V_P/2^{[1]}$			5		%
$ID_{O-tri}$	Charge Pump High-Impedance Leakage Current				$\pm 2.5$		nA

**Note:**

- $ID_O$  vs T; Charge pump current variation vs. temperature.  
 $[|ID_{O(SI)}|_{T^1} - |ID_{O(SI)}|_{25^{\circ}C}] / |ID_{O(SI)}|_{25^{\circ}C} * 100\%$  and  
 $[|ID_{O(SO)}|_{T^1} - |ID_{O(SO)}|_{25^{\circ}C}] / |ID_{O(SO)}|_{25^{\circ}C} * 100\%$ .

## Timing Waveforms

### Phase Characteristics

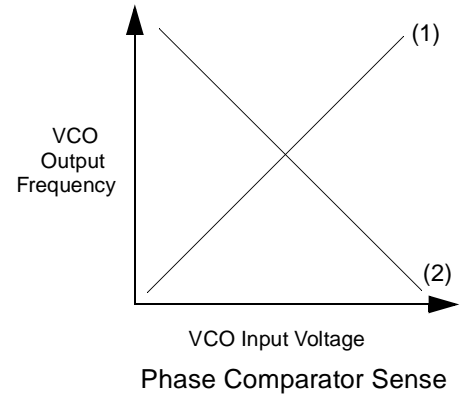
For normal operation, the FC pin is used to select the output polarity of the phase detector. Both the internal and any external charge pump are affected.

Depending upon VCO characteristics, FC pin should be set accordingly:

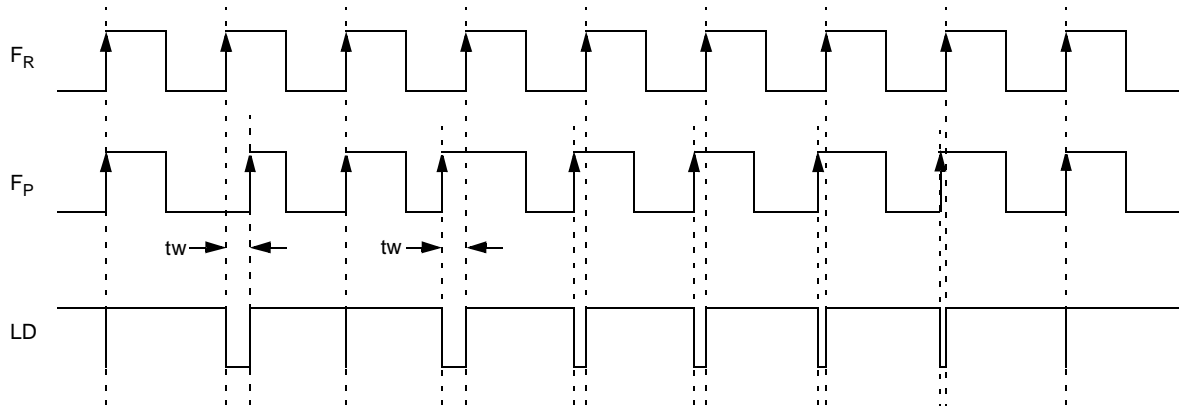
When VCO characteristics are like (1), FC should be set HIGH or OPEN CIRCUIT:

When VCO characteristics are like (2), FC should be set LOW.

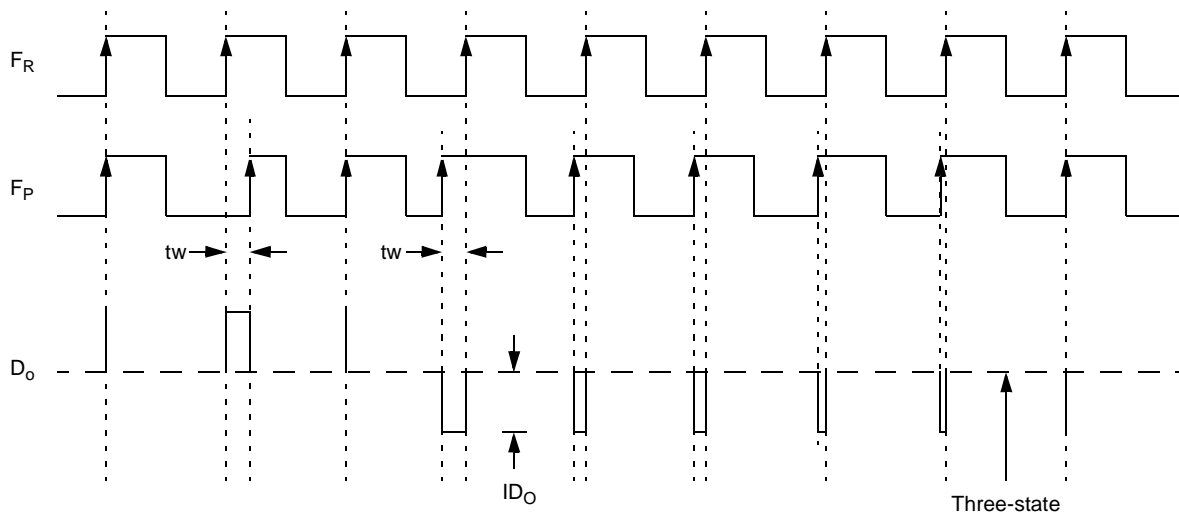
When FC is set HIGH or OPEN CIRCUIT,  $F_{out}$  pin is set to the reference divider output,  $F_R$ . When FC is set LOW,  $F_{out}$  pin is set to the programmable divider output  $F_P$ .



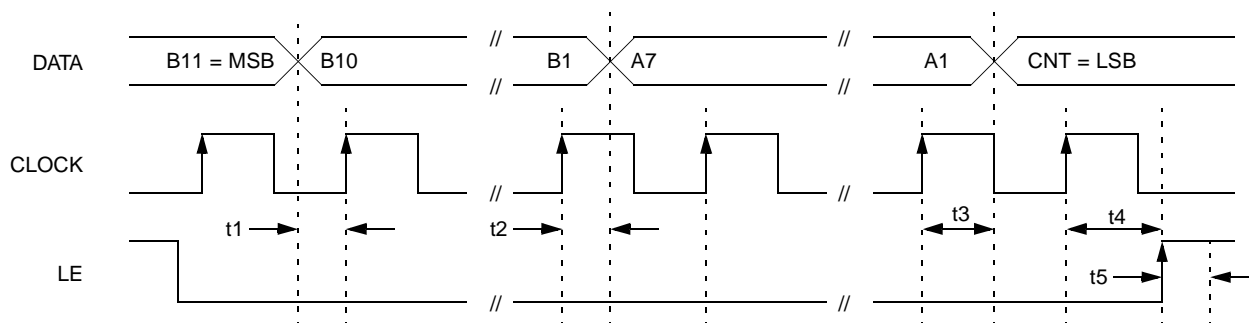
### Phase Detector Output Waveform



### $D_O$ Charge Pump Output Current Waveform



**Timing Waveforms** (continued)

**Serial Data Input Timing Waveform**<sup>[2, 3, 4, 5]</sup>

**Serial Data Input**

Data is input serially using the DATA, CLOCK, and LE pins. Two control bits direct data into the locations given in *Table 1*.

**Table 1. Control Configuration**

CNT	Function
1	<b>Reference Counter:</b> R = 3 to 16383, set prescaler ratio PRE =0:128/129, PRE=1:64/65
0	<b>Program Counter:</b> A = 0 to 127, B = 3 to 2047

**Table 2. Shift Register Configuration**<sup>[6]</sup>

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
<b>Reference Counter and Configuration Bits</b>																		
CNT	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	PRE			
<b>Programmable Counter Bits</b>																		
CNT	A1	A2	A3	A4	A5	A6	A7	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11
<b>Bit(s) Name</b>		<b>Function</b>																
CNT		<b>Control Bit:</b> Directs programming data to reference or programmable counters.																
R1–R14		<b>Reference Counter Setting Bits:</b> 14 bits, R = 3 to 16383. <sup>[7]</sup>																
PRE		<b>Prescaler Divide Bit:</b> LOW = 128/129 and HIGH = 64/65.																
A1–A7		<b>Swallow Counter Divide Ratio:</b> A = 0 to 127.																
B1–B11		<b>Programmable Counter Divide Ratio:</b> B = 3 to 2047. <sup>[7]</sup>																

**Notes:**

2.  $t1-t5 = 50 \mu s > t > 0.5 \mu s$ .
3. CLOCK may remain HIGH after latching in data.
4. DATA is shifted in with the MSB first.
5. For DATA definitions, refer to *Table 2*.
6. The MSB is loaded in first.
7. Low count ratios may violate frequency limits of the phase detector.

**Table 3. 7-Bit Swallow Counter (A) Truth Table<sup>[8]</sup>**

Divide Ratio A	A7	A6	A5	A4	A3	A2	A1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
...	...	...	...	...	...	...	...
126	1	1	1	1	1	1	0
127	1	1	1	1	1	1	1

**Table 4. 11-Bit Programmable Counter (B) Truth Table<sup>[9]</sup>**

Divide Ratio B	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
...	...	...	...	...	...	...	...	...	...	...	...
2046	1	1	1	1	1	1	1	1	1	1	0
2047	1	1	1	1	1	1	1	1	1	1	1

**Table 5. 14-Bit Programmable Reference Counter Truth Table<sup>[9]</sup>**

Divide Ratio R	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
16382	1	1	1	1	1	1	1	1	1	1	1	1	1	0
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

**Ordering Information<sup>[10]</sup>**

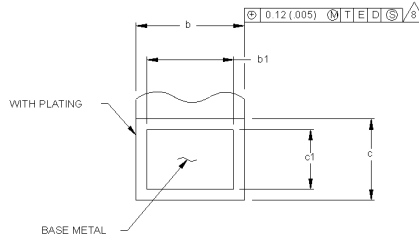
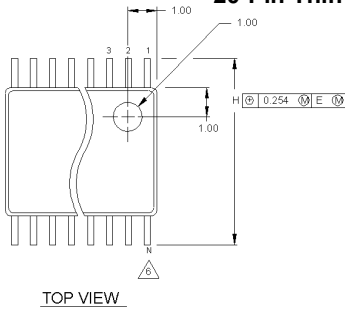
Ordering Code	Package Name	Package Type	TR
CYW2320	ZI	20-pin TSSOP (0.173" wide)	Tape and Reel Option

**Notes:**

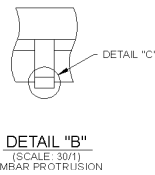
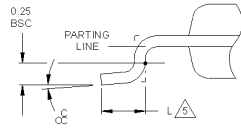
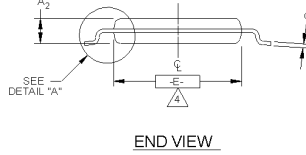
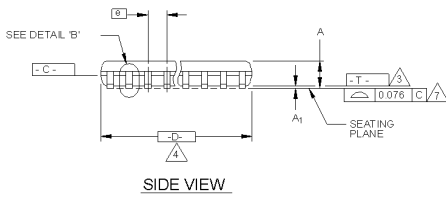
8. B is greater than or equal to A.
9. Divide ratio less than 3 is prohibited. The divide ratio can be calculated using the following equation:  

$$fvco = \{(P * B) + A\} * fosc / R \text{ where } (A \leq B)$$
 fvco: Output frequency of the external VCO.  
 fosc: The crystal reference oscillator frequency.  
 A: Preset divide ratio of the 7-bit swallow counter.  
 B: Preset ratio of the 11-bit programmable counter (3 to 2047).  
 P: Preset divide ratio of the dual modulus prescaler.  
 R: Preset ratio of the 15-bit programmable reference counter (3 to 16383).  
 The divide ratio N = (P \* B) + A.
10. Operating temperature range: -40°C to +85°C.



**Package Diagram**
**20-Pin Thin Shrink Small Outline Package (TSSOP, 0.173" wide)**


**DETAIL "C"**  
SCALE: 120/1  
(SEE NOTE 9)


**NOTES:**

- DIE THICKNESS ALLOWABLE IS 0.279±0.0127 (0.110±0.005 INCHES)
- DIMENSIONING & TOLERANCES PER ANS I Y 14.5M-1982.
- "T" IS A REFERENCE DATUM.
- "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
- TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
- FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.076mm AT SEATING PLANE. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND AN ADJACENT LEAD TO BE 0.14mm SEE DETAILS "B" AND "C".
- DETAIL "C" TO BE DETERMINED AT 0.10 TO 0.25 MM FROM THE LEAD TIP.
- CONTROLLING DIMENSION: MILLIMETERS.
- THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-153. VARIATIONS AA, AB, AC, AD AND AE.

**THIS TABLE IN MILLIMETERS**

SYMBOL	COMMON DIMENSIONS			NOTE VARIATIONS	4 D			6 N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A			1.10	AA	2.90	3.00	3.10	8
A <sub>1</sub>	0.05	0.10	0.15	AB	4.90	5.00	5.10	14
A <sub>2</sub>	0.85	0.90	0.95	AC	4.90	5.00	5.10	16
b	0.19	-	0.30	AD	6.40	6.50	6.60	20
b1	0.19	0.22	0.25	AE	7.70	7.80	7.90	24
c	0.090	-	0.20	AF	9.60	9.70	9.80	28
c1	0.090	0.127	0.135					
D	SEE VARIATIONS			4				
E	4.30	4.40	4.50	4				
e	0.65 BSC							
H	6.25	6.40	6.50					
L	0.50	0.60	0.70	5				
N	SEE VARIATIONS			6				
α	0°	4°	8°					

**THIS TABLE IN INCHES**

SYMBOL	COMMON DIMENSIONS			NOTE VARIATIONS	4 D			6 N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A			.0433	AA	.114	.118	.122	8
A <sub>1</sub>	.002	.004	.006	AB	.193	.197	.201	14
A <sub>2</sub>	.0335	.0354	.0374	AC	.193	.197	.201	16
b	.0075	-	.0118	AD	.252	.256	.260	20
b1	.0075	.0087	.0098	AE	.303	.307	.311	24
c	.0035	-	.0079	AF	.378	.382	.386	28
c1	.0035	.0050	.0053					
D	SEE VARIATIONS			4				
E	.169	.173	.177	4				
e	.0256 BSC							
H	.246	.252	.256					
L	.020	.024	.028	5				
N	SEE VARIATIONS			6				
α	0°	4°	8°					

\*VARIATION AF IS DESIGNED BUT NOT TOOLED\*