SONY

CXA3555N

All Band Tuner IC with On-chip PLL

Description

The CXA3555N is a monolithic TV tuner IC which integrates local oscillator and mixer circuits for VHF band, local oscillator and mixer circuits for UHF band, an IF amplifier and a tuning PLL onto a single chip, enabling further miniaturization of the tuner.

Features

- Low power consumption (5V, 63mA typ.)
- Low noise figure, low distortion characteristics
- High gain/low gain selectable
- Supports IF double-tuned/adjacent channel trap
- Balanced oscillator circuits (3 sets) with excellent oscillation stability
- On-chip PLL supports I^2C bus
- On-chip high voltage drive transistor for charge pump
- Frequency step selectable from 31.25, 50 or 62.5kHz (when using a 4MHz crystal)
- Low-phase noise synthesizer
- On-chip 4-output band switch (output voltage: 5V, current capacity: 5mA)
- 30-pin SSOP small package

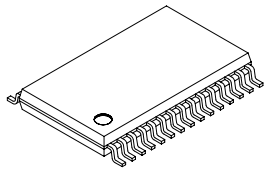
Applications

- TV tuners
- VCR tuners
- CATV tuners

Structure

Bipolar silicon monolithic IC

30 pin SSOP (Plastic)



Absolute Maximum Ratings

• Supply voltage	V_{CC}	–0.3 to +5.5	V
• Operating temperature	Topr	–25 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C
• Allowable power dissipation	P_D	580	mW

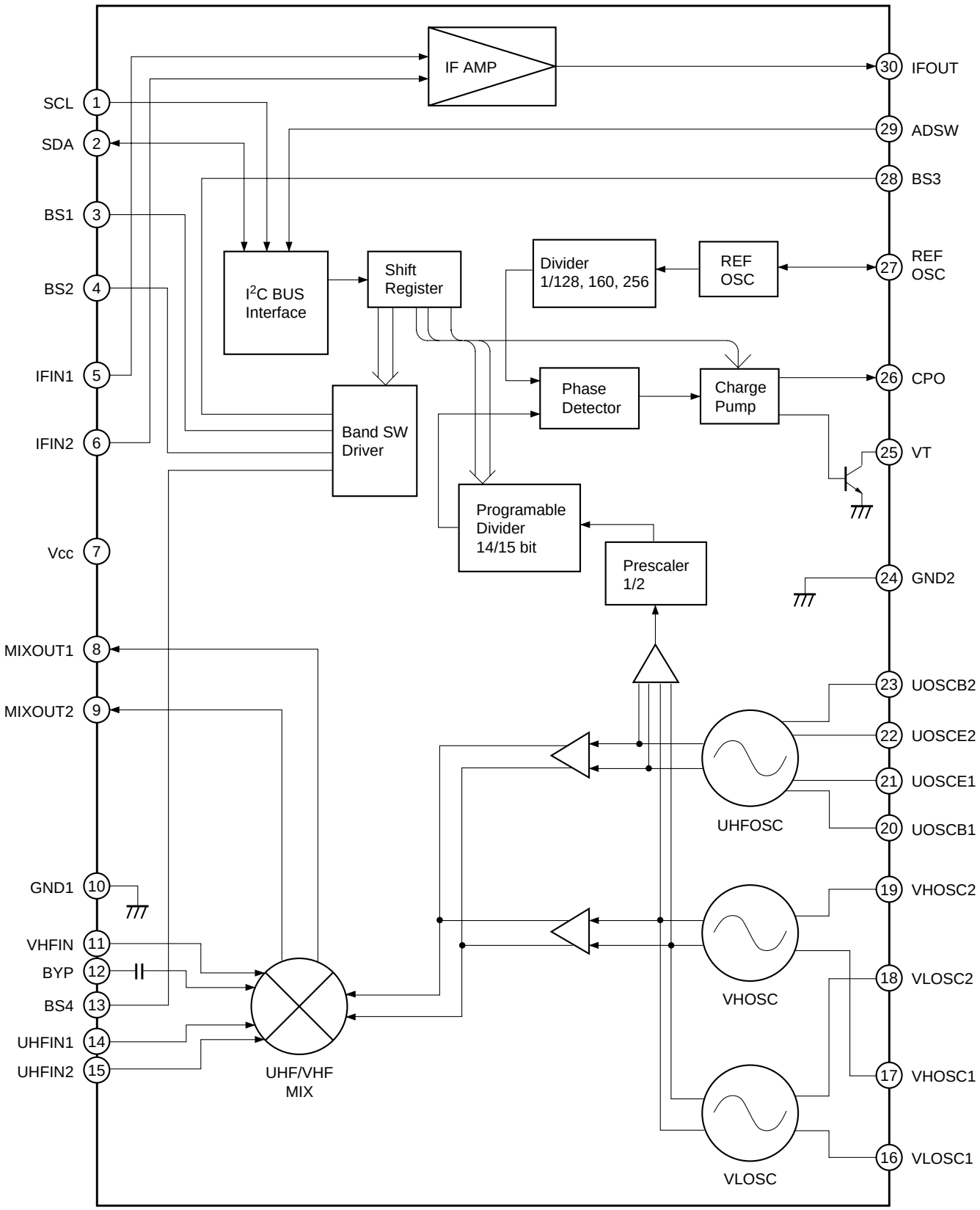
Operating Conditions

Supply voltage	V_{CC}	4.75 to 5.30	V

Note: This IC has pins whose electrostatic discharge strength is weak as the operating frequency is high and the high-frequency process is used for this IC. Take care of handling the IC.

E01326-PS

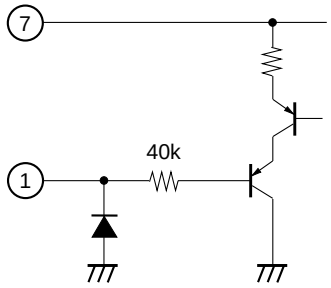
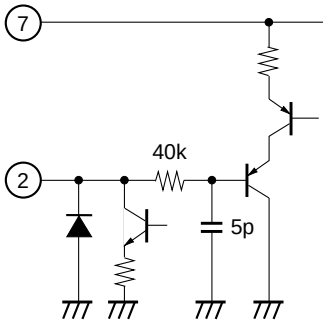
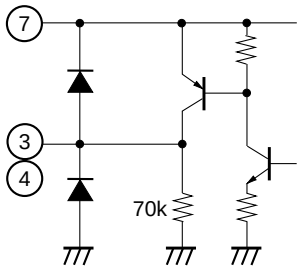
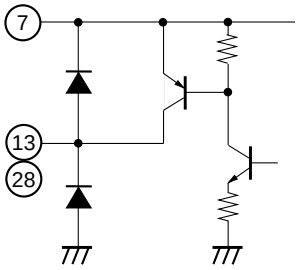
Block Diagram and Pin Configuration

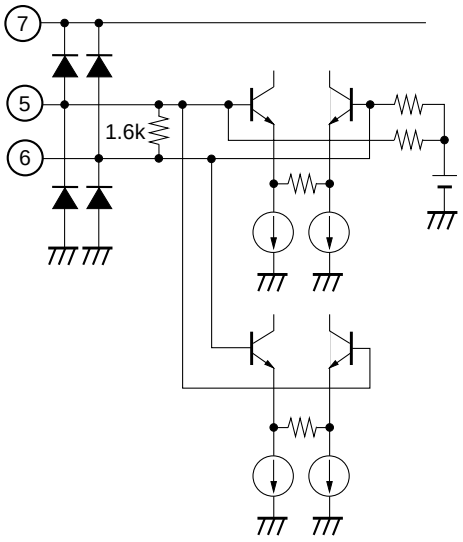
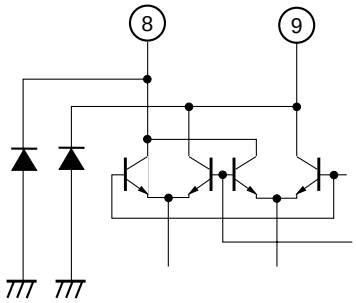
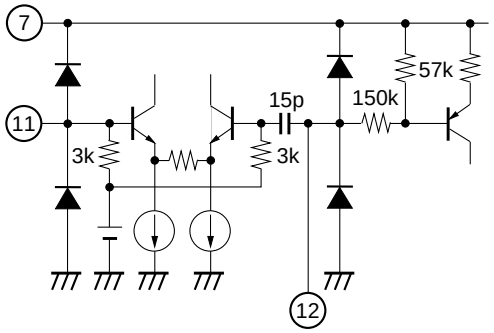
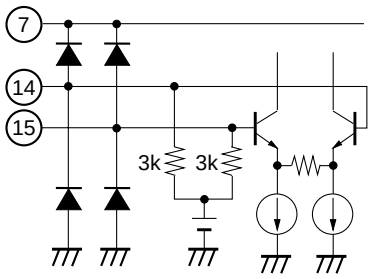


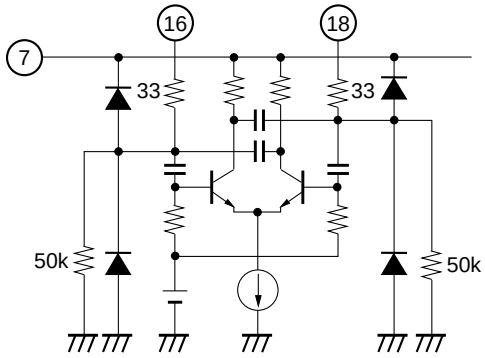
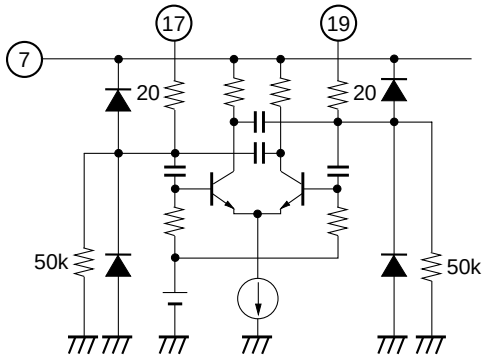
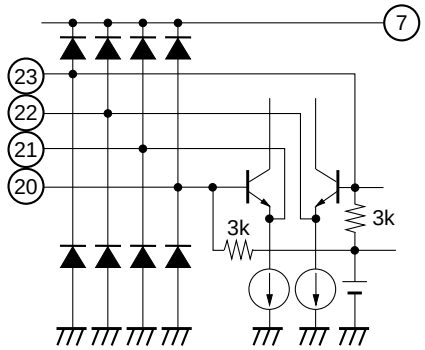
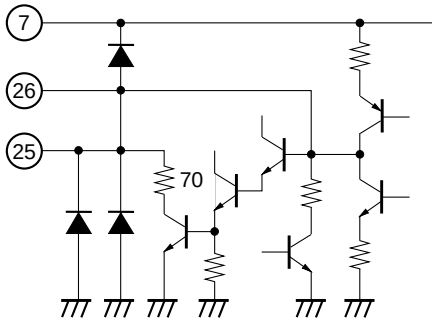
Pin Description

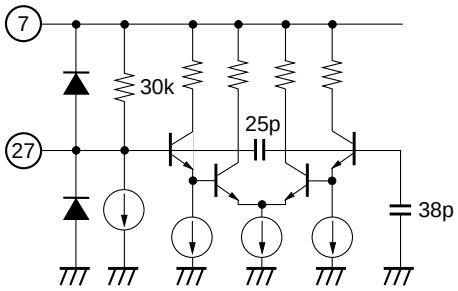
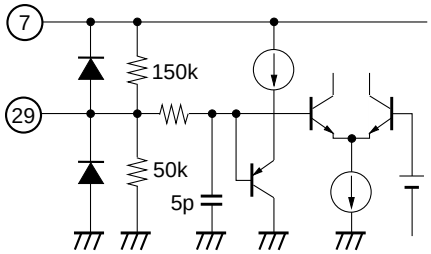
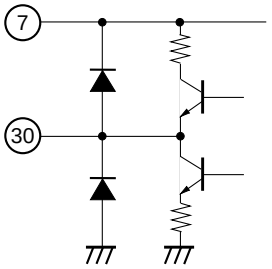
Pin No.	Symbol	Description
1	SCL	SCL input
2	SDA	SDA I/O
3	BS1	Band switch output 1
4	BS2	Band switch output 2
5	IFIN1	IF amplifier input
6	IFIN2	IF amplifier input
7	Vcc	Power supply
8	MIXOUT1	MIX output (open collector)
9	MIXOUT2	MIX output (open collector)
10	GND1	Analog circuit GND
11	VHFIN	VHF input
12	BYP	VHF input GND and gain switching (low: GND, high: open)
13	BS4	Band switch output 4
14	UHFIN1	UHF input
15	UHFIN2	UHF input
16	VLOSC1	VHF Low-band oscillator
17	VHOSC1	VHF High-band oscillator
18	VLOSC2	VHF Low-band oscillator
19	VHOSC2	VHF High-band oscillator
20	UOSCB1	UHF oscillator (base pin)
21	UOSCE1	UHF oscillator (emitter pin)
22	UOSCE2	UHF oscillator (emitter pin)
23	UOSCB2	UHF oscillator (base pin)
24	GND2	PLL circuit GND
25	VT	Tuning voltage output (open collector)
26	CPO	Charge pump output (loop filter connection)
27	REFOSC	Crystal connection for PLL reference oscillator
28	BS3	Band switch output 3
29	ADSW	Address selection (I^2C bus)
30	IFOUT	IF amplifier output

Pin Description

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Pin voltage [V]</th><th>Equivalent circuit</th><th>Description</th></tr>
<tr><td>1</td><td>SCL</td><td>—</td><td> 
</td><td>Clock input</td></tr>
<tr><td>2</td><td>SDA</td><td>—</td><td> 
</td><td>Data input</td></tr>
<tr><td>3</td><td>BS1</td><td rowspan="4">High: 4.9
Low: 0.0</td><td rowspan="2"> 
</td><td rowspan="4">Band switch outputs.
This pin corresponding to the selected band goes High.</td></tr>
<tr><td>4</td><td>BS2</td></tr>
<tr><td>13</td><td>BS4</td><td rowspan="2"> 
</td></tr>
<tr><td>28</td><td>BS3</td></tr>
</table>

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
5	IFIN1	2.0		IF inputs. These pins must be connected to the mixer outputs via coupling capacitance.
6	IFIN2			
7	V_{CC}	—		Power supply.
8	MIXOUT1	—		Mixer outputs. These pins output the signal in open collector format, and they must be connected to the power supply via a load.
9	MIXOUT2			
10	GND1	—		Analog circuit GND.
11	VHFIN	2.4 during VHF reception 0.0 during UHF reception		VHF input. The input format is unbalanced input.
12	BYP	V_{CC} (when open)		VHF input GND and gain switching. GND: low gain Open: high gain (However, when control byte GC is "0")
14	UHFIN1	0.0 during VHF reception 2.3 during UHF reception		UHF inputs. Input a balanced signal to Pins 14 and 15, or ground either of Pin 14 or 15 with a capacitor and input the signal to the other pin.
15	UHFIN2			

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
16	VLOSC1	0.0		External resonance circuit connection for VL oscillator.
18	VLOSC2			
17	VHOSC1	0.0		External resonance circuit connection for VH oscillator.
19	VHOSC2			
20	UOSCB1	2.4 during VHF reception 2.2 during UHF reception		External resonance circuit connection for UHF oscillator.
21	UOSCE1	2.0 during VHF reception 1.5 during UHF reception		
22	UOSCE2	2.0 during VHF reception 1.5 during UHF reception		
23	UOSCB2	2.4 during VHF reception 2.2 during UHF reception		
24	GND2	—		PLL circuit GND.
25	VT	—		Varicap drive voltage output. This pin outputs the signal in open collector format, and it must be connected to the tuning power supply via a load.
26	CPO	2.0		Charge pump output. Connects the loop filter.

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
27	REFOSC	4.4		Crystal connection for reference oscillator.
29	ADSW	1.25 (when open)		Address selection. Controls address bits 1 and 2.
30	IFOUT	2.8		IF output.

Electrical Characteristics (See the Electrical Characteristics Measurement Circuit.)

Circuit Current

(Vcc = 5V, IFVcc = 5V, Ta = 25°C)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Circuit current	Iccv	Vcc current Band switch output open during VHF operation	35	56	78	mA
	Iccu	Vcc current Band switch output open during UHF operation	35	56	78	mA

OSC/MIX/IF Amplifier Block

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Conversion gain*1	CG1	VHF operation fRF = 55MHz High gain mode	19.0	22.0	25.0	dB
	CG2	VHF operation fRF = 360MHz High gain mode	19.5	22.5	25.5	dB
	CG3	UHF operation fRF = 360MHz High gain mode	23.0	26.0	29.0	dB
	CG4	UHF operation fRF = 800MHz High gain mode	23.0	26.0	29.0	dB
	CG5	VHF operation fRF = 55MHz Low gain mode	17.0	20.0	23.0	dB
	CG6	VHF operation fRF = 360MHz Low gain mode	17.5	20.5	23.5	dB
	CG7	UHF operation fRF = 360MHz Low gain mode	21.0	24.0	27.0	dB
	CG8	UHF operation fRF = 800MHz Low gain mode	21.0	24.0	27.0	dB
Noise figure*1, *2	NF1	VHF operation fRF = 55MHz High gain mode		12	15	dB
	NF2	VHF operation fRF = 360MHz High gain mode		12	15	dB
	NF3	UHF operation fRF = 360MHz High gain mode		10	13	dB
	NF4	UHF operation fRF = 800MHz High gain mode		11	14	dB
	NF5	VHF operation fRF = 55MHz Low gain mode		13	16	dB
	NF6	VHF operation fRF = 360MHz Low gain mode		13	16	dB
	NF7	UHF operation fRF = 360MHz Low gain mode		11	14	dB
	NF8	UHF operation fRF = 800MHz Low gain mode		12	15	dB
1% cross modulation 1*1, *3	CM1	VHF operation fD = 55MHz fUD = ±12MHz (30% AM) High gain mode	99	103		dBµ
	CM2	VHF operation fD = 360MHz fUD = ±12MHz (30% AM) High gain mode	99	103		dBµ
	CM3	UHF operation fD = 360MHz fUD = ±12MHz (30% AM) High gain mode	97	101		dBµ
	CM4	UHF operation fD = 800MHz fUD = ±12MHz (30% AM) High gain mode	94	98		dBµ
	CM5	VHF operation fD = 55MHz fUD = ±12MHz (30% AM) Low gain mode	100	104		dBµ
	CM6	VHF operation fD = 360MHz fUD = ±12MHz (30% AM) Low gain mode	100	104		dBµ
	CM7	UHF operation fD = 360MHz fUD = ±12 MHz (30% AM) Low gain mode	98	102		dBµ
	CM8	UHF operation fD = 800MHz fUD = ±12 MHz (30% AM) Low gain mode	94	98		dBµ
Maximum output power	Pomax	50Ω load, saturation output	8	11		dBm

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Switch ON drift (PLL not operating) *4	Δfsw1	VHF operation fosc = 100MHz Δf from 3s to 3min after switch ON			±300	kHz
	Δfsw2	VHF operation fosc = 405MHz Δf from 3s to 3min after switch ON			±600	kHz
	Δfsw3	UHF operation fosc = 405MHz Δf from 3s to 3min after switch ON			±350	kHz
	Δfsw4	UHF operation fosc = 845MHz Δf from 3s to 3min after switch ON			±400	kHz
Supply voltage drift (PLL not operating) *4	Δfst1	VHF operation fosc = 100MHz Δf when Vcc 5V changes ±5%			±100	kHz
	Δfst2	VHF operation fosc = 405MHz Δf when Vcc 5V changes ±5%			±450	kHz
	Δfst3	UHF operation fosc = 405MHz Δf when Vcc 5V changes ±5%			±100	kHz
	Δfst4	UHF operation fosc = 845MHz Δf when Vcc 5V changes ±5%			±100	kHz
Oscillator phase noise	C/N1	VHF operation 10kHz offset CP = 1 Phase comparison frequency = 31.25kHz	86			dBc/Hz
	C/N2	UHF operation 10kHz offset CP = 1 Phase comparison frequency = 31.25kHz	80			dBc/Hz

*1 Value measured with untuned input.

*2 NF meter direct-reading value (DSB measurement).

*3 Value with a desired reception signal input level of –30dBm, an interference signal of 100kHz/30% AM, and an interference signal level where S/I = 46dB measured with a spectrum analyzer.

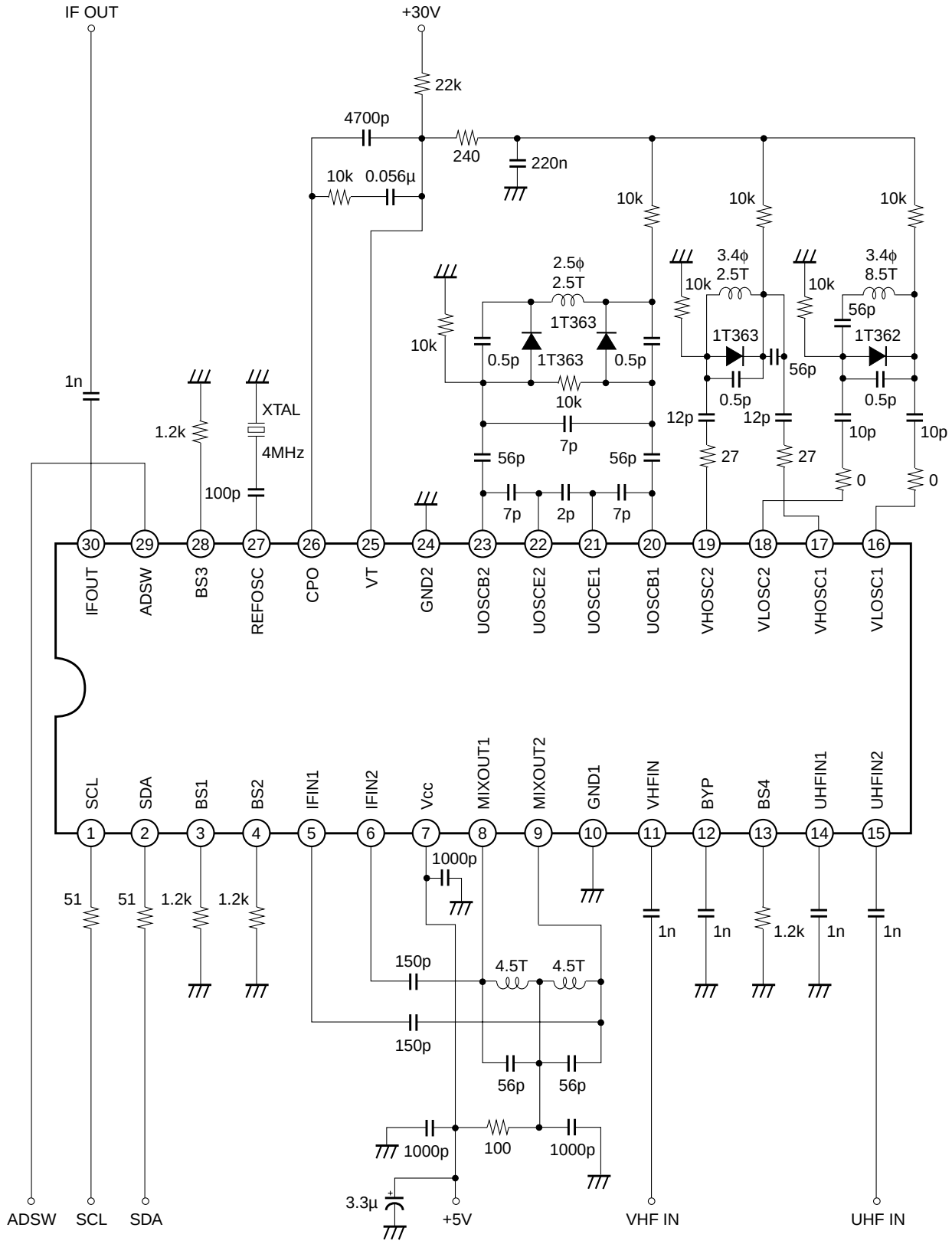
*4 Value when the PLL is not operating.

PLL Block

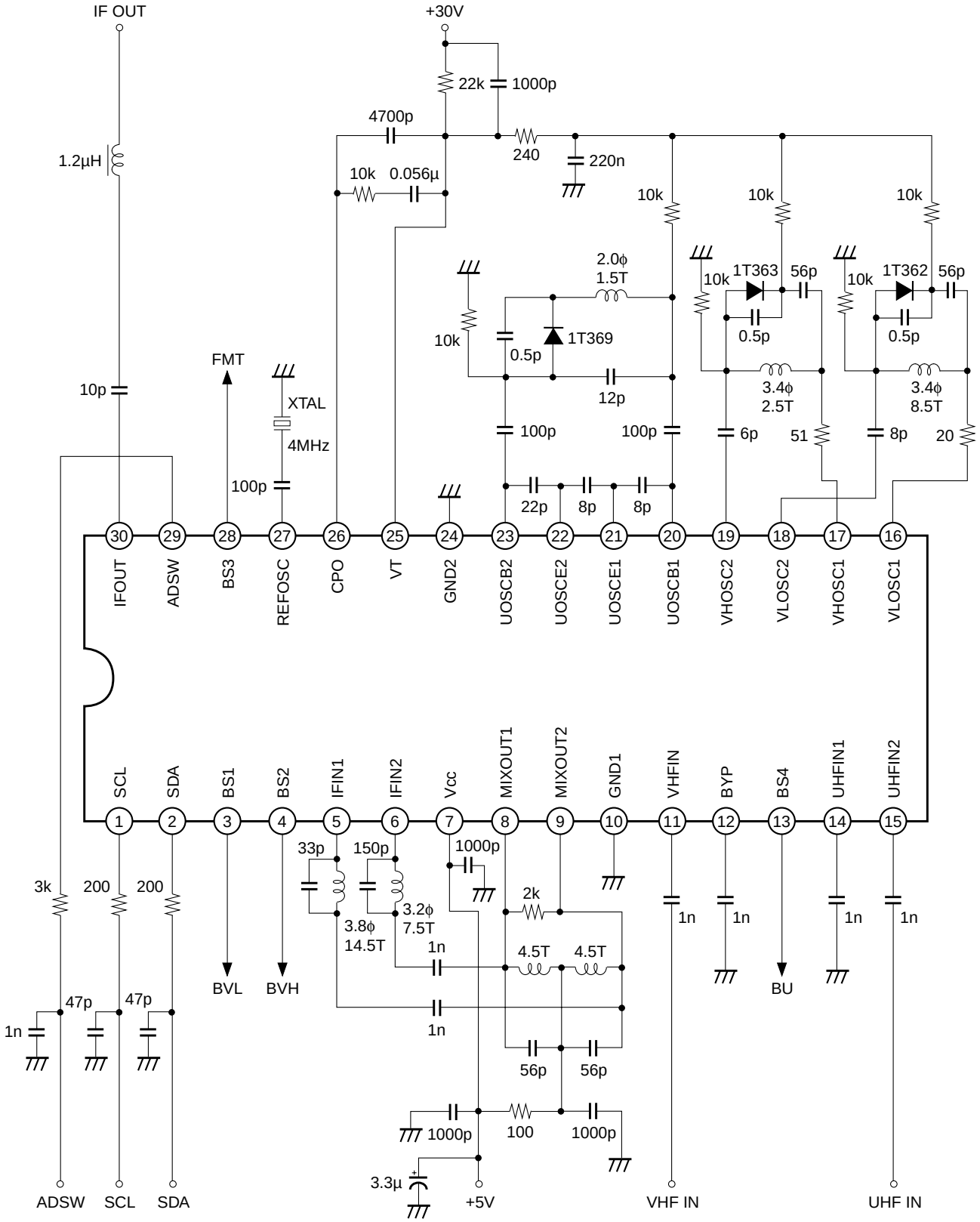
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Lock-up time	LUT1	VHF operation CP = 1 fosc 100MHz ↔ fosc 405MHz			50	ms
	LUT2	UHF operation CP = 1 fosc 405MHz ↔ fosc 845MHz			50	ms
Reference leak	REFL	Phase comparison frequency = 31.25kHz CP = 1	54			dBc
CL and DA inputs						
"H" level input voltage	V_{IH}		3		Vcc	V
"L" level input voltage	V_{IL}		GND		1.5	V
"H" level input current	I_{IH}	V_{IH} = Vcc		0	–0.1	µA
"L" level input current	I_{IL}	V_{IL} = GND		–0.2	–4	µA
AD input						
"H" level input voltage	V_{IH}		3		Vcc	V
"L" level input voltage	V_{IL}		GND		1	V
"H" level input current	I_{IH}	V_{IH} = Vcc		100	200	µA
"L" level input current	I_{IL}	V_{IL} = GND		–35	–100	µA
SDA output						
"H" output leak current	I_{SDALK}	V_{IN} = 5.5V			5	µA
"L" output voltage	V_{SDAL}	Sink = –3mA	GND		0.4	V
CPO (charge pump)						
Output current 1	I_{CPO1}	When CP = 0 is selected	±30	±50	±80	µA
Leak current 1	LeakCP1	When CP = 0 is selected			30	nA
Output current 2	I_{CPO2}	When CP = 1 is selected	±120	±200	±320	µA
Leak current 2	LeakCP2	When CP = 1 is selected			100	nA
VT (VC voltage output)						
Maximum output voltage	V_{TH}				34	V
Minimum output voltage	V_{TL}	Sink current = 1mA		0.15	0.8	V
REFOSC						
Oscillation frequency range	F_{XTOSC}		3		12	MHz
Input capacitance	C_{XTOSC}		22	24	26	pF
Negative resistance	R_{NEG}	Crystal source impedance f_{REF} = 4MHz	–1	–3		kΩ
Band SW						
Output current	I_{BS}	When ON			–5	mA
Saturation voltage	V_{SAT}	When ON Source current = 5mA		100	300	mV
Leak current	LeakBS	When OFF IFVcc = 5.5V		0.5	3	µA

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Bus timing (I^2C bus)						
SCL clock frequency	f_{SCL}		0		400	kHz
Start waiting time	$t_{W;STA}$		1300			ns
Start hold time	$t_{H;STA}$		600			ns
Low hold time	t_{LOW}		1300			ns
High hold time	t_{HIGH}		600			ns
Start setup time	$t_{S;STA}$		600			ns
Data hold time	$t_{H;DAT}$		0		900	ns
Data setup time	$t_{S;DAT}$		600			ns
Rise time	t_R				300	ns
Fall time	t_F				300	ns
Stop setup time	$t_{S;STO}$		600			ns

Electrical Characteristics Measurement Circuit



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Functions

The CXA3555N is an analog terrestrial TV broadcasting tuner IC which converts frequencies to IF in order to tune and detect only the desired reception frequency of VHF and UHF band signals.
In addition to the mixer, local oscillation and IF amplifier circuits required for frequency conversion to IF, this IC also integrates a PLL circuit for local oscillation frequency control onto a single chip.
The functions of the various circuits are described below.

1. Mixer circuit

This circuit outputs the frequency difference between the signal input to VHFIN or UHFIN and the local oscillation signal.

2. Local oscillation circuit

A VCO is formed by externally connecting an LC resonance circuit composed of a varicap diode and inductance.

3. IF amplifier circuit

This circuit amplifies the mixer IF output, and consists of an amplifier stage and low impedance output stage.

4. PLL circuit

This PLL circuit fixes the local oscillation frequency to the desired frequency. It consists of a programmable divider, reference divider, phase comparator, charge pump and reference oscillator. The control format supports the I^2C bus format.

The frequency steps of 31.25, 50 or 62.5kHz can be selected by the I^2C bus data-based reference divider frequency division setting value.

5. Band switch circuit

The CXA3555N has four sets of built-in PNP transistors for switching between the VL, VH and UHF bands and for switching the FM trap, etc. These PNP transistors can be controlled by the bus data.

The emitters for these PNP transistors are connected to the power supply pin (V_{CC}), and are ON and output 5V when the bus data is "1 (H)".

Description of Analog Block Operation (See the Electrical Characteristics Measurement Circuit.)

VHF-Low oscillator circuit

- This is a completely balanced oscillator circuit. The oscillation frequency is varied by connecting an LC parallel resonance circuit including a varicap between Pins 16 and 18 via coupled capacitance and controlling the voltage applied to the varicap.

VHF-High oscillator circuit

- This is a completely balanced oscillator circuit. The oscillation frequency is varied by connecting an LC parallel resonance circuit including a varicap between Pins 17 and 19 via coupled capacitance and controlling the voltage applied to the varicap.

VHF mixer circuit

- The mixer circuit employs a double balanced mixer with little local oscillation signal leakage.
  The input format is base input type, with Pin 12 grounded either directly or via a capacitor and the RF signal input to Pin 11.
  (Pin 12 can also be used to switch the IC gain according to the applied DC voltage value. When switching the gain with Pin 12, the GC bit of the PLL data must be set to "0".)
- The RF signal is fed from the oscillator, converted to IF frequency and output from Pins 8 and 9. Pins 8 and 9 are open collectors, so external power feed is necessary. Also, connect single-tuned filters to Pins 8 and 9.

UHF oscillator circuit

- The oscillator circuit is designed so that two collector ground type Colpitts oscillators perform differential oscillation operation via an LC resonance circuit including a varicap.
- Resonance capacitance is connected between Pins 20 and 21, Pins 21 and 22, and Pins 22 and 23, and an LC resonance circuit including a varicap is connected between Pins 20 and 23.

UHF mixer circuit

- This circuit employs a double balanced mixer like the VHF mixer circuit.
  The input format is base input type, with Pins 14 and 15 as the RF input pins. The input method can be selected from balanced input consisting of differential input to Pins 14 and 15 or unbalanced input consisting of grounding Pin 14 via a capacitor and input to Pin 15.
- Pins 8 and 9 are the mixer outputs. Pins 8 and 9 are open collectors, so external power feed is necessary. Also, connect single-tuned filters to Pins 8 and 9.

IF amplifier circuit

- Pins 5 and 6 are the IF amplifier inputs, and the input impedance is approximately 1.6kΩ.
- The signals frequency converted by the mixer are output from Pins 8 and 9, and Pins 8 and 9 are connected to Pins 5 and 6 via capacitors. (An adjacent channel trap circuit can be formed by connecting LC parallel circuits in place of capacitors.)
- The signal amplified by the IF amplifier is output from Pin 30. The output impedance is approximately 10Ω.

Description of PLL Block

This IC is controlled by the I^2C bus.
The PLL of this IC performs high-speed phase comparison, providing low reference leak and quick lock-up time characteristics.
During power on, the power-on reset circuit operates to initialize the frequency data to all "0" and the band data to all "OFF". Power-on reset is performed when $V_{CC} \geq 3.2V$ at room temperature (Ta = 25°C).

1) Address setting

Up to four addresses can be selected by the hardware bit settings, so that multiple PLL can exist within one system.
The responding address can be set according to the ADSW pin voltage.

Address

1	1	0	0	0	MA1	MA0	R/W

Hardware bits

ADSW pin voltage	MA1	MA0
0 to 0.1Vcc	0	0
OPEN or 0.2Vcc to 0.3Vcc	0	1
0.4Vcc to 0.6Vcc	1	0
0.9Vcc to Vcc	1	1

2) Frequency data setting

The VCO lock frequency is obtained according to the following formula.

$fosc = 2 \times fref \times (32M + S)$

fosc: local oscillator frequency
fref: phase comparison frequency
M: main divider frequency division ratio
S: swallow counter frequency division ratio

The variable frequency division ranges of M and S are as follows, and are set as binary.

$S < M \leq 1023$
$0 \leq S \leq 31$

3) Control format

When performing control for this IC, byte 1 contains the address data, bytes 2 and 3 contain the frequency data, byte 4 contains the control data, and byte 5 contains the band switch data.
These data are latch transferred in the manner of byte 1, byte 2 + byte 3, and byte 4 + byte 5.
When the correct address is received and acknowledged, the data is recognized as frequency data if the first bit of the next byte is "0", and as control data and band switch data if this bit is "1".
Also, when data transmission is stopped part-way, the previously programmed data is valid. Therefore, once the control and band switch data have been programmed, 3-byte commands consisting of the address and frequency data are possible.
Further, even if the I^2C bus stop conditions are not met, data can be input by sending the start conditions and the new address.

The control format is as shown in the table below.

Slave Receiver

	MSB							LSB	
Mode	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
Address byte	1	1	0	0	0	MA1	MA0	0	A
Divider byte1	0	M9	M8	M7	M6	M5	M4	M3	A
Divider byte2	M2	M1	M0	S4	S3	S2	S1	S0	A
Control byte	1	CP	GC	CD	X	R1	R0	OS	A
Band SW byte	X	X	X	X	BS4	BS3	BS2	BS1	A

X: Don't care

A: Acknowledge bit
MA0, MA1: address setting
M0 to: main divider frequency division ratio setting
S0 to: swallow counter frequency division ratio setting
CD: charge pump OFF (when "1")
OS: varicap output OFF (when "1")
CP: charge pump current switching (200µA when "1", 50µA when "0")
GC: gain switching (IC gain reduced by 2dB when "1") *1
BS1 to BS4: band switch control (output PNP transistor ON when "1")
R0, R1: reference divider frequency division ratio setting (See the Reference Divider Frequency Division Ratio Table.)

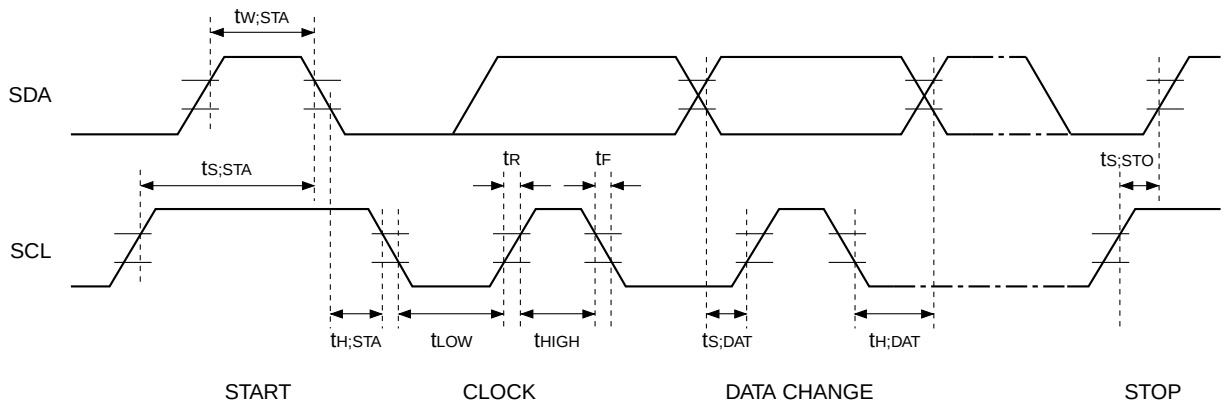
*1 When switching the gain with the PLL data, ground Pin 12 (BYP) via a capacitor.

Reference Divider Frequency Division Ratio Table

R1	R0	Reference Divider
0	1	256
1	1	128
X	0	160

X: Don't care

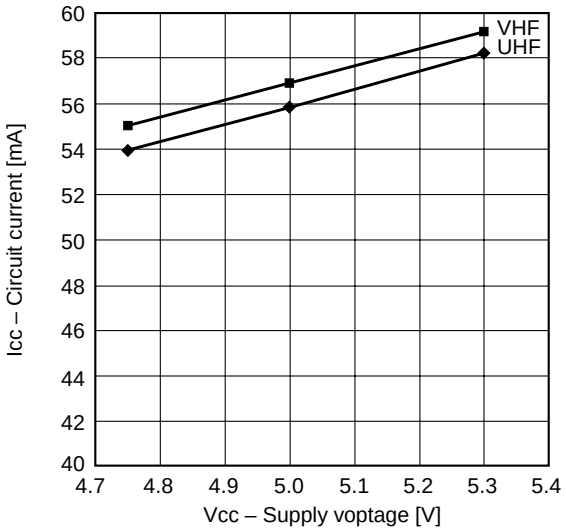
I²C Bus Timing Chart



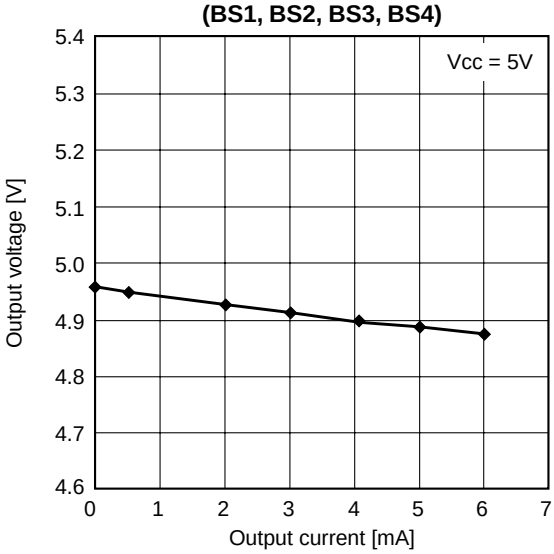
$t_{S;STA}$ = Start setup time
$t_{W;STA}$ = Start waiting time
$t_{H;STA}$ = Start hold time
t_{LOW} = Low clock pulse width
t_{HIGH} = High clock pulse width
$t_{S;DAT}$ = Data setup time
$t_{H;DAT}$ = Data hold time
$t_{S;STO}$ = Stop setup time
t_R = Rise time
t_F = Fall time

Example of Representative Characteristics

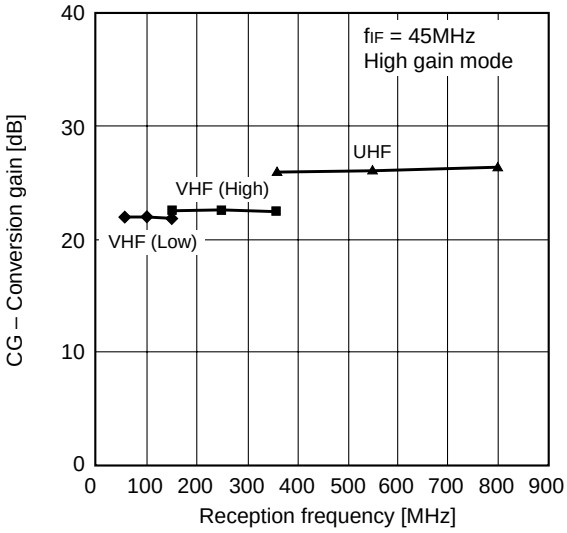
Circuit current vs. Supply voltage



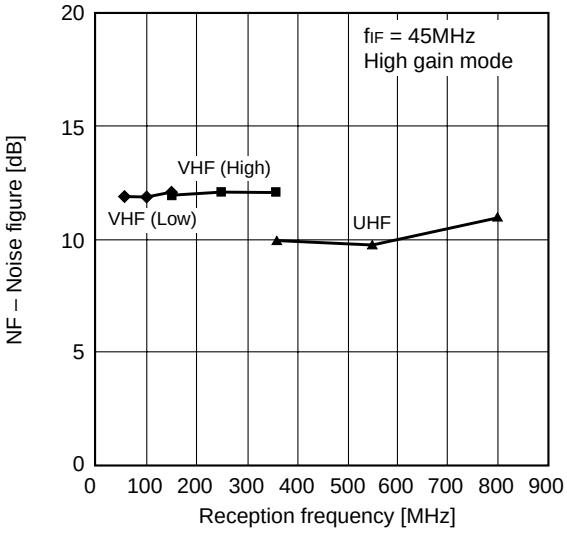
Band SW output voltage vs. Output current (BS1, BS2, BS3, BS4)



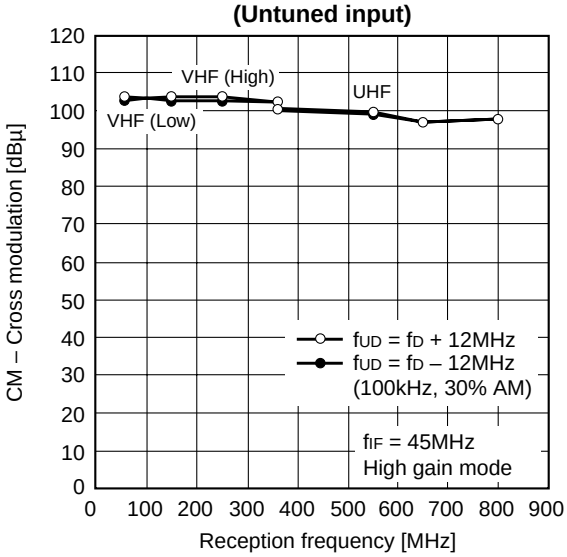
Conversion gain vs. Reception frequency (Untuned input)



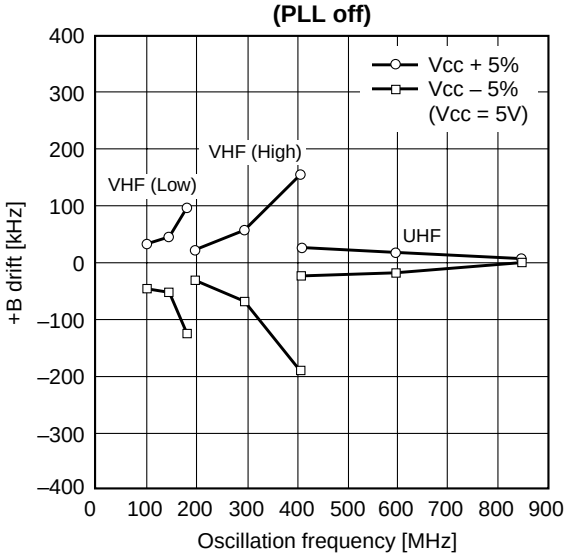
Noise figure vs. Reception frequency (Untuned input, in DSB)



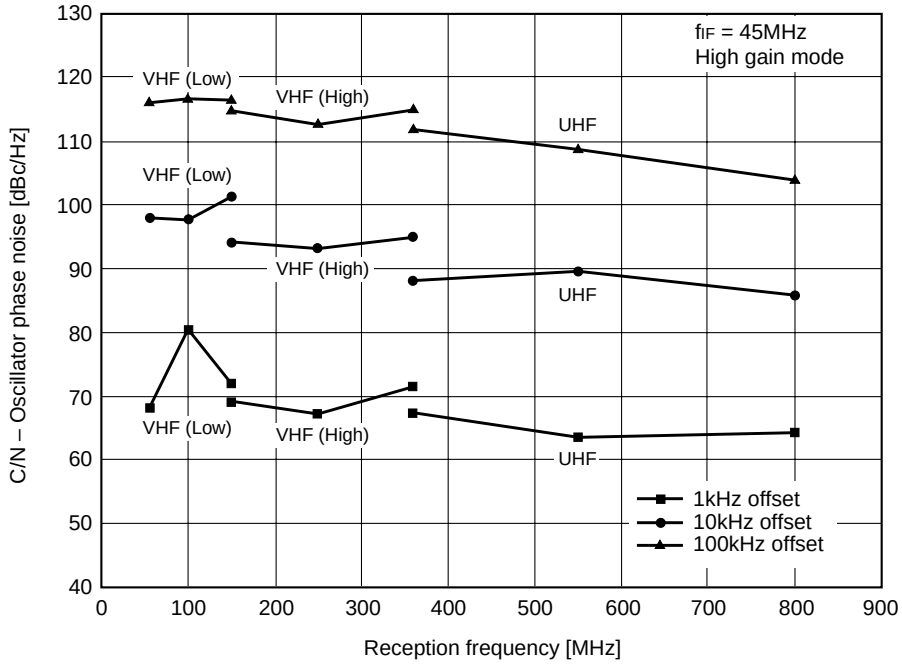
Next adjacent cross modulation vs. Reception frequency (Untuned input)



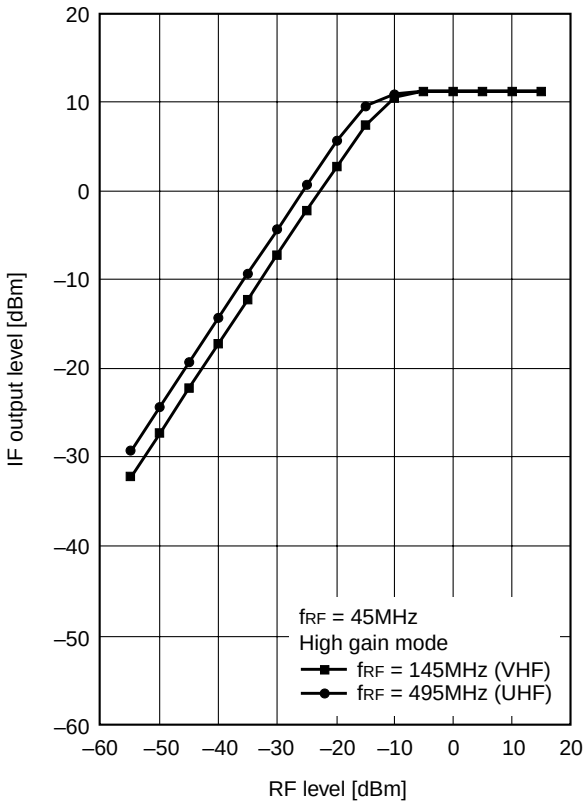
Oscillation frequency power supply fluctuation (PLL off)



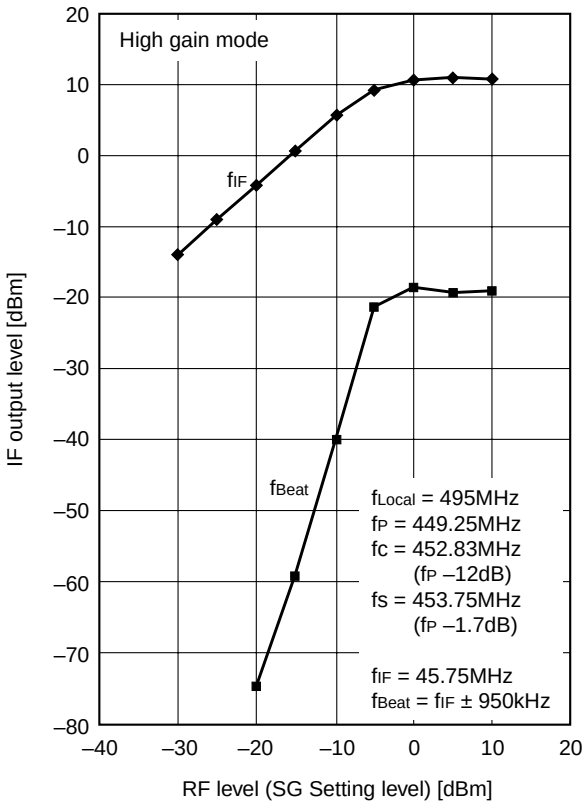
Oscillator phase noise vs. Reception frequency (untuned input)



I/O characteristics (untuned input)

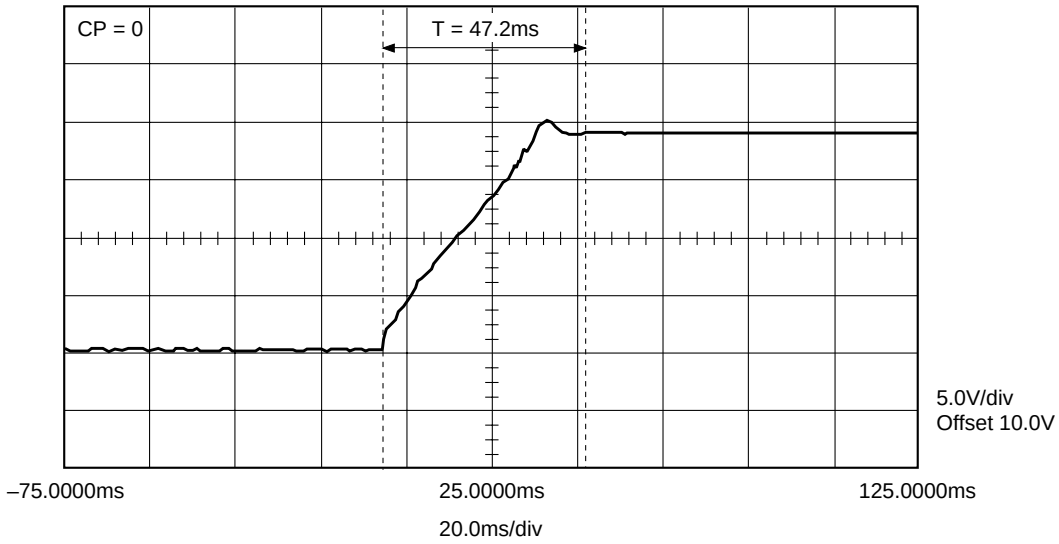


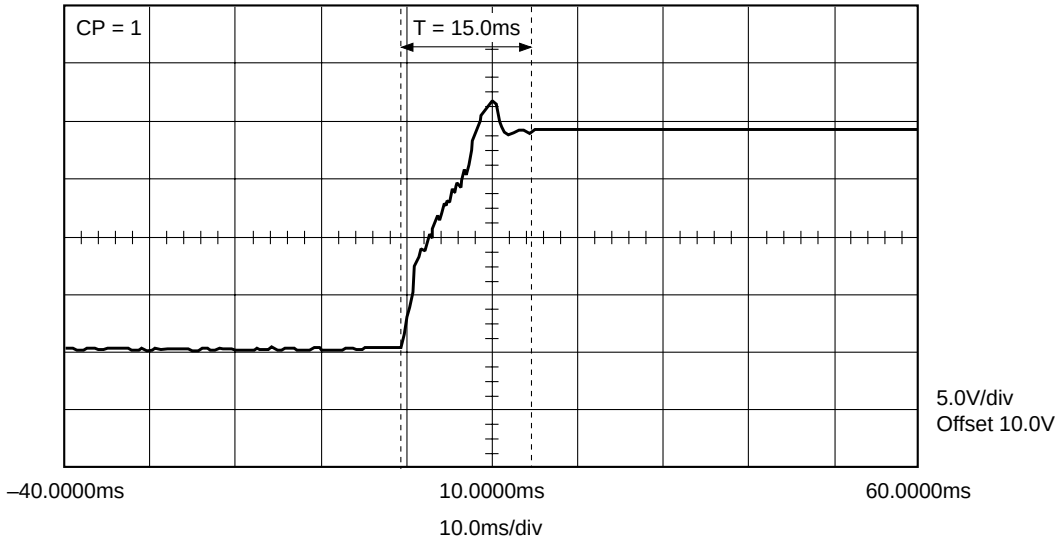
PCS beat characteristics (untuned input)



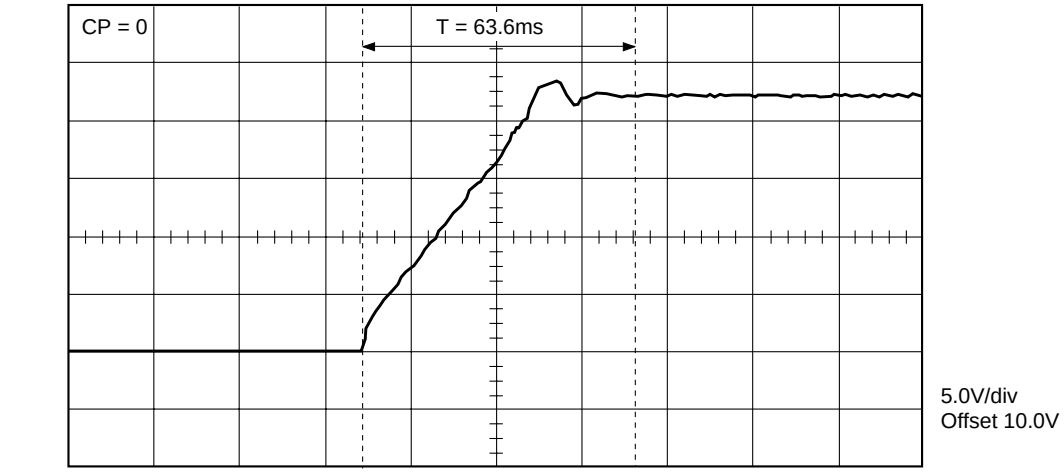
Tuning Response Time

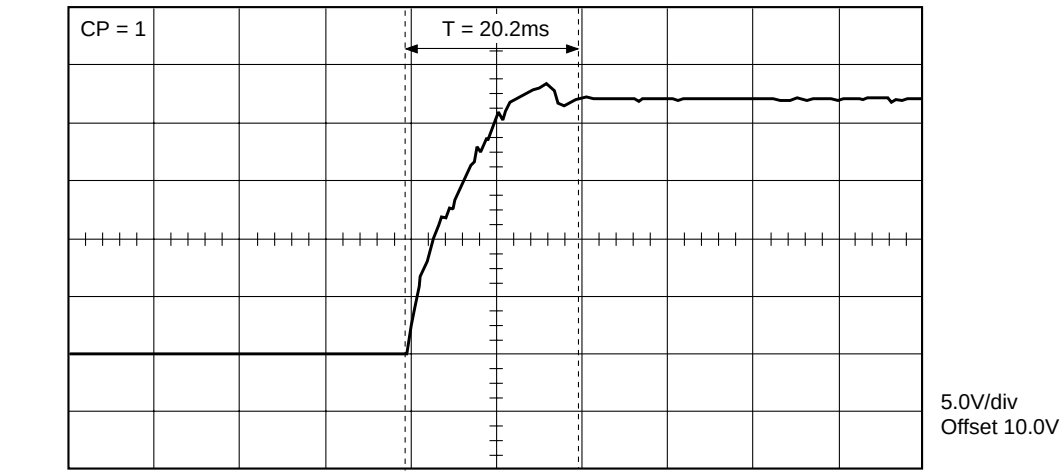
VHF (Low) 95MHz → VHF (High) 395MHz



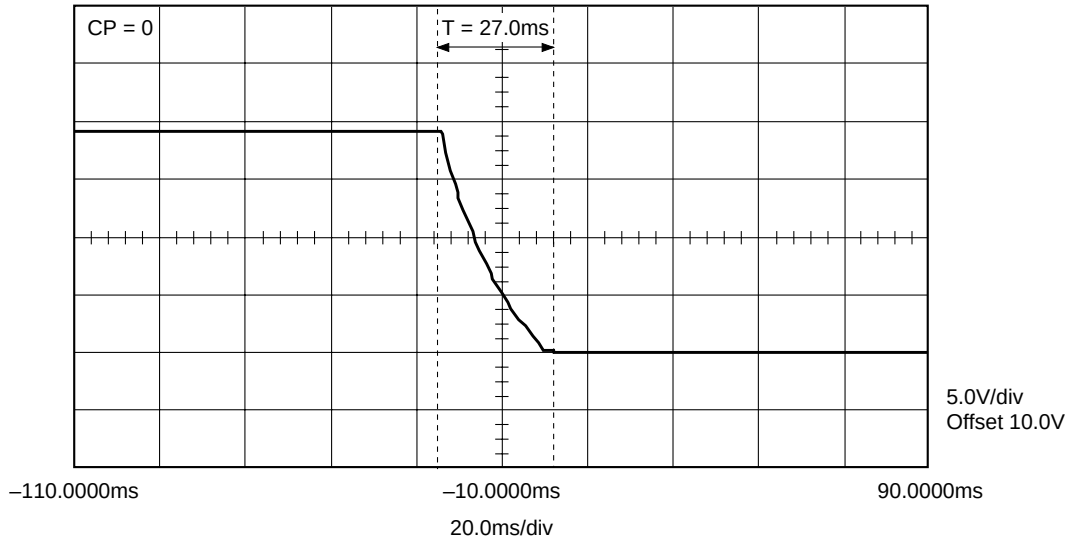


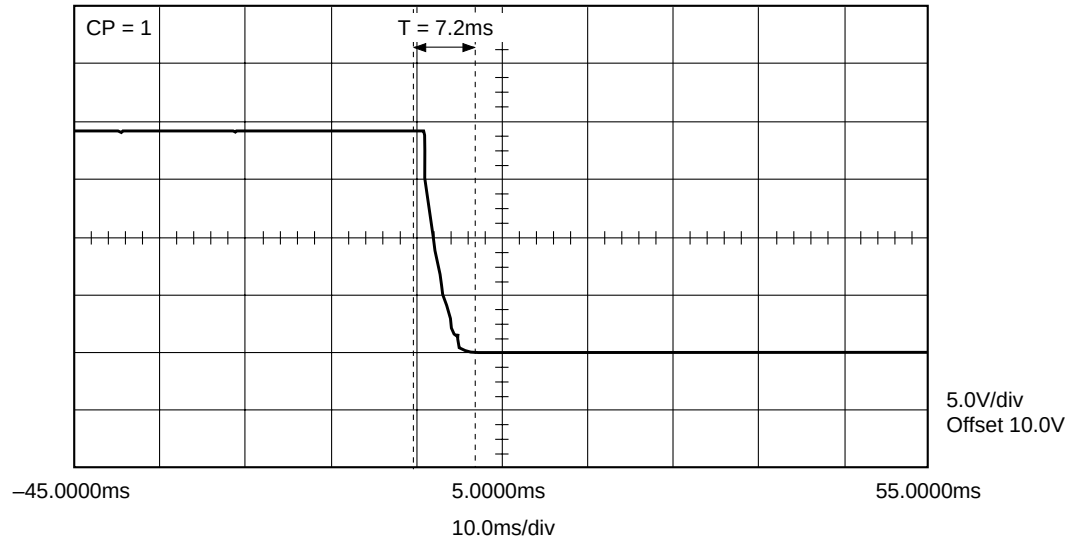
UHF 413MHz → UHF 847MHz



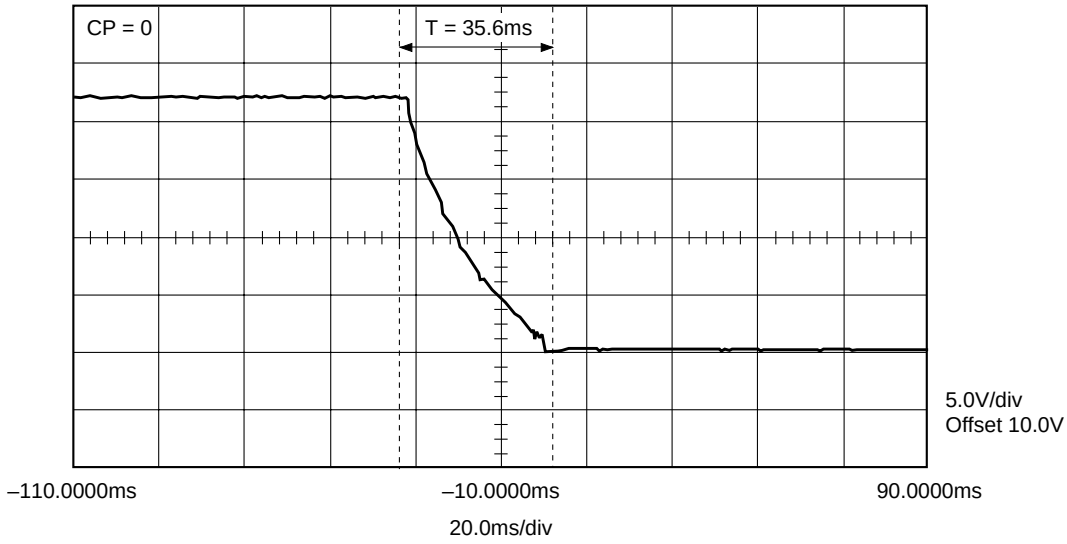


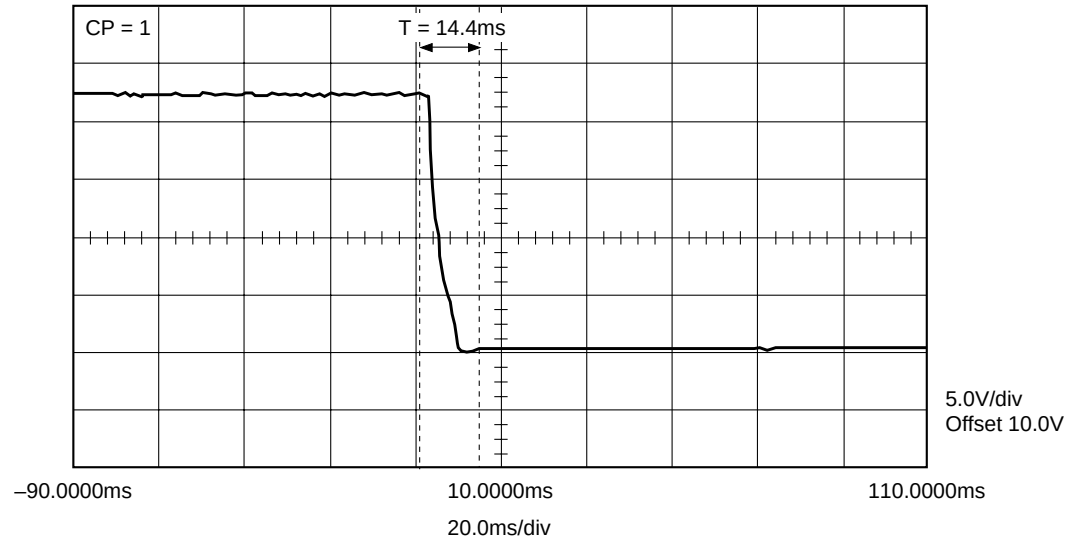
VHF (High) 395MHz → VHF (Low) 95MHz



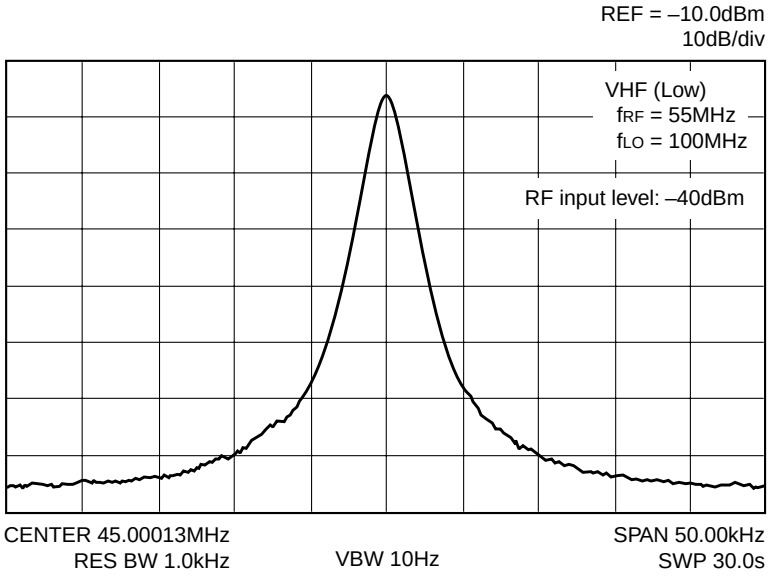


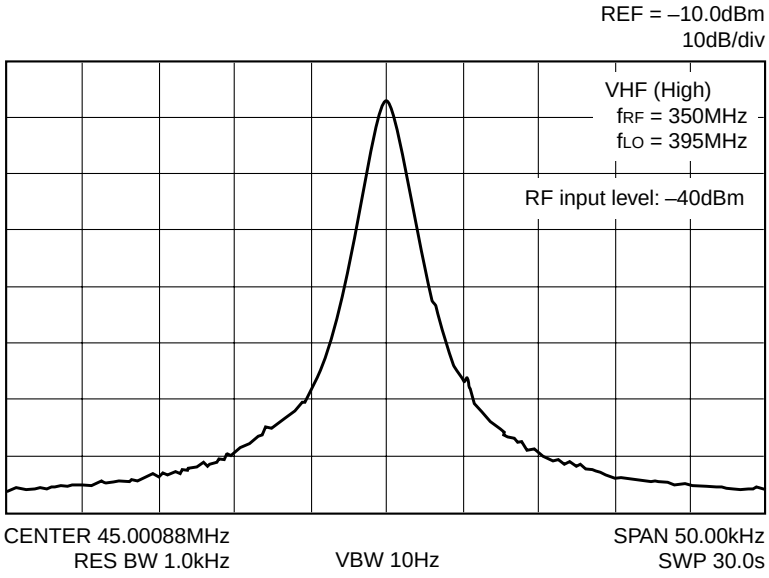
UHF 847MHz → UHF 413MHz

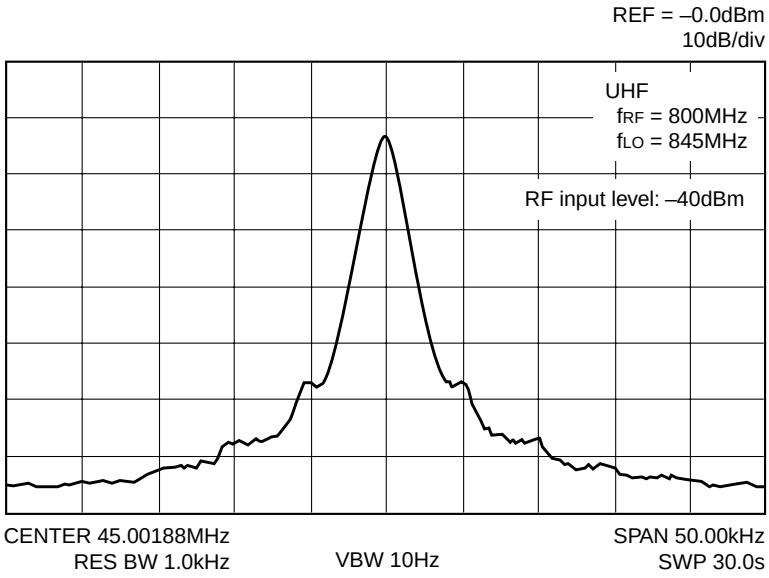




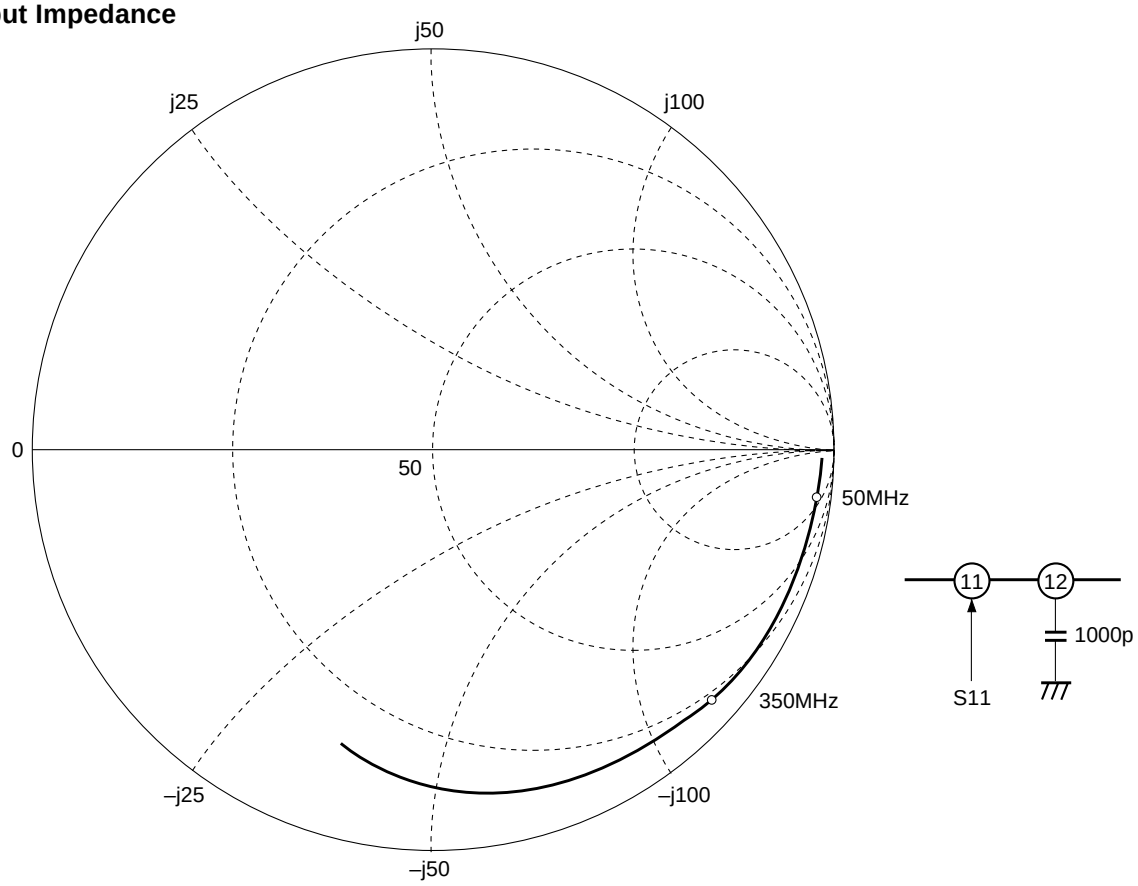
IF output spectrum



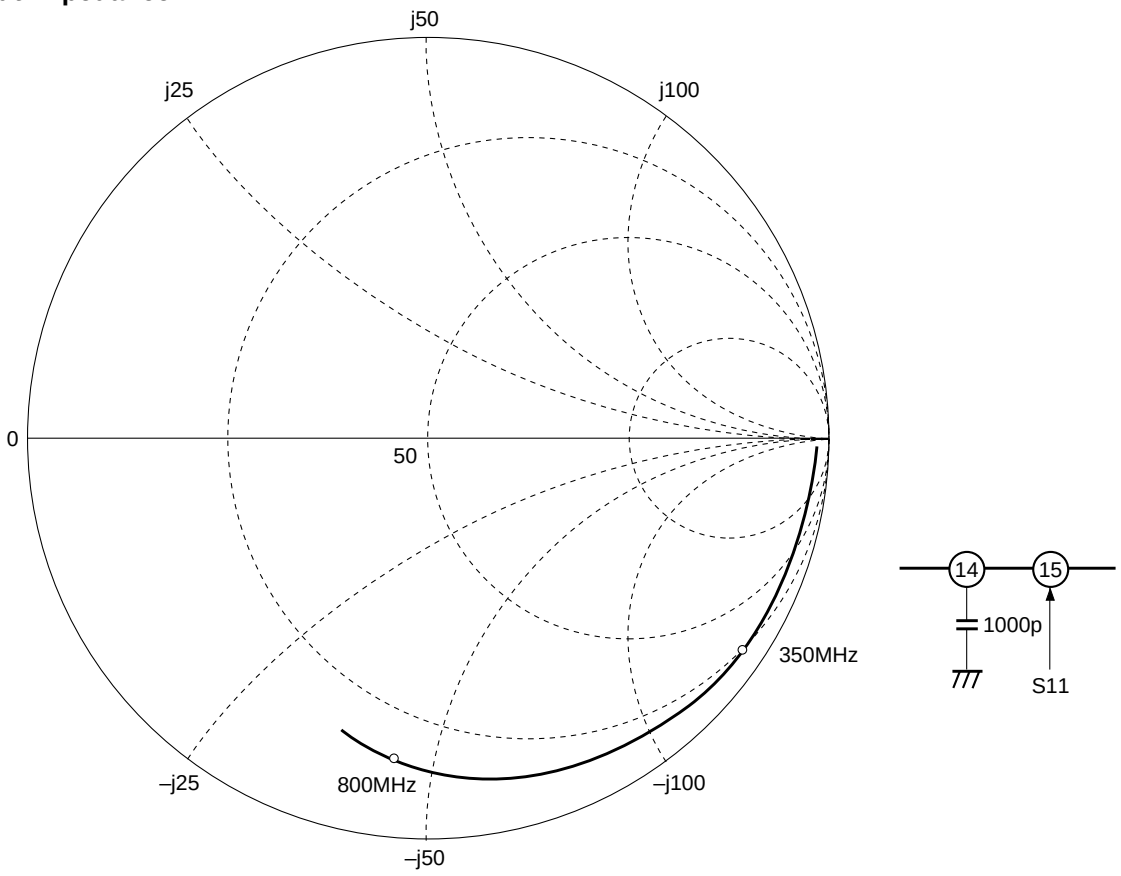




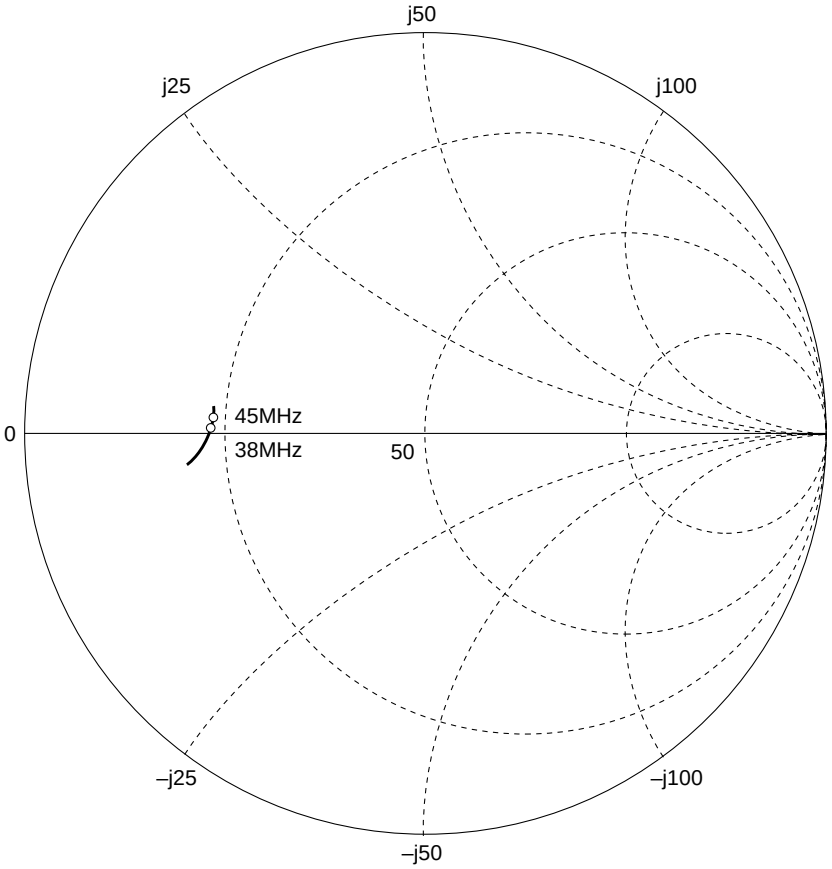
VHF Input Impedance



UHF Input Impedance

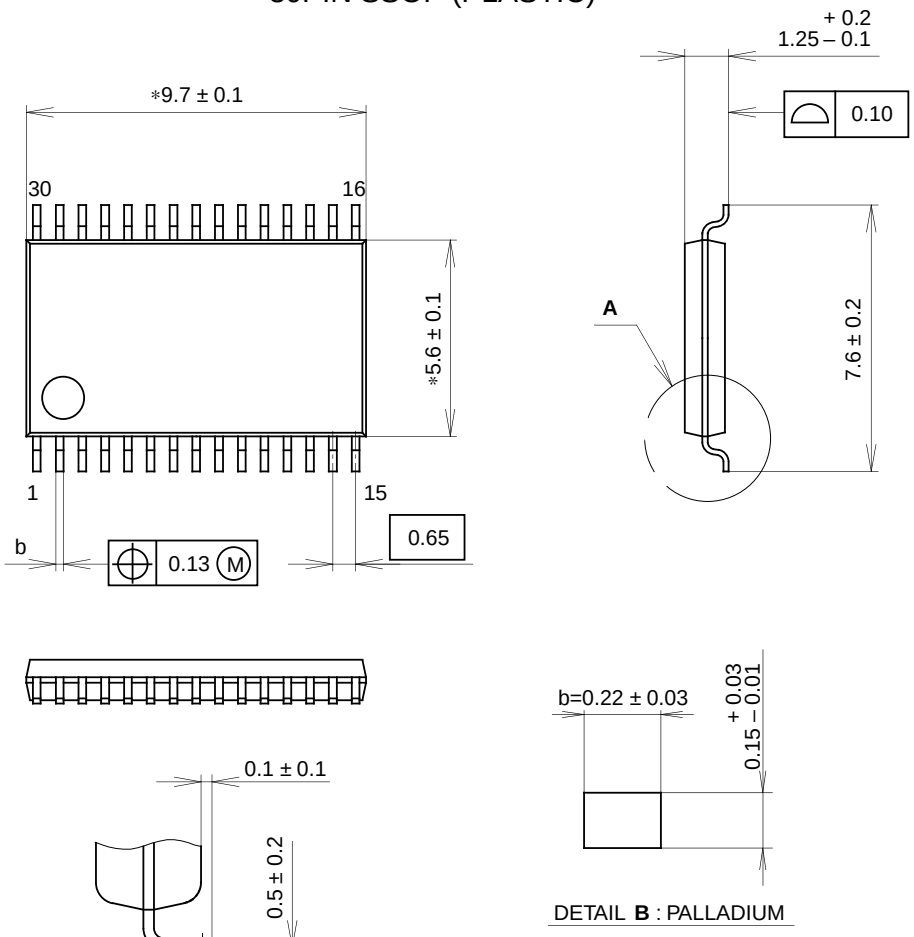


IF Output Impedance



Package Outline Unit: mm

30PIN SSOP (PLASTIC)



DETAIL **B** : PALLADIUM

DETAIL **A**

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	SSOP-30P-L01
EIAJ CODE	P-SSOP30-5.6x9.7-0.65
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.1g