STANDARD
MICROSYSTEMS
CORPORATION

CAM35C44
ADVANCE INFORMATION

Infrared Communications Controller Chip CameraFR

FEATURES

- Mixed Voltage Support
  - Supports 3.3V Operation
  - Supports Mixed Internal 3.3V Operation with 3.3V/5V External Configuration
- Intelligent Auto Power Management
  - Supports Multiple Power Down Modes
- Serial Port
  - High Speed NS16C550A Compatible UART with 16-Byte Send/Receive FIFOs
  - Programmable Baud Rate Generator
- Infrared Port
  - Multi-Protocol Infrared Interface
  - 128-Byte Data FIFO
  - IrDA 1.1 Compliant (up to 4Mbps)
  - Consumer IR
  - SHARP ASK IR
  - Programmed I/O and DMA Options
- Up to 5 General Purpose I/O Pins
- Programmable Multi-Protocol Host Interface
  - ISA-Style 5 Bit Address and 8 Bit Data Bus
  - IOCHRDY and No Wait State Support for Fast IR
  - Non-ISA 8 Bit Multiplexed Address/Data Bus
  - Programmable Read/Write Interface
  - One 8 Bit DMA Channel
  - One Programmable IRQ
  - Chip Select
  - Multihost Interface Support Includes Hitachi and Mitsubishi Microcontrollers
- 24MHz Crystal Oscillator
  - Supports Internal or External Clock Source
- 48 Pin TQFP Package

GENERAL DESCRIPTION

The CAM35C44 with IrDA v1.1 (4Mbps) and Consumer IR support incorporates SMSC's advanced Infrared Communications Controller (IrCC 2.0), a 16C550A-compatible UART, Multiple Host Interface options, flexible Address Decoding and up to five General Purpose I/Os.

The CAM35C44 also features sophisticated power control circuitry to support multiple power down modes, an on-chip 24MHz crystal oscillator, and *12mA* host bus drivers.

The CAM35C44 is particularly suited for 3.3v battery-powered systems.

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ARCHITECTURE

There are six basic architectural components in the CAM35C44: the multihost CPU interface, the IrCC 2.0, a clock generator, configuration registers, power management, and general purpose I/O (

FIGURE **1**).

The multihost CPU interface is capable of supporting several bus configurations; including, a non-multiplexed ISA-style address and data bus, and a multiplexed address/data bus with selectable read/write command options. The multihost CPU interface includes support for Hitachi and Mitsubishi microcontrollers.

The IrCC 2.0 is a multi-protocol serial communications controller that incorporates an ACE 16C550A UART and a Synchronous Communications Engine (SCE). Refer to the SMSC Infrared Communications Controller 2.0 specification for more information.

The clock generator provides connections for a 24MHz crystal or an external clock source. The 24MHz clock directly drives the ACE block. An internal PLL is used for data rates above 115.2Kbps.

Power management in the CAM35C44 includes various power down modes and an infrared wake-up option. The general purpose I/O interface provides generic I/O programming capabilities.

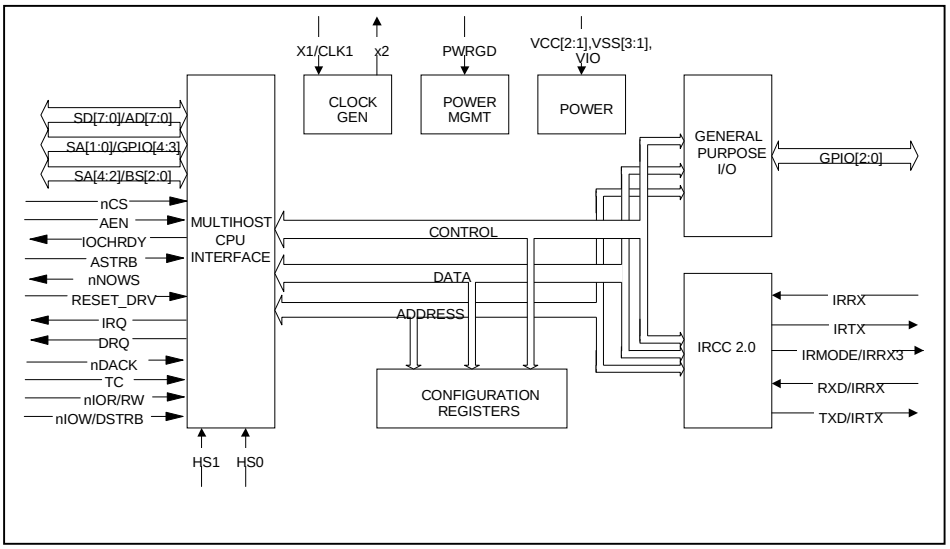


FIGURE 1 - CAM35C44 BLOCK DIAGRAM

PIN CONFIGURATION

The CAM35C44 pin numbers are shown in FIGURE 2. Functional descriptions per pin-group are shown in TABLE 1.

Note: The pin numbers in FIGURE 2 are subject to change.

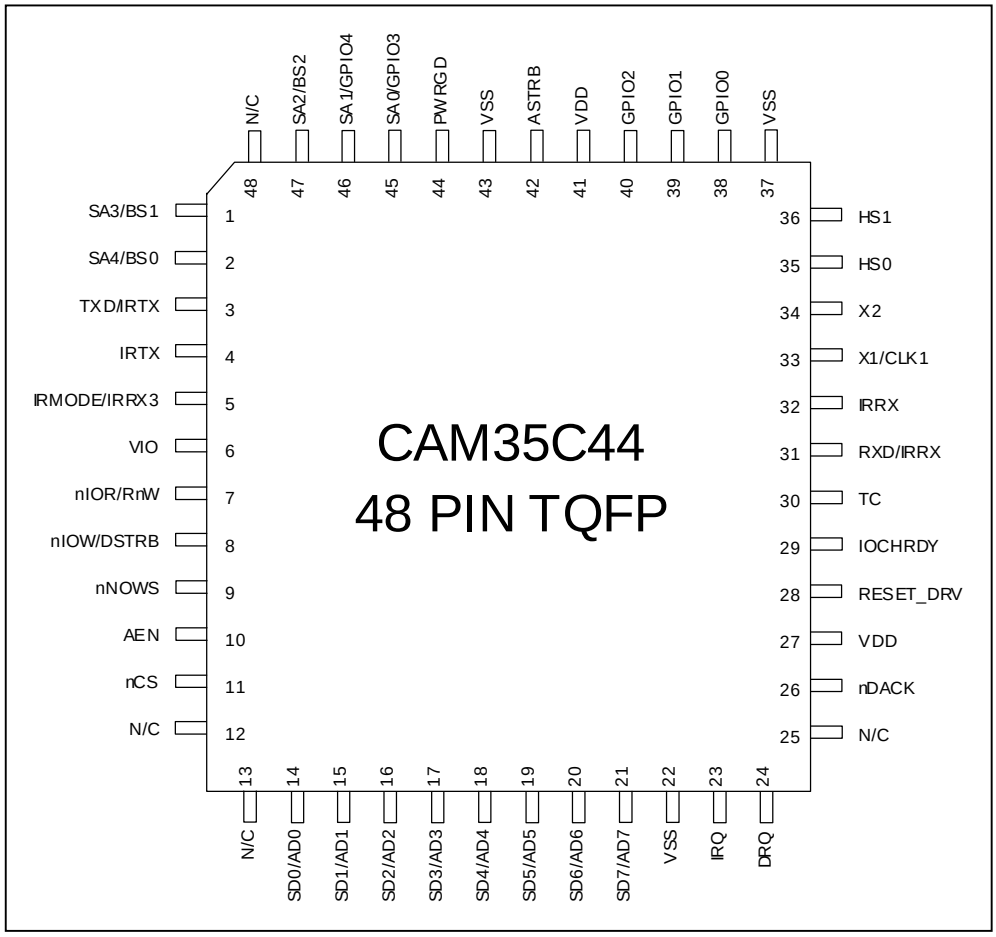


FIGURE 2 - CAM35C44 PIN CONFIGURATION

DESCRIPTION OF PIN FUNCTIONS

TABLE 1 - CAM35C44 PIN FUNCTION DESCRIPTION

NAME	TOTAL PINS	SYMBOL	BUFFER TYPE	DESCRIPTION
PROCESSOR/HOST INTERFACE (25)				
ISA System Data Bus/ Multiplexed Address/Data Bus (Non-ISA)	8	SD[7:0]/AD[7:0]	IO12	This 8 bit bus is used to exchange data with the host. The bus is bi-directional and can be configured as either an ISA system data bus or as a multiplexed address/data bus (TABLE 3). These pins are in a high-impedance state when not in the output mode.
ISA System Address Bus (SA0 - SA1)/ General Purpose I/O (GPIO3 - GPIO4)[4]	2	SA[1:0]/GPIO[4:3]	I/IO12	The ISA system address bus is used to determine the I/O address during read and write cycles. These two ISA system address bus pins are general purpose I/O pins (TABLE 30) when a multiplexed address/data host interface type is selected (TABLE 3).
ISA System Address Bus (SA2 - SA4)/ Memory Block Selects (BS0 - BS2)	3	SA[4:2]/BS[2:0]	I	The ISA system address bus is used to determine the I/O address during read and write cycles. These three ISA system address bus pins are memory block select pins (TABLE 10) when a multiplexed address/data host interface type is selected (TABLE 3).
Chip Select	1	nCS	I	The active low chip select input is a 32-byte address block decoder when the ISA host interface type is selected and a 256-byte page decoder when a multiplexed address/data host interface type is selected (TABLE 3).

NAME	TOTAL PINS	SYMBOL	BUFFER TYPE	DESCRIPTION
Address Enable	1	AEN	I	The active high Address Enable pin indicates DMA operations on the host data bus. AEN must be inactive to access the CAM35C44 registers and active during DMA operations regardless of the selected host interface type.
ISA I/O Channel Ready	1	IOCHRDY	OD12	IOCHRDY is pulled low to extend ISA I/O read/write commands. Only SCE-driven functions in the IrCC 2.0 can be enabled to use IOCHRDY.
Multiplex Mode Address Strobe	1	ASTRB	I	ASTRB is used to internally latch I/O addresses during read/write cycles when a multiplexed address/data host interface type is selected (TABLE 3).
No Wait State	1	nNOWS	OD12	nNOWS can be enabled to be activated by IrCC 2.0 SCE-driven functions to indicate that an access cycle shorter than the standard ISA I/O cycle can be executed.
ISA Reset Drive	1	RESET_DRV	IS	The RESET_DRV pin is active high and is used to reset the CAM35C44 as described in the appropriate sections in this document. The configuration registers are not affected by this pin except where noted (TABLE 13). The RESET_DRV pin must be valid for 500ns minimum.
IRQ	1	IRQ	OD12	The IRQ pin is forced active when an interrupt is asserted. IRQ goes inactive as soon as the source of the interrupt has been cleared. The active IRQ pin-state is determined by the IRQ_LEV bit in CR00 (see page 22).

NAME	TOTAL PINS	SYMBOL	BUFFER TYPE	DESCRIPTION
DMA Request	1	DRQ	O12	The DRQ pin is forced active by the CAM35C44 when byte transfers to the host using DMA are required. DRQ goes inactive when the transfer has been completed. The active DRQ pin-state is determined by the DRQ_LEV bit in CR01 (see page 22).
DMA Acknowledge	1	DACK	I	The DACK pin is forced active by the host DMA controller to acknowledge CAM35C44 transfer requests. DACK goes inactive following the transfer command. The active DACK pin-state is determined by the DAC_LEV bit in CR01 (see page 23).
Terminal Count	1	TC	I	TC indicates that a DMA transfer is complete. TC is only acknowledged when DACK is active.
ISA I/O Read/ Non-ISA Read/Write Control	1	nIOR/RnW	I	The active low nIOR input is issued by the host to execute I/O read commands when an ISA read/write-styled host interface type is selected (TABLE 3). The RnW input is used to determine the I/O command type when a non-ISA read/write-styled host interface type is selected.
ISA I/O Write/ Non-ISA R/W Data Strobe	1	nIOW/DSTRB	I	The active low nIOW input is issued by the host to execute I/O write commands when an ISA read/write-styled host interface type is selected (TABLE 3). The DSTRB input is used to execute the I/O command when a non-ISA read/write-styled host interface type is selected (FIGURE 5).
MISCELLANEOUS (12)				

NAME	TOTAL PINS	SYMBOL	BUFFER TYPE	DESCRIPTION
Clock Input (24MHz CMOS Clock/Crystal)	1	X1/CLK1	ICLK	X1/CLK is the input for either a 24MHz clock crystal or 24MHz crystal oscillator source (see section CLOCK GENERATOR on page 12)
Crystal Driver	1	X2	OCLK	X2 is the 24MHz crystal driver and should be left unconnected if an external clock source is used.
Host Interface Select	2	HS[1:0]	IP	The Host Interface Select bits determine the host interface type. These bits are static controls and must remain stable during device operation (see section MULTIHOST CPU INTERFACE on page 13).
General Purpose I/O (GPIO0 - GPIO2)[4]	3	GPIO[2:0]	IO12	The general purpose I/O pins provide a simple programmable I/O interface. The state of a GPIO pin can be forced to the value contained in the GPIO data register or this register can reflect the logical state of the GPIO pin depending on values programmed in GPIO direction and enable registers (see section GENERAL PURPOSE I/O on page 32).

NAME	TOTAL PINS	SYMBOL	BUFFER TYPE	DESCRIPTION
Power Good	1	PWRGD	IP	This active high input indicates that the positive supply voltage VCC is valid. For normal device operation, PWRGD must be active. When PWRGD is inactive, all device inputs are disconnected and placed into a low power state; all outputs are put into a high-impedance state. *Note: The crystal oscillator pins are unaffected by PWRGD*. The contents of all registers are preserved as long as VCC has a valid value. Output driver current drain when PWRGD is inactive drops to I_{STDBY} - standby current. The PWRGD input has an internal 30µA pull-up.
No Connect	4	N/C	-	No internal connections are made to these pins.
INFRARED INTERFACE (3)				
Infrared Rx[3]	1	IRRX	I	This is the infrared port receiver input pin.
Infrared Tx[1,2]	1	IRTX	O12PD	This is the infrared port transmitter output pin.
Infrared Mode/IRRX3[1]	1	IRMODE/IRRX3	O12/I	This is the infrared port secondary receiver input channel or a transceiver mode control pin, depending on the state of the transceiver module interface type select (TABLE 27).
POWER PINS (6)				
+3.3V Digital Supply Voltage	2	VCC		Positive Supply Voltage
I/O Interface Supply Voltage[1]	1	VIO		Positive I/O Interface Supply Voltage
Ground	3	VSS		Ground Supply

NAME	TOTAL PINS	SYMBOL	BUFFER TYPE	DESCRIPTION
SERIAL PORT INTERFACE (2)				
Receive Serial Data 2/ Infrared Rx[3]	1	RXD/IRRX	I	This is the receiver input pin for the UART COM port or an alternate infrared port receiver input.
Transmit Serial Data 2/Infrared Tx[1,2]	1	TXD/IRTX	O12PD	This is the transmitter output pin for the UART COM port or an alternate infrared port transmitter output.

Note[1] TX and MODE pins drive to VIO level.
Note[2] TX defaults to zero even during POR.
Note[3] RX pins are voltage tolerant to VIO level.
Note[4] All GPIOs are VIO tolerant and back drive protected.

Buffer-Type Summary

The characteristics of the buffer types shown in TABLE 1 are summarized in TABLE 2.

TABLE 2 - CAM35C44 BUFFER-TYPE SUMMARY

BUFFER TYPE	DESCRIPTION
IO12	Input/Output. 12mA sink; 6mA source
O12	Output. 12mA sink; 6mA source
OD12	Open Drain. 12mA sink
O12PD	Output. 12mA sink; 6mA source; 30μA Pulldown @ Tristate
ICLK	Input to Crystal Oscillator Circuit (TTL levels)
OCLK	Output to External Crystal
I	Input TTL Compatible.
IP	Input TTL Compatible with 30μA Pullup
IS	Input with Schmitt Trigger.

CLOCK GENERATOR

An internal 3.3v crystal oscillator or an external oscillator source is required for the CAM35C44 (FIGURE 3). The crystal/clock pins and buffer types are shown in TABLE 1.

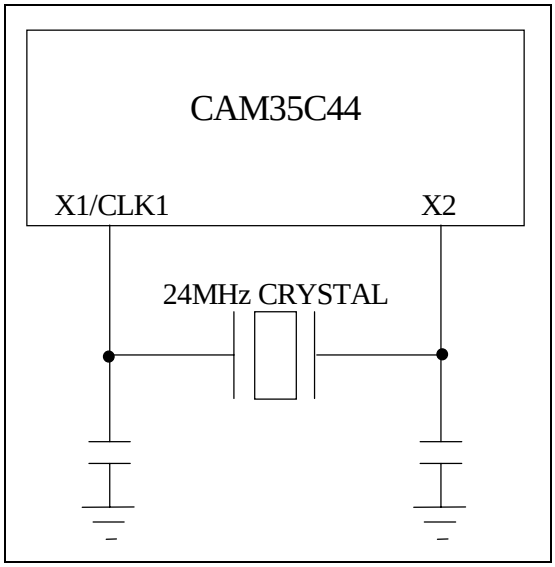
The X1/CLK1 and X2 pins provide an external connection for a parallel resonant 24MHz crystal. Configuration register CR08 bit 5, INT_OSC, must be set to "1" to configure the internal oscillator for this arrangement (see the section CRO8 - Power Control on page 27).

An external CMOS compatible oscillator is required if a 24MHz crystal is not used. In this case INT_OSC must be set to "0".

The X2 pin is the 24MHz crystal driver and should not be used to drive any other device. This pin should be left unconnected if an external clock is used and INT_OSC is "0".

The 24MHz crystal can be used to directly drive the ACE block. This saves power when 115.2Kbps or slower data transfers are required because the PLL and SCE block do not need to be powered. See TABLE 25 and the section CRO8 - Power Control on page 27.

FIGURE 3 - EXAMPLE 24MHz OSCILLATOR CIRCUIT

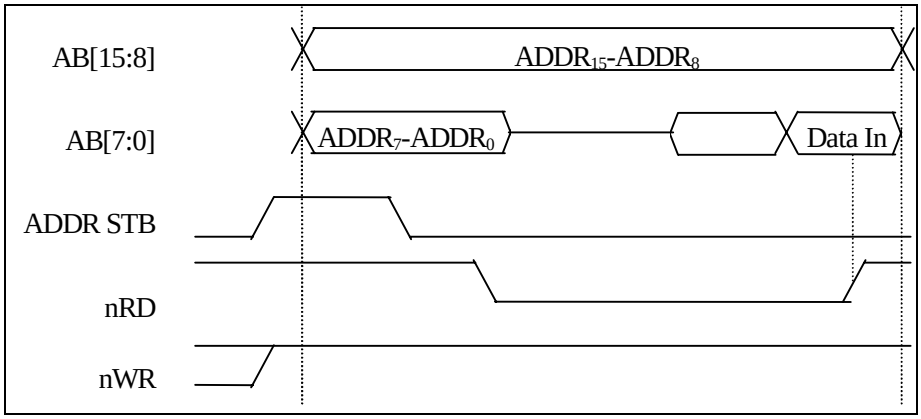


MULTIHOST CPU INTERFACE

The CAM35C44 multihost CPU interface is capable of supporting three bus configurations; including, 1) an ISA-style address and data bus, 2) a multiplexed address/data bus with ISA-style read/write commands like the example shown in (FIGURE 4, and 3) a multiplexed address/data bus with a read/write select and data strobe like the example shown in FIGURE 5.

The CPU interface type as well as the type-specific multiplexing of the processor/host interface pins (TABLE 1) is controlled by the Host Interface Select pins.

FIGURE 4 - NEC UPD781C1X READ CYCLE



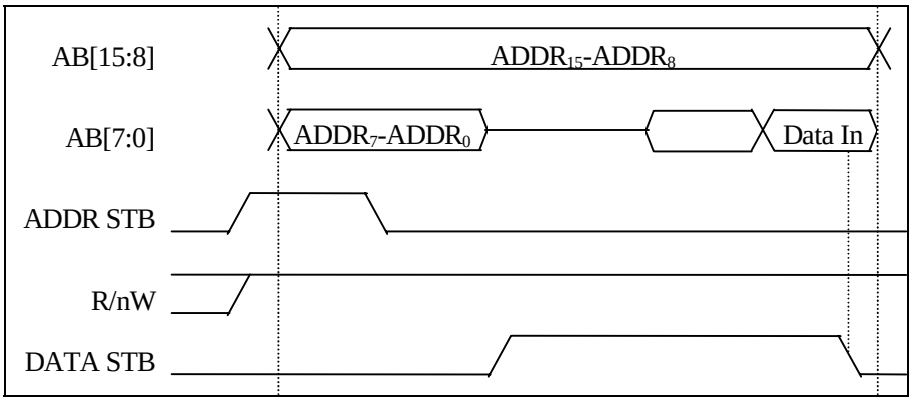


FIGURE 5 - HITACHI HD63P01M1 READ CYCLE

Host Interface Select

The Host Interface Select pins HS[1:0] (TABLE 1) determine the host interface type.

The encoding for these bits is shown in TABLE 3. The Host Interface Select pins are static controls and must remain stable during device operation.

TABLE 3 - HOST INTERFACE ENCODING

HOST INTERFACE SELECT		HOST INTERFACE TYPE
HS1	HS0	
0	0	Reserved
0	1	ISA
1	0	MULTIPLEXED ADDRESS/DATA, Non-ISA Read/Write (FIGURE 5)
1	1	MULTIPLEXED ADDRESS/DATA, ISA Read/Write (FIGURE 4)

Host Interface Pin Multiplexing

Pin multiplexing for the processor/host interface (TABLE 1) is controlled by the Host Interface Select pins HS[1:0].

ISA signals that are not multiplexed, like IOCHRDY and nNOWS, remain operative regardless of the state of the Host Interface Select bits.

The following tables describe processor/host interface multiplexing per pin or per pin group.

System Data Bus

TABLE 4 - SD[7:0] PIN MULTIPLEXING

PIN NAME	MUX CONTROLS		SELECTED FUNCTION
	HS1	HS0	
SD[7:0]	0	0	NOT DEFINED
	0	1	SD[7:0]
	1	0	AD[7:0]
	1	1	AD[7:0]

ISA Address Bus SA0 - SA1

TABLE 5 - SA[1:0] PIN MULTIPLEXING

PIN NAME	MUX CONTROLS		SELECTED FUNCTION
	HS1	HS0	
SA[1:0]	0	0	NOT DEFINED
	0	1	SA[1:0]
	1	0	GPIO[4:3]
	1	1	GPIO[4:3]

ISA Address Bus SA2 - SA4

TABLE 6 - SA[4:2] PIN MULTIPLEXING

PIN NAME	MUX CONTROLS		SELECTED FUNCTION
	HS1	HS0	
SA[4:2]	0	0	NOT DEFINED
	0	1	SA[4:2]
	1	0	BS[2:0]
	1	1	BS[2:0]

ISA nIOR

TABLE 7 - nIOR PIN MULTIPLEXING

PIN NAME	MUX CONTROLS		SELECTED FUNCTION
	HS1	HS0	
nIOR	0	0	NOT DEFINED
	0	1	nIOR
	1	0	R/nW
	1	1	nIOR

ISA nIOW

TABLE 8 - nIOW PIN MULTIPLEXING

PIN NAME	MUX CONTROLS		SELECTED FUNCTION
	HS1	HS0	
nIOW	0	0	NOT DEFINED
	0	1	nIOW
	1	0	DSTRB
	1	1	nIOW

REGISTER ADDRESS MAP

Register addressing in the CAM35C44 is fixed and requires a 32-byte memory block. Typically, register addressing is accomplished with a 5 bit address bus and a 1 bit chip select.

TABLE 9 describes the mapping for the four register banks in the CAM35C44 address space, CONFIGURATION, GPIO, ACE and SCE, that are required for device configuration and run-time control.

The external address pins that are responsible for register addressing will depend on the Host Interface Select bits (see section MULTIHOST CPU INTERFACE on page 13).

TABLE 9 - CAM35C44 REGISTER MAP

8-BYTE ADDRESS BANK	BANK SELECT BITS		ADDRESS RANGE SA[4:0] [1]	REGISTER BANK DECODING
	SA4	SA3		
0	0	0	0x00 - 0x07	CONFIGURATION
1	0	1	0x08 - 0x0F	GPIO
2	1	0	0x10 - 0x17	ACE
3	1	1	0x18 - 0x1F	SCE

Note[1] Address Enable (AEN) must be low to access the CAM35C44 registers regardless of the state of the Host Interface Select bits.

Non-Multiplexed (ISA) Addressing

As shown in TABLE 9 five address bits SA[4:0] and a chip select nCS are required to access the CAM35C44 run-time and configuration registers.

In ISA mode, five bits of the ISA System Address bus SA[4:0] determine the register address, while nCS decodes the 32-byte address block. Note: address block decoding must be done externally.

The Block Select bits BS[2:0] and two of the general purpose I/Os GPIO[4:3] are unavailable in ISA mode.

Multiplexed Addressing

When multiplexed address modes are selected, i.e. HS[1:0] = 02H or 03H (TABLE 3), register addresses are decoded from the Multiplexed Address/Data Bus AD[7:0], the Block Select bits BS[2:0] and the chip select nCS pin.

In the multiplexed addressing modes the 5 low-order bits of the Multiplexed Address/Data Bus AD[4:0] determine the register address while the Block Select bits BS[2:0] qualify the three high-order Multiplexed Address/Data Bus bits, AD[7:5]; i.e., BS[2:0] decodes which of eight 32-byte blocks is selected in the 256-byte page decoded by nCS. Note: page address decoding must be done externally.

For example, TABLE 10 illustrates that if BS[2:0] = 01H, nCS = 0 (active), and AD[7:0] = 20H, the Index Register in the Configuration Bank has been selected.

Two extra GPIO pins GPIO[4:3] are available in the multiplexed address modes.

TABLE 10 - EXAMPLE MULTIPLEXED ADDRESS DECODING

256-BYTE ADDRESS PAGE	32-BYTE ADDRESS BLOCK			MULTIPLEX ADDR/DATA BUS	DESCRIPTION
nCS	BS2	BS1	BS0	AD[7:0]	
1	0	0	1	XXH	No Decode: Invalid Page
0	0	0	1	20H	Decode Configuration Bank Index Register (TABLE 12)
0	0	0	1	00H	No Decode: Invalid Block

CONFIGURATION

The CAM35C44 configuration registers are used to program selectable chip-level device options (TABLE 13).

The configuration registers can only be programmed through the configuration access ports that appear when the chip is placed into the configuration state.

Configuration register programming typically follows this sequence:

1. Enter the Configuration State,
2. Program the Configuration Register(s),
3. Exit the Configuration State.

If enabled, logical devices in the CAM35C44 will operate normally in the configuration state.

Configuration Access Ports

The configuration access ports are the config port, the index port, and the data port (TABLE 11).

The configuration access ports are the only addressable registers in the CAM35C44 configuration bank (TABLE 12).

The index port and the data port are only active in the configuration state.

TABLE 11 - CONFIGURATION ACCESS PORTS

PORT NAME	ADDRESS	DIRECTION
CONFIG PORT	BANK 0, ADDRESS 0[3]	WRITE
INDEX PORT	BANK 0, ADDRESS 0[3]	READ/WRITE[1,2]
DATA PORT	BANK 0, ADDRESS 1[3]	READ/WRITE[1]

Note[1] The INDEX and DATA ports are active only when the CAM35C44 is in the configuration state.

Note[2] The INDEX PORT is only readable in the configuration state.

Note[3] The CAM35C44 register banks are described in section REGISTER ADDRESS MAP on page 16. The register addresses in the CAM35C44 configuration bank are shown in TABLE 12.

Configuration State

Logical devices in the CAM35C44 can operate in the run state and/or the configuration state. After power up the CAM35C44 is in the run state, by default.

To program the configuration registers the configuration state must be explicitly enabled.

Entering the Configuration State

To enter the configuration state, a configuration access key must be written to the config port. The configuration access key is one byte of 55H data.

Once the configuration access key has been written to the config port, the CAM35C44 automatically activates the configuration access ports and enters the configuration state.

Configuration Select Register

The Configuration Select Register (CSR) is located at the index port address and must be initialized with the configuration register index before the register can be accessed using the data port.

The CSR can only be accessed when the CAM35C44 is in the configuration state.

Configuration Register Programming

The CAM35C44 contains ten configuration registers CR00-CR09. After the CAM35C44 enters the configuration state, the configuration registers are programmed by first writing the register index number (00 - 09) to the configuration select register (CSR) and then writing or reading the configuration register contents through the data port.

Configuration register access remains enabled until the configuration state is explicitly exited.

Exiting the Configuration State

To exit the configuration state one byte of AAH data must be written to the config port.

Once AAH has been written to the config port, the CAM35C44 automatically deactivates the configuration access ports and enters the run state. In the run state, configuration register access cannot occur until the configuration state is explicitly re-enabled.

Programming Example

The following Intel 8086 assembly language instructions illustrate CAM35C44 configuration register programming. In this example, the config port is located at address 3F0H.

```
;-----------------------------.
; ENTER CONFIGURATION STATE    |
;-----------------------------'
MOV    DX,3F0H
MOV    AX,055H
OUT    DX,AL
;-----------------------------.
; CONFIGURE REGISTERS CR0-CRx  |
;-----------------------------'
MOV    DX,3F0H
MOV    AL,00H
OUT    DX,AL         ;Point to CR0
MOV    DX,3F1H
MOV    AL,3FH
OUT    DX,AL         ;Update CR0
;
MOV    DX,3F0H
MOV    AL,01H
OUT    DX,AL         ;Point to CR1
MOV    DX,3F1H
MOV    AL,9FH
OUT    DX,AL         ;Update CR1
;
; Repeat for all CRx registers
;
;-----------------------------.
; EXIT CONFIGURATION STATE     |
;-----------------------------'
MOV    DX,3F0H
MOV    AX,AAH
OUT    DX,AL
```

Configuration Registers

Introduction

The configuration registers (TABLE 13) are set to their default values at power up and are not affected by RESET, except where noted in the register descriptions that follow.

Configuration register bits that are not needed in the CAM35C44 are marked RESERVED in the sections below. RESERVED bits cannot be written and return "0" when read.

Configuration Register references are in hex; e.g., CRC0.3 means *Configuration Register* 0xC0, *Bit* 0x03.

Configuration Bank Addressing

The CONFIGURATION register bank is defined as the first eight addresses in the CAM35C44 memory map (see section REGISTER ADDRESS MAP on page 16).

TABLE 12 summarizes the contents of the CONFIGURATION bank. The Index and Data registers access the configuration registers (TABLE 13) as described above.

TABLE 12 - CONFIGURATION REGISTER BANK

ADDRESS	DEFAULT	REGISTER NAME
0x00	0x00	Config/Index Register
0x01	0x00	Data Register
0x02 . . . 0x07	0x00	RESERVED

Description

TABLE 13 - CONFIGURATION REGISTERS

CR INDEX	POR DEFAULT	RESET DEFAULT	REGISTER NAME
0x00	0x00	0x00	IRQ CONTROL
0x01	0x00	0x00	DMA CONTROL
0x02	0x02	n/a	INFRARED OPTION
0x03	0x01	n/a	INFRARED CONTROL B
0x04	0x00	n/a	TEST CONTROL A
0x05	0x00	n/a	*SOFTWARE SELECT A*
0x06	0x00	n/a	*SOFTWARE SELECT B*
0x07	0x03	n/a	IR HALF DUPLEX TIME-OUT
0x08	0x00	0x00	POWER CONTROL
0x09	0x00	n/a	TEST CONTROL B

CR00 - IRQ Control

The IRQ Control register CR00 determines the IRQ pin polarity and enables the configuration register locking feature.

CR00 can only be accessed in the configuration state and only after the CSR has been initialized to 00H. The default value of this register after power up is 00H (TABLE 14).

Bits[7:3, 1] in the IRQ Control register are RESERVED.

TABLE 14 - IRQ CONTROL REGISTER

		D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
CR00	R/W	RESERVED					LOCK	RES	IRQ_LEV	0x00

IRQ_LEV, Bit 0

The IRQ_LEV bit D0 determines the active state of the IRQ output pin (TABLE 1). If IRQ_LEV is "0" (default), the IRQ pin is active low. If IRQ_LEV is "1", the IRQ pin is active high.

LOCK, Bit 2

The LOCK bit D2 selects configuration register locking. "Locked" means configuration registers can be read but cannot be written, except for the IRCC Legacy Controls like the IR HALF DUPLEX TIME-OUT that can be written through the SCE Registers and appear in the chip-level configuration registers regardless of the state of the LOCK bit.

If LOCK is "0" (default), the configuration registers are unlocked. If LOCK is "1", the configuration registers are locked.

Note: once the LOCK bit is set to "1" the configuration registers are permanently locked. The LOCK bit can only be reset to "0" by a hard-reset or a power-on-reset; i.e., the configuration registers cannot be changed until either a hard-reset or power-on-reset occur.

CR01 - DMA Control

The DMA Control register CR01 determines the DRQ and DACK pin polarity (TABLE 1).

CR01 can only be accessed in the configuration state and only after the CSR has been initialized to 01H. The default value of this register after power up is 00H (TABLE 15).

Bits[7:2] in the DMA Control register are RESERVED.

TABLE 15 - DMA CONTROL REGISTER (CR01)

		D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
CR01	R/W	RESERVED						DAC_LEV	DREQ_LEV	0x00

DRQ_LEV, Bit 0

The DRQ_LEV bit D0 determines the active state of the DMA Request (DRQ) output pin (TABLE 1).

If DRQ_LEV is “0” (default), the DRQ pin is active low. If DRQ_LEV is “1”, the DRQ pin is active high.

DAC_LEV, Bit 1

The DAC_LEV bit D1 determines the active state of the DMA Acknowledge (DACK) input pin (TABLE 1).

If DAC_LEV is “0” (default), the DACK pin is active low. If DAC_LEV is “1”, the DACK pin is active high.

CR02 - Infrared Option

The Infrared Option register CR02 determines the infrared port transmit and receive pin polarity, the port duplex mode, and the infrared port protocol.

The controls in the Infrared Option register are also duplicated in the IrCC 2.0 SCE Configuration Register A. These controls are arranged such that the last write from either source determines the current control state and is visible in both registers.

CR02 can only be accessed in the configuration state and only after the CSR has been initialized to 02H. The default value of this register after power up is 02H (TABLE 16).

Bits[7:6] in the Infrared Option register are RESERVED.

TABLE 16 - INFRARED OPTION REGISTER

		D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
CR02	R/W	RES.		IR_ MODE2	IR_ MODE1	IR_ MODE0	HALF DUPLEX	XMT_ POL	RCV_ POL	0x02

RCV_POL, Bit 0

The RCV_POL bit D0 defines the active state for the infrared port receive pins.

If RCV_POL is “0” (default), the IRRX pin is active low. If RCV_POL is “1”, the IRRX pin is active high.

The RCV_POL pin has no affect when the port is configured as a 16C550A UART (see section IR_MODE, Bits 3 - 5 on page 24).

XMT_POL, Bit 1

The XMT_POL bit D1 defines the active state for the infrared port transmit pins.

If XMT_POL is “0”, the IRTX pin is active low. If XMT_POL is “1” (default), the IRTX pin is active high.

The XMT_POL pin has no affect when the port is configured as a 16C550A UART (see section IR_MODE, Bits 3 - 5 on page 24).

HALF DUPLEX, Bit 2

When the HALF DUPLEX bit D2 is "0" (default), the 16C550A UART in the IrCC 2.0 is in full duplex mode. Full duplex mode has no effect on the IrCC 2.0 SCE.

When the HALF DUPLEX bit is "1", the IrCC 2.0 is in half duplex mode. Half duplex mode is typically required for all infrared transactions.

In half duplex mode, the IR Half Duplex Time-Out will apply to IrCC 2.0 transmit/receive direction mode changes (see section CR07 - IR Half Duplex Time-Out on page 26). The IR Half Duplex Time-Out does not apply to full duplex mode.

IR_MODE, Bits 3 - 5

The IR_MODE bits D3 - D5 select the active IrCC 2.0 encoder/decoder. The default is COM (TABLE 17).

The IR_MODE bits are equivalent to the three low-order Block Control bits in the IrCC 2.0 SCE Configuration Register A.

TABLE 17 - CAM35C44 INFRARED PROTOCOL OPTIONS

IR_MODE[2:0]			MODE	DESCRIPTION
D5	D4	D3		
0	0	0	COM	16C550A UART (Default)
0	0	1	IrDA SIR-A	Up to 115.2Kbps, Variable 3/16ths Pulse
0	1	0	ASK IR	500KHz Carrier, Amplitude Shift Keyed IR
0	1	1	IrDA SIR-B	Up to 115.2Kbps, Fixed 1.6μs Pulse
1	0	0	IrDA HDLC	0.576Mbps and 1.152Mbps
1	0	1	IrDA 4PPM	4Mbps
1	1	0	CONSUMER	Consumer (TV Remote) IR
1	1	1	RAW	Direct IR Diode Control

CR03 - Infrared Control B

The Infrared Control B register CR03 configures the infrared interface and COM port clock select.

CR03 can only be accessed in the configuration state and only after the CSR has been initialized to 03H. The default value of this register after power up is 01H (TABLE 18).

Bits[7:5,3:1] in the Infrared Control B register are RESERVED.

TABLE 18 - IR CONTROL B REGISTER

		D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
CR03	R/W	RESERVED			MIDI	RESERVED			HPMODE	0x01

HPMODE, Bit 0

The HPMODE bit D0 is used to configure the transceiver type in the CAM35C44 infrared interface (see FIGURE 6). When HPMODE is "1" (default), the IRMODE/IRRX3 pin is configured as an input (IRRX3) to support transceiver types that require two receive channels. When HPMODE is "0", the IRMODE/IRRX3 pin is configured as an output (IRMODE) to support transceiver types that require one receive channel and a mode control pin.

MIDI, Bit 4

The MIDI bit D4 is the 16C550A UART clock divider select. When MIDI is "0" (default), the 16C550A clock divider is configured to generate the standard UART data rates up to 115.2Kbaud.

When MIDI is "1", the 16C550A clock divider is configured to generate UART data rates that are compatible with the 31.25Kbaud (±1%) Musical Instrument Digital Interface standard.

CR04 - Test Control A

The Test Control A register CR04 enables user-level serial loopback testing and SMSC internal test modes.

CR04 can only be accessed in the configuration state and only after the CSR has been initialized to 04H. The default value of this register after power up is 00H (TABLE 19).

TABLE 19 - TEST CONTROL A REGISTER

		D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
CR04	R/W	IR_TEST[6:0]							IR_LB	0x00

IR_LB, Bit 0

The IR_LB bit D0 enables serial loopback testing, independent of the internal IrCC 2.0 loopback controls. When IR_LB is "1" the transmit output is internally connected to the receiver input. When IR_LB is "0" (default), the transmit output is not connected to the receive input and loopback testing is disabled.

IR_TEST[6:0], Bits 1 - 7

The IR_TEST[6:0] bits D1 - D7 control SMSC internal test modes.

The IR_TEST[6:0] bits are "0" (default) for normal operation.

When any of the IR_TEST[6:0] bits are "1", an SMSC internal test mode is activated. Note: SMSC internal test modes are reserved for SMSC use, only. Activating SMSC internal test modes may produce undesired results.

CR05 - Software Select A

The Software Select A register CR05 is directly connected to the read-only IrCC 2.0 Software Select A register in SCE Register Block Three. Writing to CR05 is the only way to revise the contents of the Software Select A register. CR05 can only be accessed in the configuration state and only after the CSR has been initialized to 05H. The default value of this register after power up is 00H (TABLE 20).

TABLE 20 - SOFTWARE SELECT A REGISTER

		D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
CR05	R/W	Software Select A								0x00

CR06 - Software Select B

The Software Select B register CR06 is directly connected to the read-only IrCC 2.0 Software Select B register in SCE Register Block Three. Writing to CR06 is the only way to revise the contents of the Software Select B register. CR06 can only be accessed in the configuration state and only after the CSR has been initialized to 06H. The default value of this register after power up is 00H (TABLE 21).

TABLE 21 - SOFTWARE SELECT B REGISTER

		D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
CR06	R/W	Software Select B								0x00

CR07 - IR Half Duplex Time-Out

CR07 is the IR Half Duplex Time-Out register (TABLE 22).

If the Half Duplex option is selected (see section HALF DUPLEX, Bit 2 on page 24), the IR half duplex time-out constrains the timing of transmit/receive direction mode changes in the IrCC 2.0. The IR half duplex time-out is started as each IR message data bit is transferred and prevents direction mode changes until the time-out expires. The timer is restarted whenever new data is transferred in the current direction mode.

For example, in an SIR mode if data is loaded into the transmit buffer while a character is being received, the transmission will not start until the last bit has been received and the time-out expires. If the start bit of another character is received during this time-out, the timer is restarted after the new character is received.

The IRCC block in the CAM35C44 also includes an 8 bit IR half duplex time-out register, like CR07, in SCE Register Block 5. These two registers behave like the other IRCC legacy controls where either source uniformly updates the value of both registers when either register is explicitly written using IOW or following a device-level POR. IRCC software resets do not affect these registers.

The IR half duplex time-out is programmable from 0 to 25.5ms in 100µs increments, as follows:

IR HALF DUPLEX TIME-OUT = (CR07) x 100µs

TABLE 22 - IR HALF DUPLEX TIME-OUT REGISTER

		D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
CR07	R/W	IR HALF DUPLEX TIME-OUT								0x03

CR08 - Power Control

The Power Control register CR08 contains the power control enables to select the various CAM35C44 power states (TABLE 25) and also includes a bit to configure the system clock source. CR08 can only be accessed in the configuration state and only after the CSR has been initialized to 08H. The default value of this register after power up is 00H (TABLE 23). Bits[7:6] in the Power Control register are RESERVED.

TABLE 23 - POWER CONTROL REGISTER

		D7	D6	D5	D4	D3	D2	D1	D0	Default
CR08	R/W	RES		INT_ OSC	AUTO_ PWR	SCE_ ON	PLL_ ON	ACE_ON	OSC_ON	0x00

OSC_ON, Bit 0

The OSC_ON bit D0 determines the power state for CAM35C44 clock generator, independent of the clock source (see section INT_OSC, Bit 5 on page 28). When OSC_ON is “0” (default), the clock generator is powered down. When OSC_ON is “1”, the clock generator is running.

ACE_ON, Bit 1

The ACE_ON bit D1 along with the AUTO_PWR bit D4 determines the power state for IrCC 2.0 ACE UART. When ACE_ON is “0” (default), the UART is powered down, regardless of the state of AUTO_PWR; i.e., when ACE_ON is “0”, UART wake-up events are disabled (see section AUTO_PWR, Bit 4). When ACE_ON is “1”, the UART is active.

PLL_ON, Bit 2

The PLL_ON bit D2 determines the power state for the PLL clock multiplier. The PLL is required for IrDA transfers above 115.2Kbps. When PLL_ON is “0” (default), the PLL is powered down. When PLL_ON is “1”, the PLL is running.

SCE_ON, Bit 3

The SCE_ON bit D3 determines the power state for the IrCC 2.0 SCE. The SCE is required for IrDA transfers above 115.2Kbps and for all Consumer IR transactions. When SCE_ON is “0” (default), the SCE is powered down. When SCE_ON is “1”, the SCE is active.

AUTO_PWR, Bit 4

The AUTO_PWR bit D4 along with the ACE_ON bit D1 selects the auto power down state of the ACE UART (TABLE 24). When AUTO_PWR is “0” (default), the ACE auto power down state is disabled and the ACE UART power state is controlled solely by the ACE_ON bit (see section ACE_ON, Bit 1 on page 27). Note: If the ACE auto power state is disabled the ring indicator (nRI) and the RXD power-on wake-up events are disabled. When AUTO_PWR is “1” and ACE_ON is “1”, the ACE auto power down state is enabled and the following power management events are possible.

Transmitter Auto Power Down

The UART transmitter is powered down from the auto power down state when the transmit buffer and transmit shift registers are empty.

Receiver Auto Power Down

The UART receiver is powered down from the auto power state when the receive FIFO is empty and the receiver is waiting for a start bit.

Ring Indicator Auto Power Down

When the UART is powered down from the auto power state, a Ring Indicator interrupt can occur on active transitions of the Ring Indicator input nRI.

Exit Auto Power Down

The transmitter exits the auto power down state on a write to the transmit buffer. The receiver exits the auto power down state when the receiver input RXD changes state.

TABLE 24 - ACE UART POWER STATES

ACE_ON (D1)	AUTO_PWR (D4)	DESCRIPTION
0	X	ACE POWER OFF
1	0	ACE POWER ON
1	1	ACE AUTO POWER DOWN

INT_OSC, Bit 5

The INT_ OSC bit D5 selects the clock source for the CAM35C44 clock generator (see section CLOCK GENERATOR on page 12). When INT_OSC is “0” (default), the clock generator is driven by an external clock source. When INT_OSC is “1”, the clock generator is driven by the internal crystal oscillator.

TABLE 25 - EXAMPLE POWER CONSUMPTION VS. POWER CONTROL ENABLES

CR08[3:0]				*POWER CONSUMPTION (I_{CC})*		CLOCK GENERATOR	ACE BLOCK[1]	PLL	SCE BLOCK[2]
D3	D2	D1	D0	*TYP*	*MAX*				
0	0	0	0	*1μA[4] 2μA[5] (Note[3])*	*2.5μA[4] 5μA[5] (Note[3])*	OFF	OFF	OFF	OFF
0	0	0	1	*500μA*	*1mA*	RUNNING	OFF	OFF	OFF
0	0	1	1	*1mA*	*2mA*	RUNNING	ON	OFF	OFF
0	1	1	1	*1.6mA*	*3mA*	RUNNING	ON	*RUNNING*	OFF
1	1	1	1	*6mA*	*8mA*	RUNNING	ON	*RUNNING*	ON

Note[1]: The 24MHz crystal oscillator directly driving the ACE block enables data transfers up to 115.2Kbps.
Note[2]: The PLL driving the SCE block enables data transfers up to 4Mbps.
Note[3]: PWRGD does not stop the crystal from oscillating if OSC_ON, D0 in configuration register CR08, is "1".
Note[4]: PWRGD is "0".
Note[5]: PWRGD is "1".

CR09 - Test Control B

The IR_TEST[14:7] bits D0 - D7 in the Test Control B register enable SMSC internal test modes. CR09 can only be accessed in the configuration state and only after the CSR has been initialized to 09H. The default value of this register after power up is 00H (TABLE 26). The IR_TEST[14:7] bits are "0" (default) for normal operation. When any of the IR_TEST[14:7] bits are "1", an SMSC internal test mode is activated. Note: SMSC internal test modes are reserved for SMSC use, only. Activating SMSC internal test modes may produce undesired results.

TABLE 26 - TEST CONTROL B REGISTER

		D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
CR09	R/W	IR_TEST[14:7]								0x00

INFRARED INTERFACE

The CAM35C44 infrared interface can support various infrared protocols and transceiver configurations. For more information consult the SMSC Infrared Communication Controller (IrCC 2.0) specification.

IrDA SIR/FIR

IrDA SIR (v1.0) specifies asynchronous serial communication at baud rates up to 115.2kbps. Each byte is sent serially LSB first beginning with a zero value start bit. A zero is signaled by sending a single infrared pulse at the beginning of the serial bit time. A one is signaled by the absence of an infrared pulse during the bit time. IrDA FIR (v1.1) includes IrDA v1.0 SIR and additionally specifies synchronous serial communications at data rates up to 4Mbps. Data is transferred LSB first in packets that can be up to 2048 bits in length. IrDA v1.1 includes .576Mbps and 1.152Mbps data rates using an encoding scheme that is similar to SIR. The 4Mbps data rate uses a pulse position modulation (PPM) technique.

ASKIR

The ASKIR infrared protocol allows asynchronous amplitude shift keyed serial communication at baud rates up to 19.2kbps. Each byte is sent serially LSB first beginning with a zero value start bit. A zero is signaled by sending a 500kHz carrier waveform for the duration of the serial bit time. A one is signaled by the absence of carrier during the bit time.

Consumer IR

The CAM35C44 Consumer IR interface is a general-purpose synchronous amplitude shift keyed encoder/decoder with programmable carrier and bit-cell rates that can emulate many popular TV Remote encoding formats; including, 38kHz PPM, PWM and RC-5. Each bit is sent serially LSB first. The carrier frequency is programmable from 1.6MHz to 6.25kHz. The bit-cell rate range is 100kHz to 390Hz.

Hardware Interface

The CAM35C44 IR hardware interface is shown in FIGURE 6. This interface supports two types of IR transceiver modules. One interface type requires a mode pin (IR Mode) to select the data rate, while the other interface type requires a second Rx data pin (IRRX3). The transceiver interface type is selected with the HPMODE bit D0 in CR03 as shown in TABLE 27 (see section HPMODE, Bit 0 on page 25).

TABLE 27 - TRANSCEIVER MODULE INTERFACE TYPE SELECT

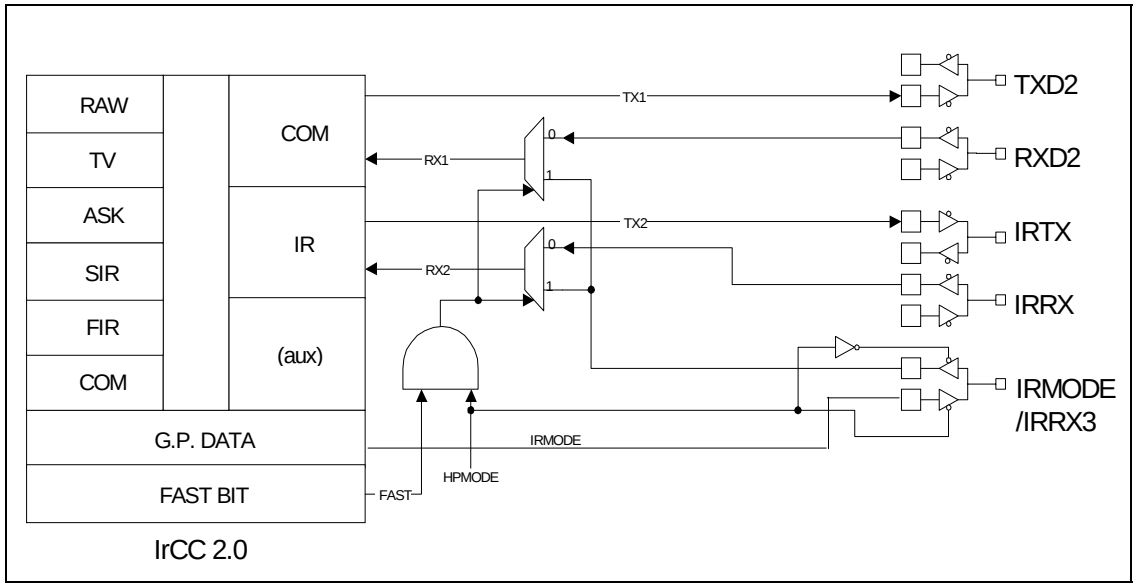
HP MODE (CR03.0)	FUNCTION
0	IR Mode
1	IRRX3

The FAST bit in FIGURE 6 is used to select between an SIR mode and FIR mode receiver, regardless of the transceiver type. If FAST is "1", the FIR mode receiver is selected; if FAST is "0", the SIR mode receiver is selected (TABLE 28).

TABLE 28 - IR RX DATA PIN SELECTION

CONTROL SIGNALS		INPUTS	
FAST	**HPMODE**	**RX1**	**RX2**
0	X	RXD2	IRRX2
X	0	RXD2	IRRX2
1	1	IR MODE/IRRX3	IR MODE/IRRX3

FIGURE 6 - IR INTERFACE BLOCK DIAGRAM



GENERAL PURPOSE I/O

Introduction

The CAM35C44 can support up to 5 general purpose I/O pins, GPIO[4:0] (TABLE 1). The number of available general purpose I/O pins depends upon the Host Interface Select bits (see the section MULTIHOST CPU INTERFACE on page 13). The general purpose I/O pins are controlled by the GPIO registers contained in Bank 1 of the CAM35C44 memory map (see the section REGISTER ADDRESS MAP on page 16). TABLE 29 summarizes the contents of the GPIO register bank.

TABLE 29 - GPIO REGISTER BANK MAP

BANK	ADDRESS	DEFAULT	REGISTER NAME
BANK 1 (GPIO)	0x00	0x00	GPIOA Enable Register
	0x01	0x00	RESERVED
	0x02	0x00	GPIOA Data Register
	0x03	0x00	RESERVED
	0x04	0x00	GPIOA Direction Register
	0x05	0x00	RESERVED
	0x06	0x00	RESERVED
	0x07	0x00	RESERVED

Description

The state of a GPIO pin can be forced to the value contained its data register, depending on the state of its direction and enable bits. For example, when a GPIO pin is configured as an output the data register contains a “1” and the enable bit is active, the GPIO pin will be driven high. When a GPIO pin is configured as an input and the enable is active, the value in the data register will reflect the state of the pin. When a GPIO pin is configured as an input and the enable is inactive, state changes at the pin are not reflected in the data register. When a GPIO pin is configured as an output and the enable is inactive, changes in the data register do not affect the pin. TABLE 12 summarizes the GPIO pin behavior described above. FIGURE 7 illustrates GPIO pin functionality. Note: FIGURE 7 is for illustration purposes only and is not intended to suggest specific implementation details.

TABLE 30 - GPIO FUNCTIONAL DESCRIPTION

GPx ENABLE [1]	GPx OUT [2]	GPIOx PIN DIRECTION	I/O COMMAND	GPx DATA [3]	DESCRIPTION
1	1	OUTPUT	READ	CURRENT VALUE	Output pin is active (driven), reads return last write.
			WRITE	NEW VALUE	Output pin is active (driven), writes update data register.
1	0	INPUT	READ	CURRENT VALUE	Input pin is active, reads return the current state of the pin.
			WRITE	NO EFFECT	Input pin is active, writes have no effect.
0	1	INPUT	READ	LAST VALUE	Output pin is floating, reads return last active state.
			WRITE	NEW VALUE	Output pin is floating, writes update data register.
0	0	INPUT	READ	LAST VALUE	Input pin is disabled, reads return last enabled read state.
			WRITE	NO EFFECT	Input pin is disabled, writes have no effect.

Note[1] This represents a GPIO Enable register bit. The GPIO Enable register is GP00 (see section GPIOA Enable Register on page 34).

Note[2] This represents a GPIO Direction register bit. The GPIO Direction register is GP04 (see section GPIOA Direction Register on page 35).

Note[3] This represents a GPIO Data register bit. The GPIO Data register is GP02 (see section GPIOA Data Register on page 35).

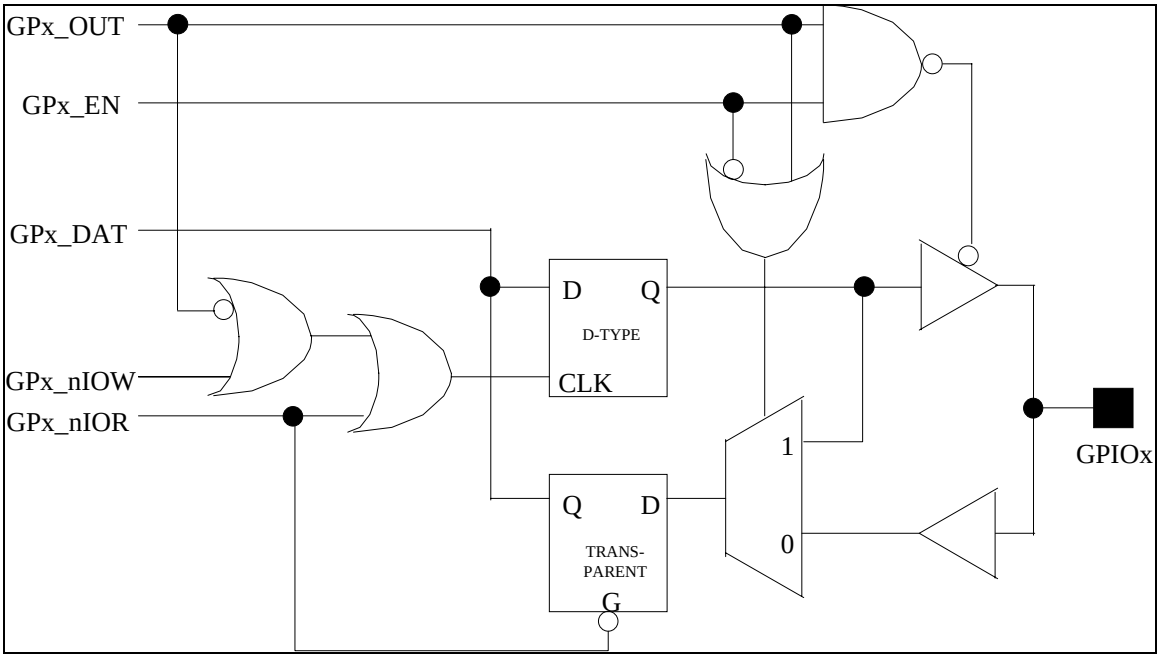


FIGURE 7 - GENERAL PURPOSE I/O BLOCK DIAGRAM

Note: This figure is for illustration purposes only and is not intended to suggest specific implementation details)

Registers

GPIOA Enable Register

The GPIOA Enable register GP00 contains the enable bits for the five general purpose I/O pins (TABLE 31). When any of the GPx_EN bits are "1", the associated general purpose I/O pin is enabled. When any of the GPx_EN bits are "0", the associated general purpose I/O pin is disabled. The affects of the GPx_EN bits are summarized in TABLE 30. GP00 can be accessed both in the configuration state and the run state (see section REGISTER ADDRESS MAP on page 16 and TABLE 29). The default value of the GPIOA Enable register after power up is 00H. Bits[7:5] in the GPIOA Enable register are RESERVED.

TABLE 31 - GPIOA ENABLE REGISTER

		D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
GP00	R/W	RESERVED			GP4_EN	GP3_EN	GP2_EN	GP1_EN	GP0_EN	0x00

GPIOA Data Register

The GPIOA Data register GP02 contains the data bits for the five general purpose I/O pins (TABLE 32). The state of a GPIO pin can be forced to the value contained its data register, or the value in the data register can reflect the state of the pin, depending on the state of the direction and enable bits. The affects of the GPx_DAT bits are summarized in TABLE 30. GP02 can be accessed both in the configuration state and the run state (see section REGISTER ADDRESS MAP on page 16 and TABLE 29). The default value of the GPIOA Data register after power up is 00H. Bits[7:5] in the GPIOA Data register are RESERVED.

TABLE 32 - GPIOA DATA REGISTER

		D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
GP02	R/W	RESERVED			GP4_DAT	GP3_DAT	GP2_DAT	GP1_DAT	GP0_DAT	0x00

GPIOA Direction Register

The GPIOA Direction register GP04 contains the direction bits for the five general purpose I/O pins (TABLE 33). The direction of a GPIO pin depends upon the state of the direction bit and the enable bit, but typically if the direction bit is “1” the GPIO pin is an output; if the direction bit is “0” the GPIO pin is an input. The affects of the GPx_OUT bits are summarized in TABLE 33. GP04 can be accessed both in the configuration state and the run state (see section REGISTER ADDRESS MAP on page 16 and TABLE 29). The default value of the GPIOA Direction register after power up is 00H. Bits[7:5] in the GPIOA Direction register are RESERVED.

TABLE 33 - GPIOA DIRECTION REGISTER

		D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
GP04	R/W	RESERVED			GP4_OUT	GP3_OUT	GP2_OUT	GP1_OUT	GP0_OUT	0x00

DC ELECTRICAL CHARACTERISTICS

(T_A = 0°C - 70°C[4], V_{cc} = +3.3 V ± 10%)

Note: Numbers appearing in parentheses represent the values for TXD/IRTX, IRTX, IRMODE/IRRX3 when VIO is 5 Volt.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
IS Type Input Buffer						
Low Input Level	V_{ILIS}			0.8	V	Schmitt Trigger
High Input Level	V_{IHIS}	2.2			V	Schmitt Trigger
Schmitt Trigger Hysteresis	V_{HYS}		250		mV	
I_{CLK} Input Buffer						
Low Input Level	V_{ILCK}			0.4	V	
High Input Level	V_{IHCK}	2.8			V	
Input Leakage (All I and IS buffers except PWRGD)						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	µA	V_{IN} = V_{cc}
Input Current PWRGD	I_{OH}		75	150	µA	V_{IN} = 0
IO12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA (24mA)
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA (-12mA)
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{cc} (Note 1)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
O12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{cc} (Note 1)
O12PD Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA (24mA)
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA (-12mA)
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{cc} (Note 1)
O_{CLK} Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 2mA
High Output Level	V_{OH}	2.2			V	I_{OH} = -2mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{cc} (Note 1)
OD12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{cc} (Note 1)
Supply Current Active	I_{CC}			8	mA	All outputs open.
Supply Current Standby	I_{CSBY}			*2.5*	µA	Note 3

TABLE 34 - DC ELECTRICAL CHARACTERISTICS

Note 1: All output leakages are measured with the current pins in high impedance as defined by the PWRGD pin.
Note 2: Output leakage is measured with the low driving output off, either for a high level output or a high impedance state defined by PWRGD.
Note 3: Defined by the device configuration with the PWRGD input low.
Note 4: Junction Temperature rise at 70°C ambient will be approximately 1.7°C. Junction Temperature rise = Ambient Temp. +~~θ~~ja x Max. Power; where ~~θ~~ja = 56.8 and Max. Power = 3.6V x 8mA

A.C. TIMING

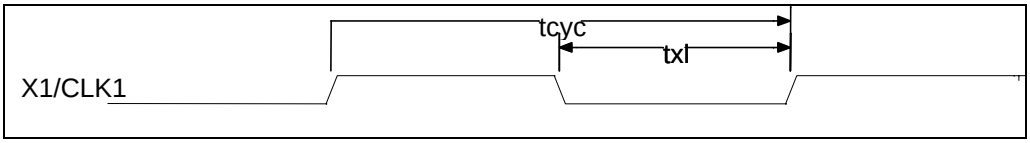


FIGURE 8 - EXTERNAL CLOCK INPUT TIMING

Clock and Reset Timing

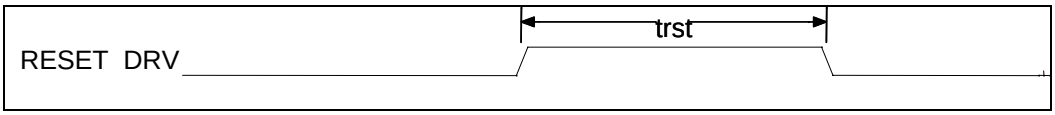


FIGURE 9 - RESET_DRV PULSE TIMING

TABLE 35 - CRYSTAL AND RESET TIMING PARAMETERS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
tcyc	Clock Cycle Time	37	41	45	ns
txl	Clock Low Pulse Width	18.5	20.5	22.5	ns
trst	Reset Pulse Width	10			us

Read Cycle Timing (Non-Multiplexed)

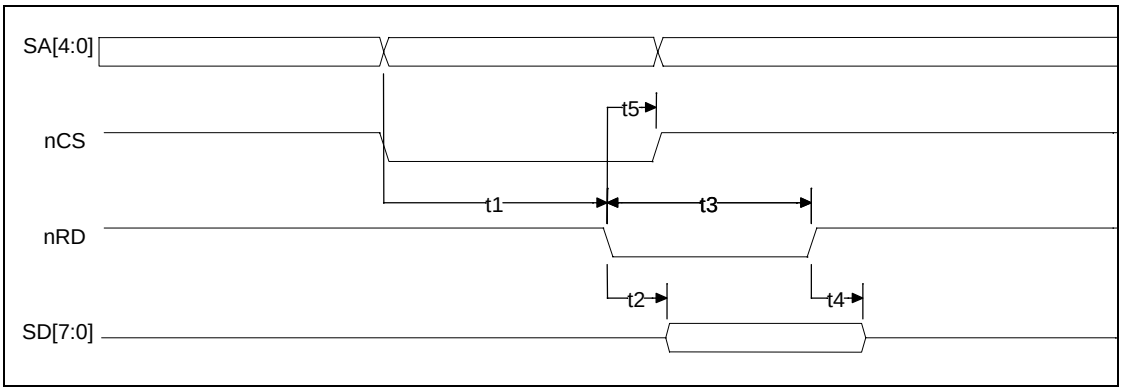


FIGURE 10 - READ CYCLE (NON-MULTIPLEXED ADDRESS AND DATA)

TABLE 36 - READ CYCLE TIMING PARAMETERS (NON-MULTIPLEXED ADDRESS AND DATA)

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Chip Select and Address Valid to Read Pulse Active	15			ns
t2	Read Pulse Active to Data Valid	0		55	ns
t3	Read Pulse Width	85			ns
t4	Data Hold Time	5			ns
t5 Note 1	Read Pulse Active to Chip Select and Address Invalid	15			ns

Note 1: Chip select must be latched internally and released when read pulse goes inactive.

Read Cycle Timing (Multiplexed)

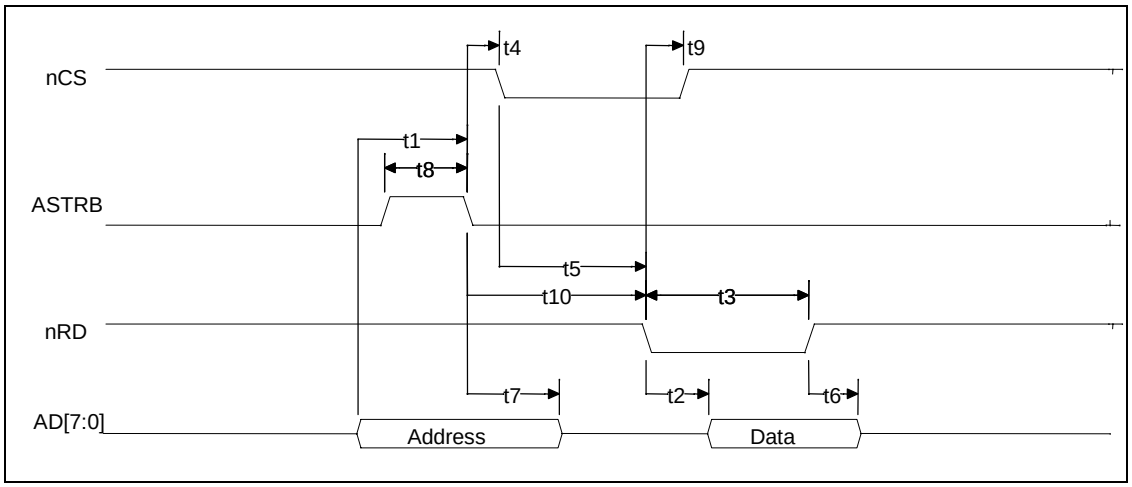


FIGURE 11 - READ CYCLE (MULTIPLEXED ADDRESS AND DATA)

TABLE 37 - READ CYCLE TIMING PARAMETERS (MULTIPLEXED ADDRESS AND DATA)

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Address Strobe Setup Time	30			ns
t2	Read Pulse Active to Data Valid			55	ns
t3	Read Pulse Width	85			ns
t4	Address Strobe Inactive to Chip Select Active	0		8	ns
t5	Chip Select Active to Read Pulse Active	15			ns
t6	Data Hold Time	5			ns
t7	Address Strobe Hold Time	5		15	ns
t8	Address Strobe Pulse Width	23			ns
t9 Note 1	Read Pulse Active to Chip Select Inactive	15			ns
t10	Address Strobe Inactive to Read Pulse Active	15			

Note 1: Chip select must be latched internally and released when read pulse goes inactive.

Write Cycle Timing (Non-Multiplexed)

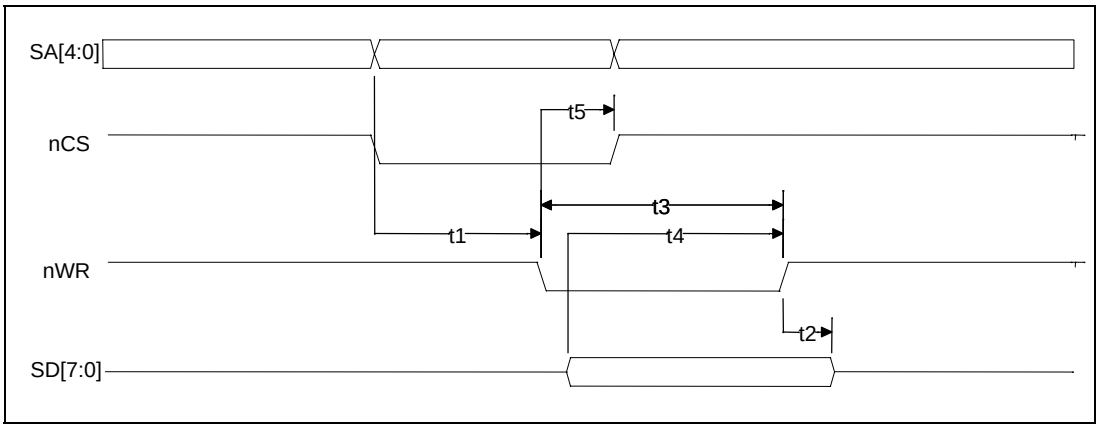


FIGURE 12 - WRITE CYCLE (NON-MULTIPLEXED ADDRESS AND DATA)

TABLE 38 - WRITE CYCLE TIMING PARAMETERS (NON-MULTIPLEXED ADDRESS AND DATA)

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Chip Select and Address Valid to Write Pulse Active	23			ns
t2	Data Hold Time	8			ns
t3	Write Pulse Width	85			ns
t4	Data valid to Write Pulse Inactive	30			ns
t5 Note 1	Write Pulse Active to Chip Select and Address Invalid	15			ns

Note 1: Chip select must be latched internally and released when write pulse goes inactive.

Write Cycle Timing (Multiplexed)

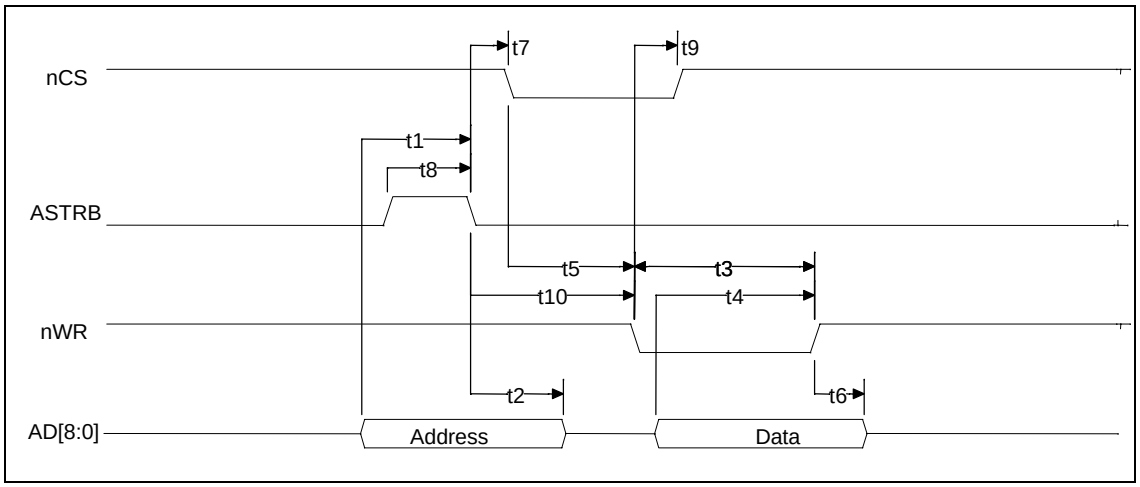


FIGURE 13 - WRITE CYCLE (MULTIPLEXED ADDRESS AND DATA)

TABLE 39 - WRITE CYCLE TIMING PARAMETERS (MULTIPLEXED ADDRESS AND DATA)

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Address Strobe Setup Time	30			ns
t2	Address Strobe Hold Time	8		15	ns
t3	Write Pulse Width	85			ns
t4	Data Valid to Write Pulse Inactive	30			ns
t5	Chip Select Active to Write Pulse Active	15			ns
t6	Data Hold Time	5			ns
t7	Address Strobe Inactive to nCS Active	0		5	ns
t8	Address Strobe Pulse Width	23			ns
t9 Note 1	Write Pulse Active to Address Strobe Inactive	15			ns
t10	Address Strobe Inactive to Write Pulse Active	10			

Note 1: Chip select must be latched internally and released when write pulse goes inactive.

Read/Write Cycle Timing (Multiplexed)

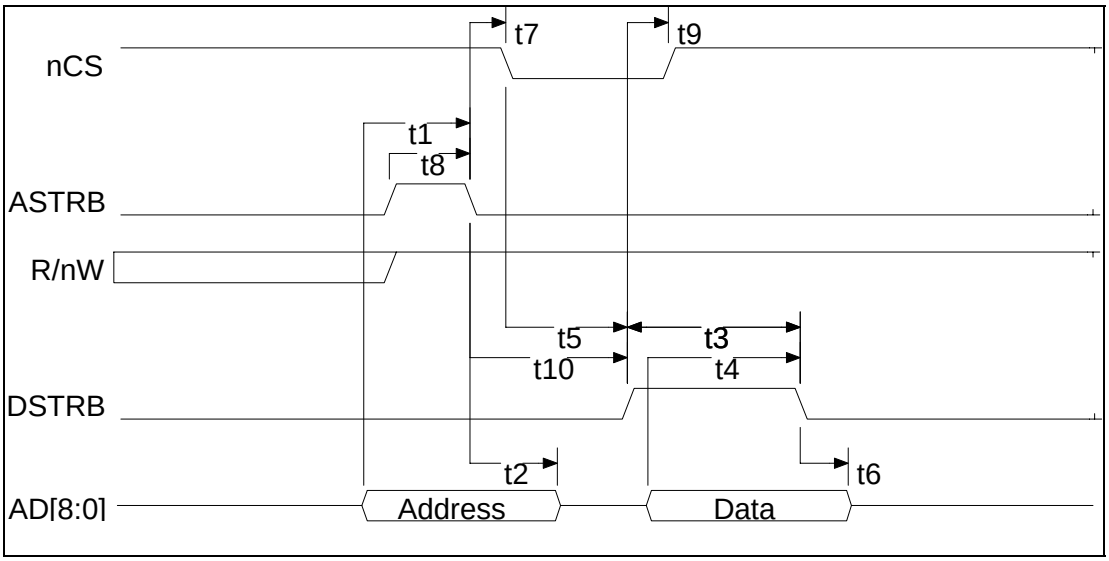


FIGURE 14 - READ/WRITE CYCLE (MULTIPLEXED ADDRESS AND DATA)

TABLE 40 - READ/WRITE CYCLE TIMING PARAMETERS (MULTIPLEXED ADDRESS AND DATA)

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Address Strobe Setup Time	30			ns
t2	Address Strobe Hold Time	8		15	ns
t3	Data Strobe Pulse Width	85			ns
t4	Data Valid to R/nW Pulse Inactive	30			ns
t5	Chip Select Active to R/nW Pulse Active	15			ns
t6	Data Hold time	5			ns
t7	Address Strobe Inactive to nCS Active	0		5	ns
t8	Address Strobe Pulse Width	23			ns
t9 Note 1	R/nW Pulse Active to Address Strobe Inactive	15			ns
t10	Address Strobe Inactive to R/nW Pulse Active	10			

Note 1: Chip select must be latched internally and released when write pulse goes inactive.

Single Transfer Mode DMA Timing

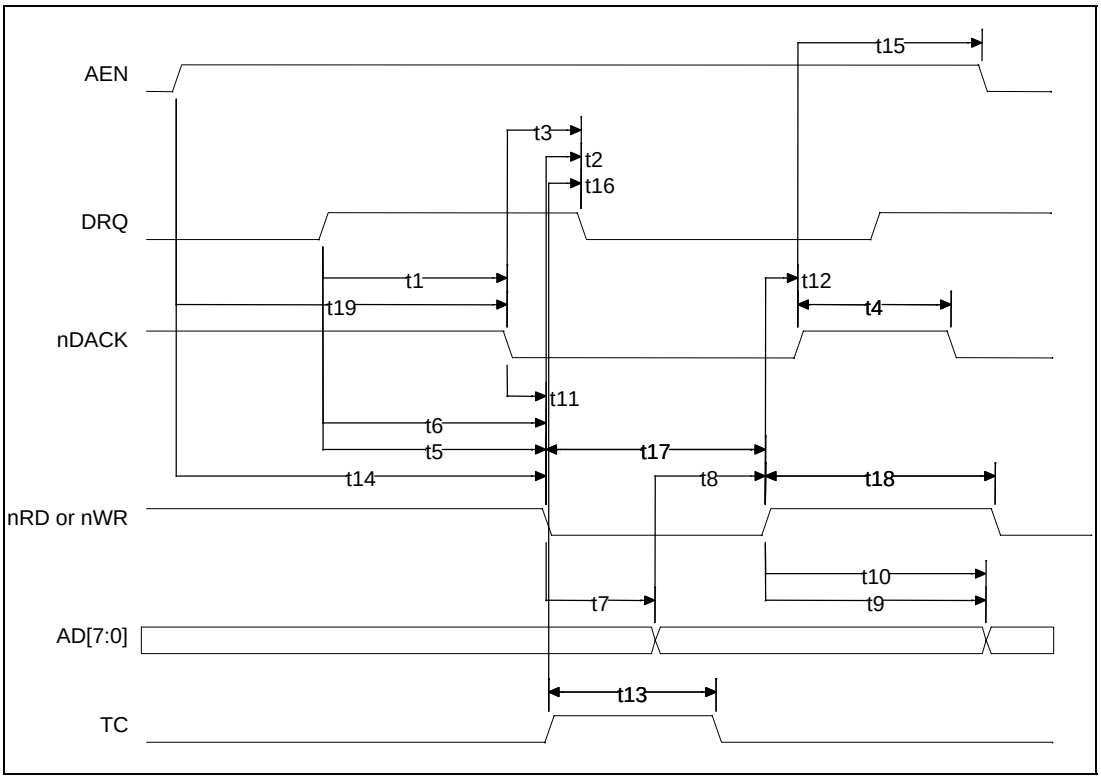


FIGURE 15 - SINGLE TRANSFER MODE DMA TIMING
Refer to table on the following page.

TABLE 41 - SINGLE TRANSFER MODE DMA TIMING PARAMETERS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nDACK Delay Time from DRQ High	0			ns
t2	DRQ Reset Delay from nRD or nWR			15	ns
t3	DRQ Reset Delay from nDACK Low			15	ns
t4	nDACK Inactive	30			ns
t5	nRD Delay from DRQ High	15			ns
t6	nWR Delay from DRQ High	15			ns
t7	Data Access Time from nRD Low			55	ns
t8	Data Set Up Time to nWR High	30			ns
t9	Data to Float Delay from nRD High	5			ns
t10	Data Hold Time from nWR High	5			ns
t11	nDACK Set Up to nWR/nRD Low	5			ns
t12	nDACK Hold after nWR/nRD High	5			ns
t13	TC Pulse Width	30			ns
t14	AEN Set Up to nRD/nWR	30			ns
t15	AEN Hold from nDACK	0			ns
t16	TC Active to DRQ Inactive			15	ns
t17	nRD/nWR Pulse Width	85			ns
t18	nRD/nWR Inactive	30			ns
t19	AEN Active to nDACK Active	0			ns

Burst Transfer Mode DMA Timing

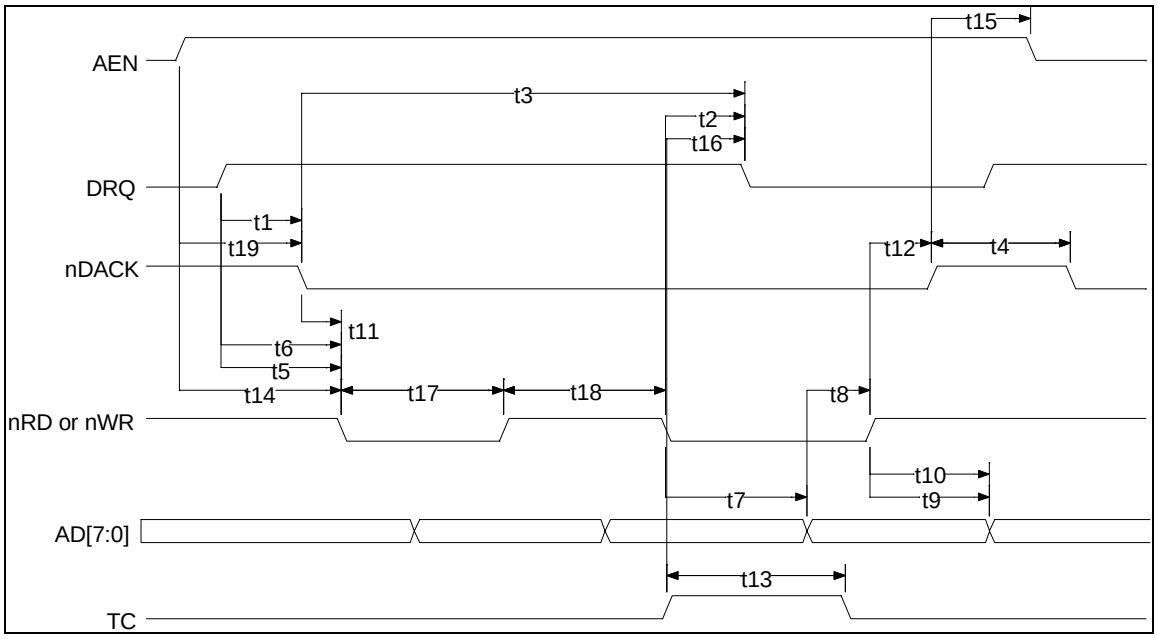


FIGURE 16 - BURST TRANSFER MODE DMA TIMING
Refer to table on the following page.

TABLE 42 - DMA TIMING (BURST TRANSFER MODE) PARAMETERS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nDACK Delay Time from DRQ High	0			ns
t2	DRQ Reset Delay from nRD or nWR			15	ns
t3	DRQ Reset Delay from nDACK Low			15	ns
t4	nDACK Inactive	30			ns
t5	nRD Delay from DRQ High	15			ns
t6	nWR Delay from DRQ High	15			ns
t7	Data Access Time from nRD Low			55	ns
t8	Data Set Up Time to nWR High	30			ns
t9	Data to Float Delay from nRD High	5			ns
t10	Data Hold Time from nWR High	5			ns
t11	nDACK Set Up to nWR/nRD Low	5			ns
t12	nDACK Hold after nWR/nRD High	5			ns
t13	TC Pulse Width	30			ns
t14	AEN Set Up to nRD/nWR	15			ns
t15	AEN Hold from nDACK	0			ns
t16	TC Active to DRQ Inactive			15	ns
t17	nRD/nWR Pulse Width	85			ns
t18	nRD/nWR Inactive	30			ns
t19	AEN Active to nDACK Active	0			ns

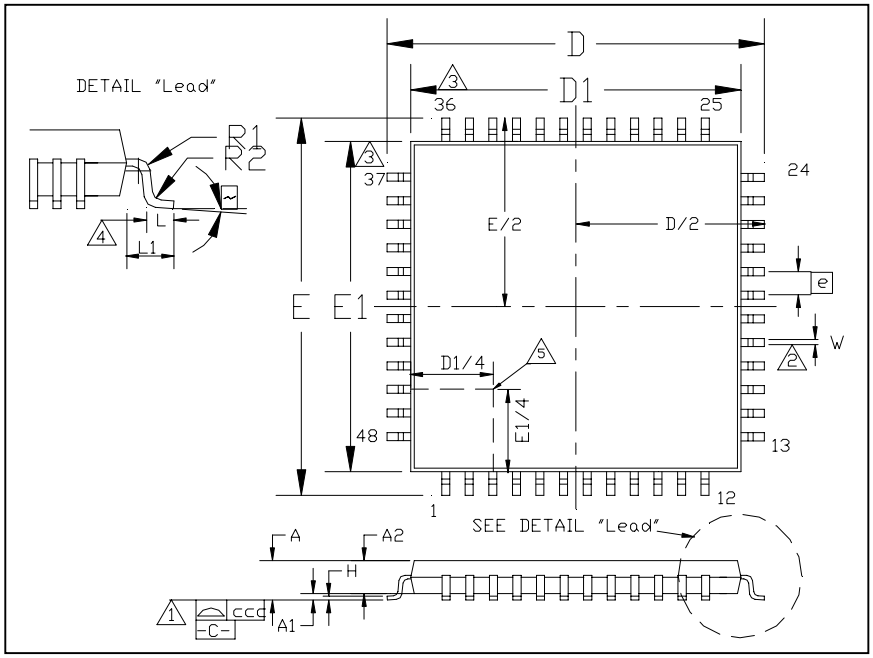


FIGURE 17 - 48 PIN TQFP PACKAGE OUTLINE

	MIN	NOMINAL	MAX	REMARK
A	~	~	1.6	Overall Package Height
A1	0.05	0.10	0.15	Standoff
A2	1.35	1.40	1.45	Body Thickness
D	~	9.00	~	X Span
D/2	4.40	4.50	4.60	$^1/_2$ X Span Measure from Centerline
D1	~	7.00	~	X body Size
E	~	9.00	~	Y Span
E/2	4.40	4.50	4.60	$^1/_2$ Y Span Measure from Centerline
E1	~	7.00	~	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length from Centerline
L1	~	1.00	~	Lead Length
e		0.50 Basic		Lead Pitch
θ	0^o	~	7^o	Lead Foot Angle
W	0.17	~	0.27	Lead Width
R1	0.08	~	~	Lead Shoulder Radius

	MIN	NOMINAL	MAX	REMARK
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.0762	Coplanarity (Assemblers)
ccc	~	~	0.08	Coplanarity (Test House)

Note 1: Controlling Unit: millimeter
Note 2: Tolerance on the position of the leads is ± 0.04 mm maximum.
Note 3: Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm.
Note 4: Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane is 0.78-1.08 mm.
Note 5: Details of pin 1 identifier are optional but must be located within the zone indicated.

CAM35C44 ERRATA SHEET

PAGE	SECTION/FIGURE/ENTRY	CORRECTION	DATE REVISED
1	GENERAL DESCRIPTION	24mA changed to 12mA	1/7/98
10	DESCRIPTION OF PIN FUNCTIONS	See Italicized Text	1/7/98
21	TABLE 13/REGISTER NAME	See Italicized Text	1/7/98
29	TABLE 25	See Italicized Text	1/7/98
37	Note 4 added	See Italicized Text	1/7/98
29	TABLE 25	2μA changed to 2.5μA	8/10/99
37	TABLE 34 – MAX Column	See Italicized Text	8/10/99

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