

## Dual-Channel, 3.3V/500mA and 2.5V/300mA Linear Regulator

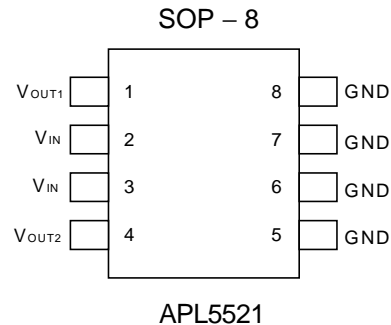
### Features

- Fixed Output Voltage :  
 $V_{OUT1}=3.3V/500mA$   
 $V_{OUT2}=2.5V/300mA$
- Low Dropout Voltage (defined as the minimum input/output voltage difference):  
 Output 1 Dropout Voltage : 1.25V (at 500mA)  
 Output 2 Dropout Voltage : 1.2V (at 300mA)
- Stable with 10uF Output Capacitor(at  $V_{OUT1}$ )  
 Stable with 10uF Output Capacitor(at  $V_{OUT2}$ )
- No Protection Diodes Needed
- Built in Thermal Protection
- Built in Current Limit Protection
- Fast transient Response
- Short Setting Time
- SOP-8 Package Available

### General Description

The APL5521 is a dual low dropout regulator with output 1 with 3.3V/0.5A and output2 with 2.5V/0.3A output capability. In order to obtain lower dropout voltage and faster transient response, which is critical for low voltage applications, the APL5221 has been optimized. The dropout voltages are guaranteed at 1.25V at 0.5A for output1 and 1.2V at 0.3A for output 2. Current limit is trimmed to ensure specified output current and controlled short-circuit current. On-chip thermal limiting provides protection against any combination of overload that would create excessive junction temperatures. The APL5521 regulator comes in a SOP-8 package.

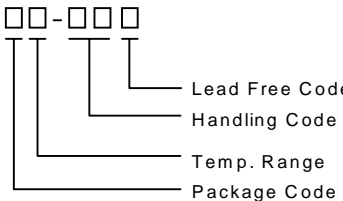
### Pin Configuration



### Applications

- Desktop Computer
- Networking Systems
- Optical Data Storage Systems

### Ordering and Marking Information

<p>APL5521    □□-□□□</p>  <p style="margin-left: 150px;">       Lead Free Code        Handling Code        Temp. Range        Package Code     </p>	<p>Package Code K : SO-8</p> <p>Operating Junction Temp. Range C : 0 to 150°C</p> <p>Handling Code TU : Tube    TR : Tape &amp; Reel</p> <p>Lead Free Code L : Lead Free Device    Blank : Original Device</p>
<p>APL5521 K :    <span style="border: 1px solid black; padding: 2px;">APL5521 XXXXX</span></p>	<p>XXXXXX - Date Code</p>

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

## Pin Description

PIN		I/O	Description
No.	Name		
1	V <sub>OUT1</sub>	O	V <sub>OUT1</sub> output Voltage 3.3V. sources up to 500 mA.
2	V <sub>IN</sub>	I	Supply Voltage. Voltage can range from 4.75V to 8V
3	V <sub>IN</sub>	I	Supply Voltage. Voltage can range from 4.75V to 8V
4	V <sub>OUT2</sub>	O	V <sub>OUT2</sub> output Voltage 2.5V. sources up to 300 mA.
5	GND		Ground also functions as a heatsink. Solder to the ground plane to maximize thermal dissipation
6	GND		
7	GND		
8	GND		

## Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V <sub>IN</sub> , V <sub>OUT</sub>	Input Voltage or Out Voltage	9	V
RTH,JA	Thermal Resistance – Junction to Ambient	80	°C/W
PD	Power Dissipation	Internally Limited	W
TJ	Operating Junction Temperature		°C
	Control Section Power Transistor	0 to 125 0 to 150	
TSTG	Storage Temperature Range	-65 to +150	°C
TL	Lead Temperature (Soldering, 10 second)	260	°C

## Electrical Characteristics

Unless otherwise noted these specifications apply over full temperature, T<sub>J</sub>=0 to 125°C. Typical values refer to T<sub>J</sub>=25°C.

Symbol	Parameter	Test Conditions	APL5521			Unit
			Min.	Typ.	Max.	
V <sub>IN</sub>	Input Voltage		4.75		8	V
I <sub>Q</sub>	Quiescent Current	I <sub>OUT1</sub> =0mA, I <sub>OUT2</sub> =0mA		10	16	mA
OTS	Over Temperature Shutdown			150		°C
	Over Temperature Shutdown Hysteresis	Hysteresis		10		°C
TC	Output Voltage Temperature Coefficient			50		ppm/°C

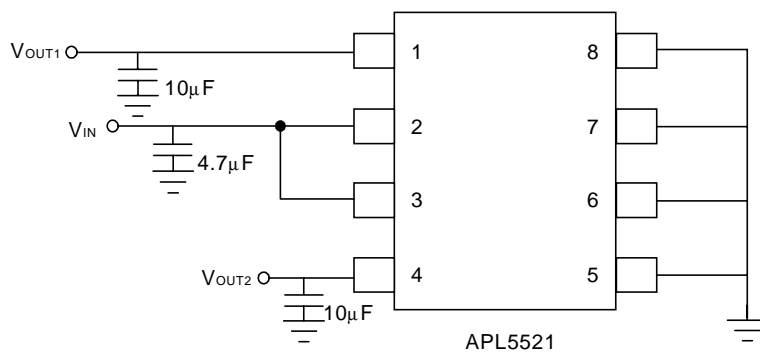
## Electrical Characteristics (Cont.)

Unless otherwise noted these specifications apply over full temperature,  $T_j=0$  to  $125^\circ\text{C}$ . Typical values refer to  $T_j=25^\circ\text{C}$ .

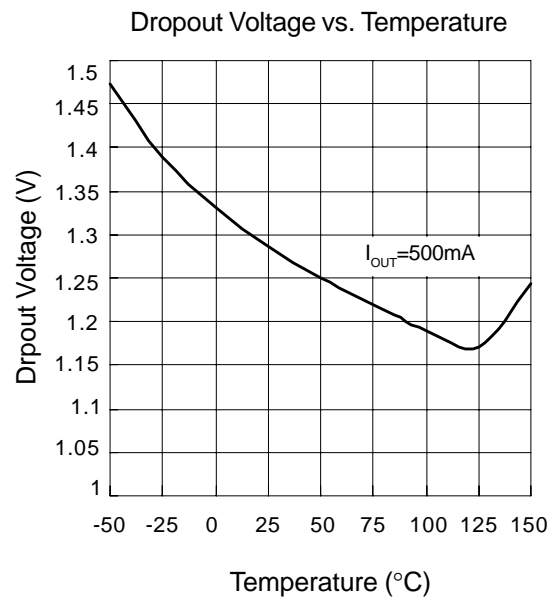
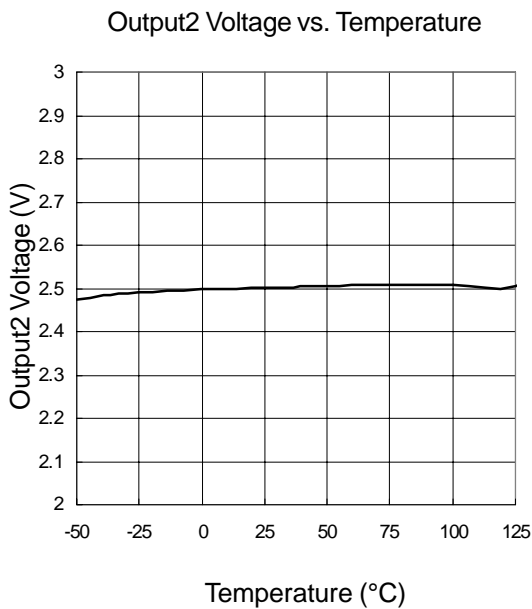
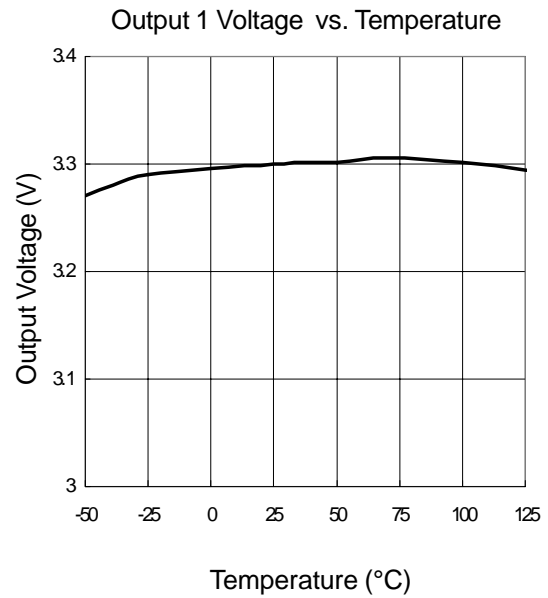
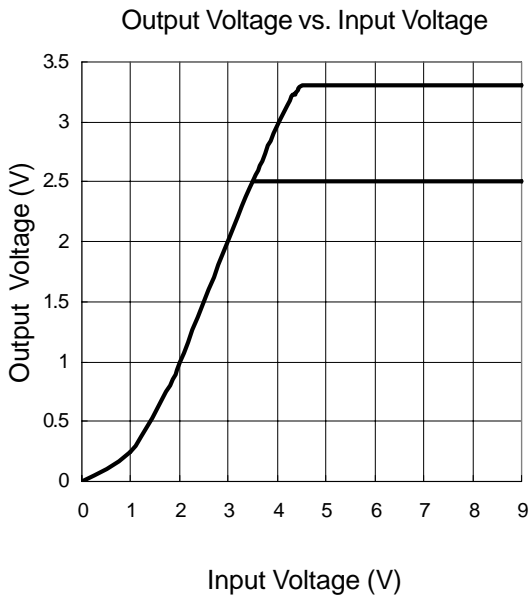
Symbol	Parameter	Test Conditions	APL5521			Unit
			Min.	Typ.	Max.	
Output1 (500mA)						
$V_{OUT1}$	Output 1 Voltage	$4.75 < V_{IN} < 8.0\text{V}$ , $0\text{mA} < I_{OUT1} < 500\text{mA}$	3.234	3.3	3.366	V
$I_{OUT1}$	Output 1 Current Capability	$V_{IN}=5\text{V}$	500			mA
REG <sub>LINE</sub>	Line Regulation	$4.75 < V_{IN} < 8.0\text{V}$ , $I_{OUT1}=0\text{mA}$		1	10	mV
REG <sub>LOAD</sub>	Load Regulation	$V_{IN}=5\text{V}$ , $0\text{mA} < I_{OUT1} < 500\text{mA}$		14	24	mV
	Load Transient	$V_{IN}=5\text{V}$ , $I_{OUT1}=1\text{mA}\sim 500\text{mA}$ in 30us		70	150	mV
$V_{DROP}$	Dropout Voltage <sup>(Note)</sup>	$I_{OUT1}=500\text{mA}$		1.25	1.4	V
PSRR	Ripple Rejection	$F \leq 1\text{kHz}$ , 1Vpp at $V_{IN}=5\text{V}$	55	65		dB
$C_{OUT}$	Output Capacitor	$C_{OUT1}$		10		$\mu\text{F}$
Output2 (300mA)						
$V_{OUT2}$	Output 2 Voltage	$4.75 < V_{IN} < 8.0\text{V}$ , $0\text{mA} < I_{OUT2} < 300\text{mA}$	2.450	2.5	2.550	V
$I_{OUT2}$	Output 2 Current Capability	$V_{IN}=5\text{V}$	300			mA
REG <sub>LINE</sub>	Line Regulation	$4.75 < V_{IN} < 8.0\text{V}$ , $I_{OUT2}=0\text{mA}$		1	10	mV
REG <sub>LOAD</sub>	Load Regulation	$V_{IN}=5\text{V}$ , $0\text{mA} < I_{OUT2} < 300\text{mA}$		8	18	mV
	Load Transient	$V_{IN}=5\text{V}$ , $I_{OUT2}=1\text{mA}\sim 300\text{mA}$ in 20us		70	150	mV
$V_{DROP}$	Dropout Voltage <sup>(Note)</sup>	$I_{OUT1}=300\text{mA}$		1.2	1.35	V
PSRR	Ripple Rejection	$F \leq 1\text{kHz}$ , 1Vpp at $V_{IN}=5\text{V}$	55	65		dB
$C_{OUT}$	Output Capacitor	$C_{OUT2}$		10		$\mu\text{F}$

Note: Dropout voltage definition :  $V_{IN}-V_{OUT}$  when  $V_{OUT}$  is 2% below the value of  $V_{OUT}$  for  $V_{IN} = V_{OUT} + 1.4\text{V}$

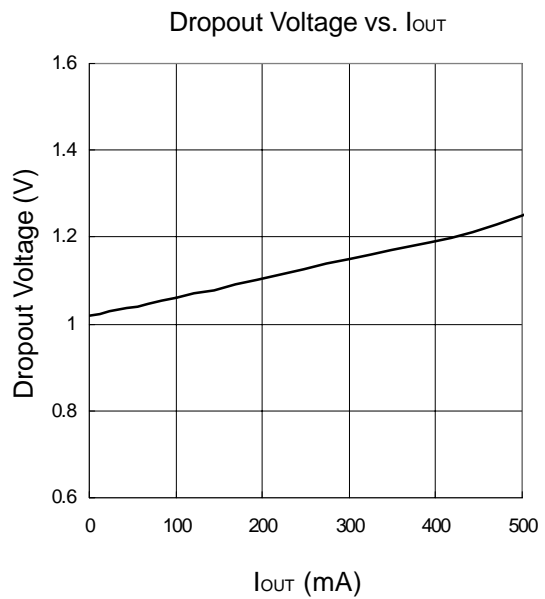
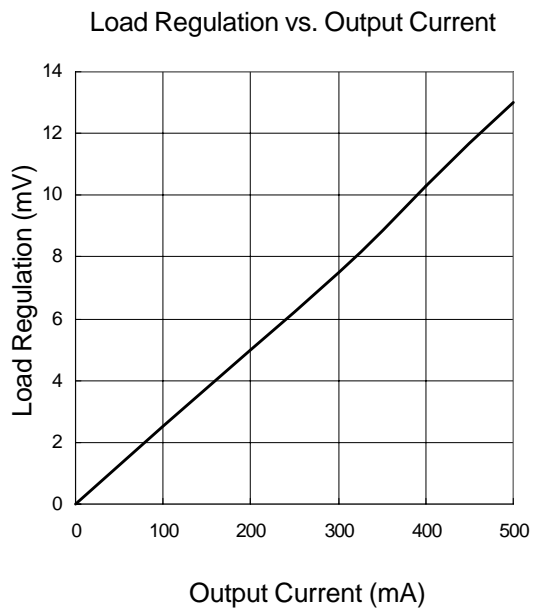
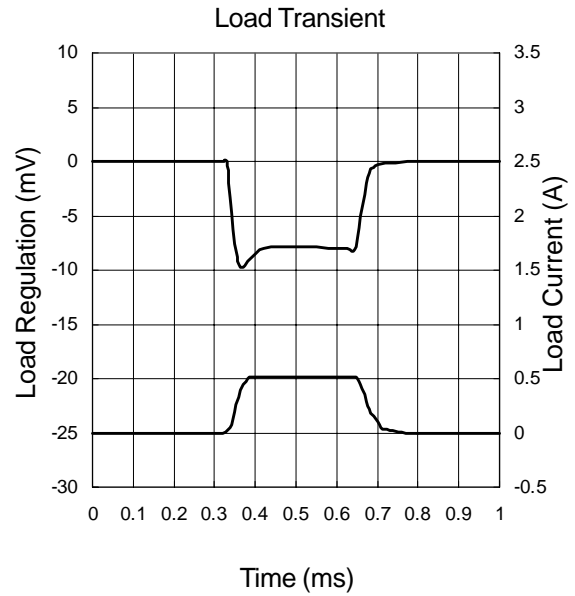
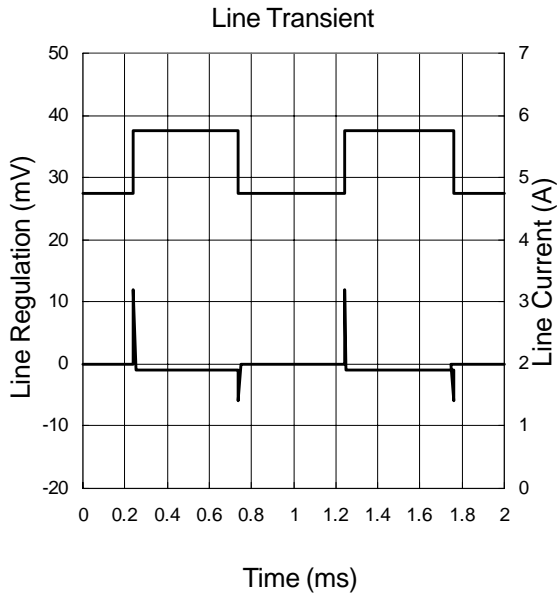
## Application Circuit



## Typical Characteristics

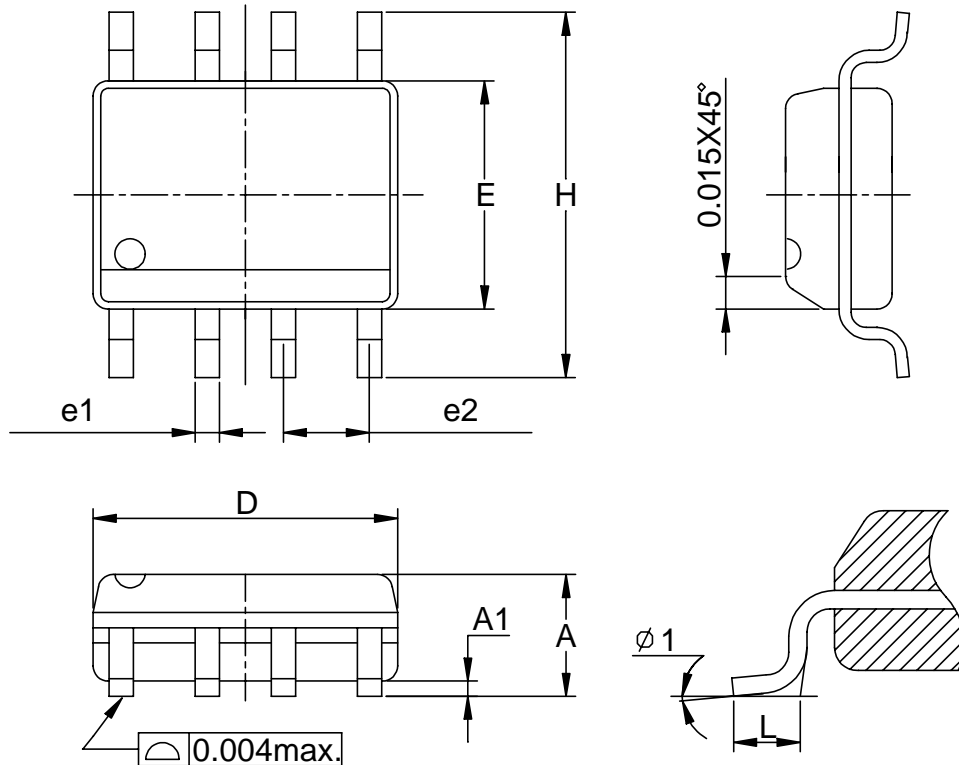


Typical Characteristics (Cont.)



## Packaging Information

SOP-8 pin ( Reference JEDEC Registration MS-012)



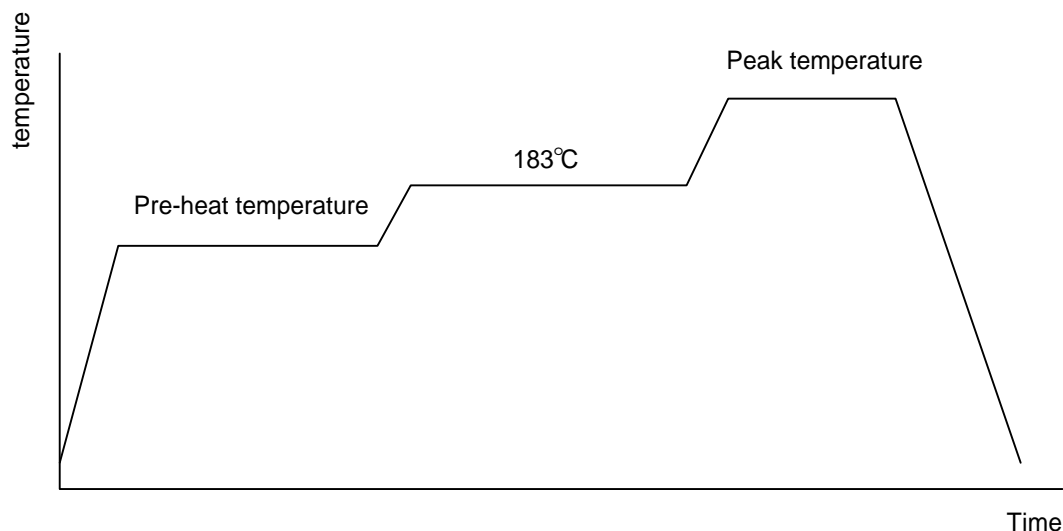
Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.00	0.150	0.157
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
e1	0.33	0.51	0.013	0.020
e2	1.27BSC		0.50BSC	
φ 1	8°		8°	

## Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb)
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

## Reflow Condition (IR/Convection or VPR Reflow)

Reference JEDEC Standard J-STD-020A APRIL 1999



## Classification Reflow Profiles

	Convection or IR/ Convection	VPR
Average ramp-up rate(183°C to Peak)	3°C/second max.	10 °C /second max.
Preheat temperature 125 ± 25°C)	120 seconds max	
Temperature maintained above 183°C	60 – 150 seconds	
Time within 5°C of actual peak temperature	10 –20 seconds	60 seconds
Peak temperature range	220 +5/-0°C or 235 +5/-0°C	215-219°C or 235 +5/-0°C
Ramp-down rate	6 °C /second max.	10 °C /second max.
Time 25°C to peak temperature	6 minutes max.	

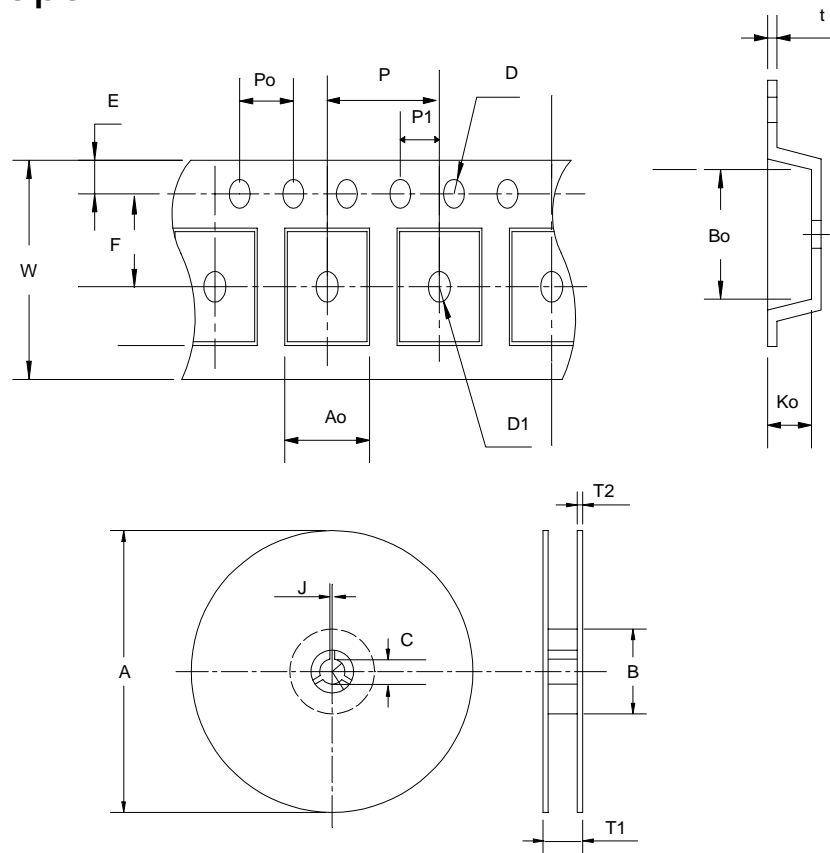
## Package Reflow Conditions

pkg. thickness ≥ 2.5mm and all bgas	pkg. thickness < 2.5mm and pkg. volume ≥ 350 mm <sup>3</sup>	pkg. thickness < 2.5mm and pkg. volume < 350mm <sup>3</sup>
Convection 220 +5/-0 °C		Convection 235 +5/-0 °C
VPR 215-219 °C		VPR 235 +5/-0 °C
IR/Convection 220 +5/-0 °C		IR/Convection 235 +5/-0 °C

### Reliability test program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C , 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @ 125 °C
PCT	JESD-22-B, A102	168 Hrs, 100 % RH , 121°C
TST	MIL-STD-883D-1011.9	-65°C ~ 150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms , I <sub>tr</sub> > 100mA

### Carrier Tape



<b>Application</b>	A	B	C	J	T1	T2	W	P	E
<b>SOP-8</b>	330±1	62 ± 1.5	12.75 + 0.15	2 + 0.5	12.4 +0.2	2± 0.2	12 + 0.3 - 0.1	8± 0.1	1.75± 0.1
<b>Application</b>	F	D	D1	Po	P1	Ao	Bo	Ko	t
<b>SOP-8</b>	5.5 ± 0.1	1.55±0.1	1.55+ 0.25	4.0 ± 0.1	2.0 ± 0.1	6.4 ± 0.1	5.2± 0.1	2.1± 0.1	0.3±0.013

(mm)



## Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP- 8	12	9.3	2500

## Customer Service

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