



**N-Channel Enhancement-Mode
Vertical DMOS FETs**

Ordering Information

BV _{DSS} / BV _{DGS}	R _{DS(ON)} (max)	I _{D(ON)} (min)	Order Number / Package
			TO-39
60V	3.0Ω	1.5A	2N6660
90V	4.0Ω	1.5A	2N6661

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor controls
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV _{DSS}
Drain-to-Gate Voltage	BV _{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

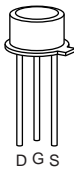
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-39
Case: DRAIN

Note: See Package Outline section for dimensions.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25^\circ\text{C}$	θ_{jc} $^\circ\text{C/W}$	θ_{ja} $^\circ\text{C/W}$	I_{DR}^*	I_{DRM}
2N6660	1.1A	3A	6.25W	20	125	1.1A	3.0A
2N6661	0.9A	3A	6.25W	20	125	0.9A	3.0A

* I_D (continuous) is limited by max rated T_j .

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	2N6660	60		V	$V_{GS} = 0V, I_D = 10\mu\text{A}$
		2N6661	90			
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.0	V	$V_{GS} = V_{DS}, I_D = 1\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		-3.8	-5.5	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = 1\text{mA}$
I_{GSS}	Gate Body Leakage			100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current			10	μA	$V_{GS} = 0V, V_{DS} = \text{Max Rating}$
				500		$V_{GS} = 0V, V_{DS} = 0.8 \text{ Max Rating}, T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current	1.5			A	$V_{GS} = 10V, V_{DS} = 10V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance	All		5.0	Ω	$V_{GS} = 5V, I_D = 0.3A$
		2N6660		3.0		$V_{GS} = 10V, I_D = 1A$
		2N6661		4.0		$V_{GS} = 10V, I_D = 1A$
G_{FS}	Forward Transconductance	170			m Ω	$V_{DS} = 25V, I_D = 0.5A$
C_{ISS}	Input Capacitance			50	pF	$V_{GS} = 0V, V_{DS} = 24V$ $f = 1 \text{ MHz}$
C_{OSS}	Common Source Output Capacitance			40		
C_{RSS}	Reverse Transfer Capacitance			10		
$t_{(ON)}$	Turn-ON Time			10	ns	$V_{DD} = 25V,$ $I_D = 1A, R_{GEN} = 25\Omega$
$t_{(OFF)}$	Turn-OFF Time			10		
V_{SD}	Diode Forward Voltage Drop		1.2		V	$V_{GS} = 0V, I_{SD} = 1A$
t_{rr}	Reverse Recovery Time		350		ns	$V_{GS} = 0V, I_{SD} = 1A$

Notes:

- 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)
- 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

