

TOSHIBA Bipolar Linear Integrated Circuit Silicon Monolithic

# TA2153FN

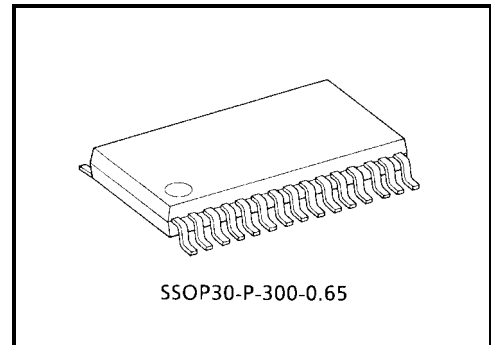
## RF Amplifier for Digital Servo CD System

TA2153FN is a 3-beam type PUH compatible RF amplifier for digital servo to be used in the CD system.

In combination with a CMOS single chip processor TC9462F/TC9495F, a CD system can be composed very simply.

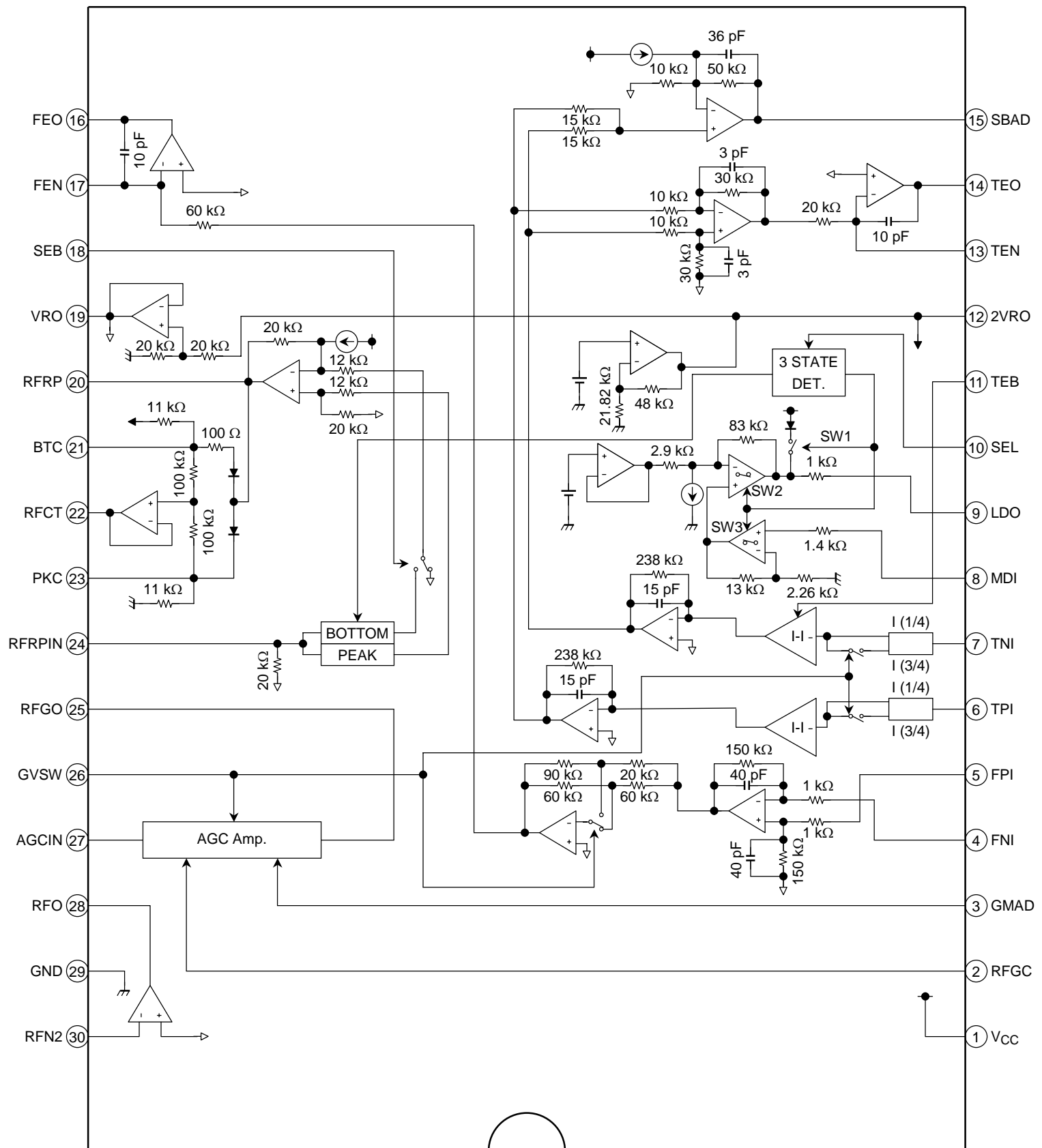
### Features

- Built-in amplifier for reference (VRO, 2VRO) supply.
- Built-in auto laser power control circuit.
- Built-in RF amplifier.
- Built-in AGC amplifier.
- Built-in focus error amp and tracking error amp.
- Built-in sub-beam adder signal amplifier.
- Built-in gain change circuit for CD-RW.
- Capable of tracking balance control with TC9462F/TC9495F.
- Capable of RF gain adjustment circuit with TC9462F/TC9495F.
- Built-in signal amplifier for track counter.
- Capable of 4 times speed operation.
- 30 pin mini flat package.



Weight: 0.17 g (typ.)

**Block Diagram**



SEL	LDC			RFRP Detect Frequency
	SW1	SW2	SW3	
GND	ON	OFF	OFF	Low
HiZ	OFF	ON	ON	Low
V <sub>CC</sub>	OFF	ON	ON	High

GVSW	Mode
GND	CD-RW
HiZ	Normal
V <sub>CC</sub>	

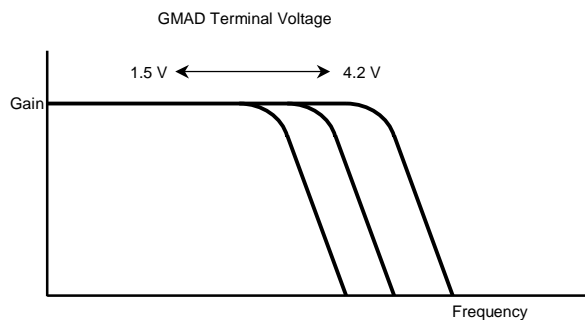
SEB	Bottom Detect	Peak Detect
GND	ON	ON
HiZ	ON	ON
V <sub>CC</sub>	OFF	ON

## Pin Function

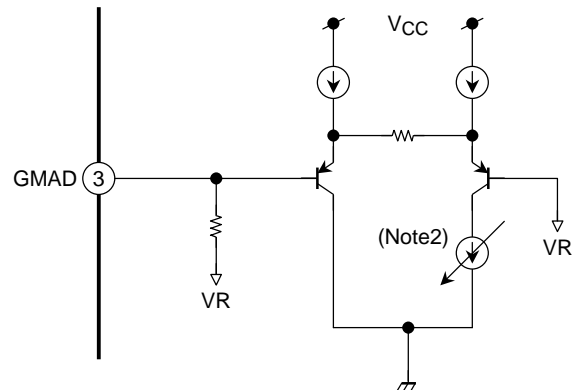
Pin No.	Symbol	I/O	Function Description	Remarks																
1	V <sub>CC</sub>	—	Power supply input terminal.	—																
2	RFGC	I	RF amplitude adjustment control signal input terminal. Controlled by 3-PWM signals. (PWM carrier = 88.2 kHz)	3 signals input. (2VRO, VRO, GND)																
3	GMAD	I	Open loop gain adjustment terminal for AGC amp.	(Note1)																
4	FNI	I	Main beam I-V amp input terminal.	Connected to pin diode output B + D (through resistor).																
5	FPI	I	Main beam I-V amp input terminal.	Connected to pin diode output A + C (through resistor).																
6	TPI	I	Sub beam I-V amp input terminal.	Connected to pin diode output F.																
7	TNI	I	Sub beam I-V amp input terminal.	Connected to pin diode output E.																
8	MDI	I	Monitor photo diode amp input terminal.	Connected to monitor photo diode.																
9	LDO	O	Laser diode amp input terminal.	Connected to laser diode control circuit.																
10	SEL	I	Laser diode control signal input terminal and APC circuit ON/OFF control signal terminal. <table border="1" style="margin: 10px auto;"> <thead> <tr> <th>SEL Level</th> <th>APC Circuit</th> <th>LDO</th> <th>Detect Frequency</th> </tr> </thead> <tbody> <tr> <td>GND</td> <td>OFF</td> <td>Connected to V<sub>CC</sub> through resistor (1 kΩ)</td> <td>Low</td> </tr> <tr> <td>HiZ</td> <td>ON</td> <td>Control signal output</td> <td>Low</td> </tr> <tr> <td>V<sub>CC</sub></td> <td>ON</td> <td>Control signal output</td> <td>High</td> </tr> </tbody> </table>	SEL Level	APC Circuit	LDO	Detect Frequency	GND	OFF	Connected to V <sub>CC</sub> through resistor (1 kΩ)	Low	HiZ	ON	Control signal output	Low	V <sub>CC</sub>	ON	Control signal output	High	3 signals input. (V <sub>CC</sub> , HiZ, GND)
SEL Level	APC Circuit	LDO	Detect Frequency																	
GND	OFF	Connected to V <sub>CC</sub> through resistor (1 kΩ)	Low																	
HiZ	ON	Control signal output	Low																	
V <sub>CC</sub>	ON	Control signal output	High																	
11	TEB	I	Tracking error balance adjustment signal input terminal. Controlled by 3-PWM signal. (PWM carrier = 88.2 kHz)	3 signals input. (2VRO, VRO, GND)																
12	2VRO	O	Reference voltage (2VRO) output terminal. 2VRO = 4.2 V when V <sub>CC</sub> = 5 V	—																
13	TEN	I	TE amp negative input terminal.	Connected to TEO through feedback resistor.																
14	TEO	O	TE error signal output terminal.	—																
15	SBAD	O	Sub beam adder signal output terminal.	—																
16	FEO	O	Focus error signal output terminal.	—																
17	FEN	I	FE amp negative input terminal.	Connected to FEO through feedback resistor.																
18	SEB	I	RFRP output circuit switching terminal. <table border="1" style="margin: 10px auto;"> <thead> <tr> <th>SEB Level</th> <th>Bottom Detection</th> <th>Peak Detection</th> </tr> </thead> <tbody> <tr> <td>GND</td> <td>ON</td> <td>ON</td> </tr> <tr> <td>V<sub>CC</sub></td> <td>OFF</td> <td>ON</td> </tr> </tbody> </table>	SEB Level	Bottom Detection	Peak Detection	GND	ON	ON	V <sub>CC</sub>	OFF	ON	Low (GND) is for normal use.							
SEB Level	Bottom Detection	Peak Detection																		
GND	ON	ON																		
V <sub>CC</sub>	OFF	ON																		
19	VRO	O	Reference signal (VRO) output terminal. VRO = 2.1 V when V <sub>CC</sub> = 5 V	—																
20	RFRP	O	Track count signal output terminal.	—																
21	BTC	I	Time constant adjustment terminal for bottom detection.	Adjusted by capacitance.																

Pin No.	Symbol	I/O	Function Description	Remarks									
22	RFCT	O	RFRP signal center level output terminal.	—									
23	PKC	I	Time constant adjustment terminal for peak detection.	Adjusted by capacitance.									
24	RFRPIN	I	Input terminal for track count signal output amp.	—									
25	RFGO	O	Output terminal for RF signal amplitude adjustment amp.	—									
26	GVSW	I	Amp (AGC, FE, TE) gain switching terminal.	Low (GND) is for 5 times gain.									
					<table border="1"> <thead> <tr> <th>GVSW</th> <th>Mode</th> </tr> </thead> <tbody> <tr> <td>GND</td> <td>CD-RW</td> </tr> <tr> <td>HiZ</td> <td>Normal</td> </tr> <tr> <td>V<sub>CC</sub></td> <td>Normal</td> </tr> </tbody> </table>	GVSW	Mode	GND	CD-RW	HiZ	Normal	V <sub>CC</sub>	Normal
					GVSW	Mode							
					GND	CD-RW							
HiZ	Normal												
V <sub>CC</sub>	Normal												
27	AGCIN	I	Input terminal for RF signal amplitude adjustment amp.	Connected to RFO through capacitance.									
28	RFO	O	Output terminal for RF signal amp.	—									
29	GND	—	Ground terminal.	—									
30	RFN2	I	Input terminal for RF signal amp.	Connected to pin-diode output A + B + C + D (through resistor).									

Note 1: Pin3 (GMAD) is gm adjustment terminal for AGC amp by applying a voltage (between 1.5 V and 4.2 V).  
 If pin3 (GMAD) is open, voltage of this terminal is fixed VR by IC interior.  
 Characteristic of frequency (open-loop characteristic) and voltage is as below.



By changing a voltage (pin3) between 1.5 V and 4.2 V, frequency band width is changed.



Note 2: Current is changed by pin3 (GMAD) voltage.

## Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V <sub>CC</sub>	8	V
Power dissipation	P <sub>D</sub>	500	mW
Operating temperature	T <sub>opr</sub>	-40~85	°C
Storage temperature	T <sub>stg</sub>	-55~150	°C

## Electrical Characteristics (unless otherwise specified, $V_{CC} = 5\text{ V}$ , $T_a = 25^\circ\text{C}$ )

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	
Power supply	Assured power supply voltage	$V_{CC}$	—	—	4.5	5.0	5.5	V	
	Power supply current	$I_{CC}$	—	SEL = HiZ	26	35	44	mA	
Reference voltage (2VRO)	Reference voltage	2VR	—	—	4.0	4.2	4.4	V	
	Output current	$I_{OH2}$	—	$\Delta V = -0.2\text{ V}$	2.0	—	—	mA	
	Input current	$I_{OL2}$	—	$\Delta V = +0.1\text{ V}$	0.1	—	—		
Reference voltage (VRO)	Reference voltage	VR	—	—	2.0	2.1	2.2	V	
	Reference voltage limit	$\Delta VR$	—	$2 \times VR/2VR - 1$	-3.0	0	3.0	%	
	Output current	$I_{OH1}$	—	$\Delta V = -0.2\text{ V}$	5.0	—	—	mA	
	Input current	$I_{OL1}$	—	$\Delta V = +0.1\text{ V}$	5.0	—	—		
RF1	Frequency band width	$f_c$	—	-3dB point, $R_{IN} = 6\text{ k}\Omega$ Between RFO – RFN2: 33 k $\Omega$	—	8	—	MHz	
	Output slew rate	SR	—	$C_{RFO} = 20\text{ pF}$ , $R_{IN} = 6\text{ k}\Omega$ Between RFO – RFN2: 33 k $\Omega$	—	22	—	V/ $\mu\text{s}$	
	Output offset voltage	$V_{OS}$	—	VR Reference Between RFO – RFN2: 33 k $\Omega$ Input: VR short	—	-100	—	mV	
	Upper limit output voltage	$V_{OH}$	—	GND Reference	3.8	—	—	V	
	Lower limit output voltage	$V_{OL}$	—	GND Reference	—	—	0.9		
	Permissive load resistance	$R_{LM}$	—	—	10	—	—	k $\Omega$	
RF2 (AGC)	Lower limit voltage gain 1 (normal mode)	$G_{v1L}$	—	$f = 1\text{ MHz}$ , RFGC = 0.6 V, GVSW = $V_{CC}$ , GMAD = VR	0.6	0.7	0.8	V/V	
	Upper limit voltage gain 1 (normal mode)	$G_{v1H}$	—	$f = 1\text{ MHz}$ , RFGC = 3.6 V, GVSW = $V_{CC}$ , GMAD = VR	1.3	1.5	1.7		
	Lower limit voltage gain 2 (CD-RW mode)	$G_{v2L}$	—	$f = 1\text{ MHz}$ , RFGC = 0.6 V, GVSW = GND, GMAD = VR	2.7	3.2	3.6		
	Upper limit voltage gain 2 (CD-RW mode)	$G_{v2H}$	—	$f = 1\text{ MHz}$ , RFGC = 3.6 V, GVSW = GND, GMAD = VR	5.8	6.8	7.7		
	Frequency band width (normal mode)	$f_{c1}$	—	-0.5dB point, RFGC = 2.1 V, GVSW = $V_{CC}$ , GMAD = VR	—	12	—	MHz	
	Frequency band width (CD-RW mode)	$f_{c2}$	—	-0.5dB point, RFGC = 2.1 V, GVSW = GND, GMAD = VR	—	12	—		
	Output slew rate	SR	—	$C_{RFGO} = 20\text{ pF}$	—	40	—	V/ $\mu\text{s}$	
	Output offset voltage 1 (normal mode)	$V_{OS1}$	—	VR Reference GMAD = VR Input: Open	GVSW = $V_{CC}$	—	-100	—	mV
	Output offset voltage 2 (CD-RW mode)	$V_{OS2}$	—		GVSW = GND	—	0	—	
	Upper limit output voltage	$V_{OH}$	—	GND Reference	3.7	—	—	V	
	Lower limit output voltage	$V_{OL}$	—	GND Reference	—	—	0.9		
	Permissive load resistance	$R_{LM}$	—	—	10	—	—	k $\Omega$	
	APC	Voltage gain	$G_v$	—	$f = 1\text{ kHz}$	—	200	—	V/V
Operation ref. Voltage		$V_{MDI}$	—	$V_{LDO} = 3.5\text{ V}_{DC}$	170	178	192	mV	
LD off voltage		$V_{LDOP}$	—	SEL = GND, $V_{CC}$ Reference	-0.7	—	—	V	
Input bias current		$I_I$	—	MDI = 178 mV	-200	—	200	nA	

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit		
FE	Voltage gain 1 (normal mode)	Gv1	—	f = 1 kHz R <sub>NF</sub> = 91 kΩ	GVSW = V <sub>CC</sub>	4.3	4.8	5.3	V/V	
	Voltage gain 2 (CD-RW mode)	Gv2	—	R <sub>FI</sub> = 47 kΩ	GVSW = GND	19.3	21.6	23.9		
	Gain balance 1 (normal mode)	GB1	—	f = 1 kHz R <sub>NF</sub> = 91 kΩ	GVSW = V <sub>CC</sub>	-1.0	—	1.0	dB	
	Gain balance 2 (CD-RW mode)	GB2	—	R <sub>FI</sub> = 47 kΩ	GVSW = GND	-1.0	—	1.0		
	Frequency band width	fc	—	-3dB point		—	26.5	—	kHz	
	Output offset voltage 1 (normal mode)	V <sub>OS1</sub>	—	R <sub>NF</sub> = 91 kΩ R <sub>FI</sub> = 47 kΩ	GVSW = V <sub>CC</sub>	-20	—	20	mV	
	Output offset voltage 2 (CD-RW mode)	V <sub>OS2</sub>	—	VR Reference Input: VR short	GVSW = GND	-50	—	50		
	Upper limit output voltage	V <sub>OH</sub>	—	GND Reference		3.8	—	—	V	
	Lower limit output voltage	V <sub>OL</sub>	—	GND Reference		—	—	0.5		
	Permissive load resistance	R <sub>LM</sub>	—	—		10	—	—	kΩ	
TE	Voltage gain 1 (normal mode)	Gv1	—	f = 1 kHz R <sub>FN</sub> = 100 kΩ	GVSW = V <sub>CC</sub>	10.9	12.3	13.5	V/V	
	Voltage gain 2 (CD-RW mode)	Gv2	—	R <sub>TI</sub> = 47 kΩ	GVSW = GND	50	56	60		
	Voltage gain adjustable range	max voltage ratio	ΔGv	—	T <sub>NI</sub> input TEB = VR Reference	TEB = GND	40	45	50	%
		min voltage ratio				TEB = 2VR	-50	-45	-40	
	Gain balance 1 (normal mode)	GB1	—	f = 1 kHz R <sub>NF</sub> = 100 kΩ	GVSW = V <sub>CC</sub>	-1.0	—	1.0	dB	
	Gain balance 2 (CD-RW mode)	GB2	—	R <sub>FI</sub> = 47 kΩ TEB = VR	GVSW = GND	-1.0	—	1.0		
	Frequency characteristic cut-off frequency	fc	—	R <sub>NF</sub> = 100 kΩ -3dB point		—	44	—	kHz	
	Output offset voltage (normal mode)	V <sub>OS1</sub>	—	R <sub>NF</sub> = 100 kΩ R <sub>FI</sub> = 47 kΩ	GVSW = V <sub>CC</sub>	-80	—	80	mV	
	Output offset voltage (CD-RW mode)	V <sub>OS2</sub>	—	VR Reference Input: VR short	GVSW = GND	-300	—	300		
	Upper limit output voltage	V <sub>OH</sub>	—	GND Reference		3.8	—	—	V	
Lower limit output voltage	V <sub>OL</sub>	—	GND Reference		—	—	0.5			
Permissive load resistance	R <sub>LM</sub>	—	—		10	—	—	kΩ		
SBAD	Voltage gain 1 (normal mode)	Gv1	—	f = 1 kHz R <sub>TI</sub> = 47 kΩ	GVSW = V <sub>CC</sub>	2.0	2.7	3.4	V/V	
	Voltage Gain 2 (CD-RW mode)	Gv2	—	TEB = VR	GVSW = GND	9.0	12.2	15.3		
	Frequency Band Width	fc	—	-3dB point		—	44	—	kHz	
	Operation reference voltage 1 (normal mode)	V <sub>OPR1</sub>	—	VR Reference R <sub>TI</sub> = 47 kΩ Input: VR short	GVSW = V <sub>CC</sub>	-1.15	-1.05	-0.95	V	
	Operation reference voltage 2 (CD-RW mode)	V <sub>OPR2</sub>	—		GVSW = GND	-1.0	-0.9	-0.8		
	Upper limit output voltage	V <sub>OH</sub>	—	GND Reference		3.8	—	—	V	
	Lower limit output voltage	V <sub>OL</sub>	—	GND Reference		—	—	1.3		
Permissive load resistance	R <sub>LM</sub>	—	—		10	—	—	kΩ		

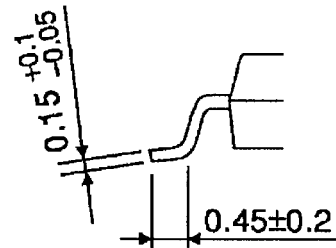
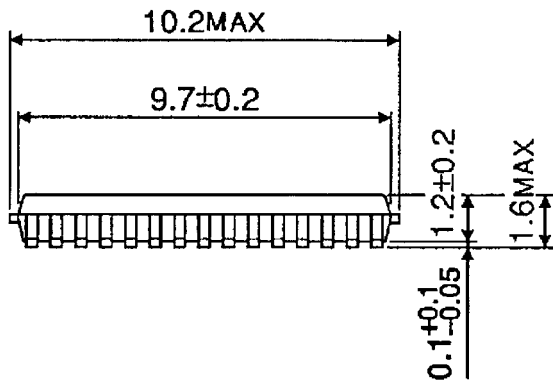
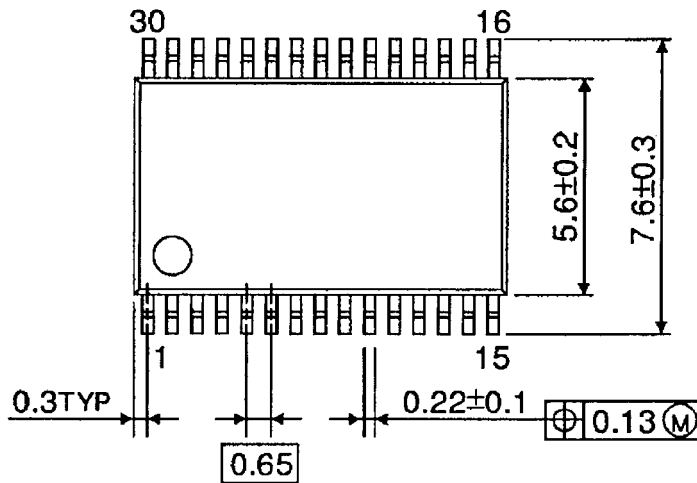
Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
RFRP	Voltage gain	Gv	—	—	—	1.7	—	V/V
	Detection frequency characteristic 1	fc1	—	SEL = HiZ	—	100	—	kHz
	Detection frequency characteristic 2	fc2	—	SEL = V <sub>CC</sub>	—	200	—	
	Operation reference voltage 1	V <sub>OPR1</sub>	—	VR Reference No Input	-1.1	-1.0	-0.9	V
	Operation reference voltage 2	V <sub>OPR2</sub>	—	VR Reference 700 kHz, 1.2 V <sub>p-p</sub>	0.7	0.8	0.9	
	Permissive load resistance	R <sub>LM</sub>	—	—	10	—	—	kΩ
RFCT	Detection frequency characteristic 1	fc1	—	C <sub>BTC</sub> = 0.22 μF	—	70	—	Hz
RFRP → RFCT	Detection frequency characteristic 2	fc2	—	C <sub>PKC</sub> = 0.22 μF	—	70	—	
	Output offset voltage	V <sub>OS</sub>	—	RFRP Reference, RFCT	-50	—	50	mV

Note: If the IC is used abnormally (ex. wrongly mounted), it may be damaged or destroyed.

## Package Dimensions

SSOP30-P-300-0.65

Unit : mm



Weight: 0.17 g (typ.)



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000707EBA

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