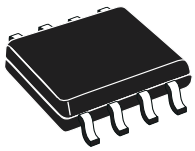
STS8DNH3LL

DUAL N-CHANNEL 30V - 0.018 Ω - 8A SO-8
LOW GATE CHARGE STripFET™ III POWER MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STS8DNH3LL	30 V	<0.022 Ω	8 A

- TYPICAL $R_{DS}(on)$ = 0.018Ω
- OPTIMAL $R_{DS}(on)$ x Qg TRADE-OFF @ 4.5V
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED



SO-8

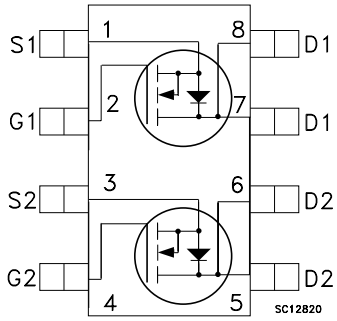
DESCRIPTION

This application specific MOSFET is the Third generation of STMicroelectronis unique "Single Feature Size™" strip-based process. The resulting transistor shows the best trade-off between on-resistance and gate charge. When used as high and low side in buck regulators, it gives the best performance in terms of both conduction and switching losses. This is extremely important for motherboards where fast switching and high efficiency are of paramount importance.

APPLICATIONS

- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY CPU CORE DC/DC CONVERTERS FOR MOBILE PC_S

INTERNAL SCHEMATIC DIAGRAM



Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
STS8DNH3LL	S8DNH3LL	SO-8	TAPE & REEL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	30	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	30	V
V_{GS}	Gate- source Voltage	± 16	V
I_D	Drain Current (continuous) at T_C = 25°C	8	A
I_D	Drain Current (continuous) at T_C = 100°C	5	A
I_{DM}(•)	Drain Current (pulsed)	32	A
P_{tot}	Total Dissipation at T_C = 25°C	2	W

(•) Pulse width limited by safe operating area.

TAB.1 THERMAL DATA

$R_{thj\text{-}amb}$	(*)Thermal Resistance Junction-ambient	Max	62.5	°C/W
T_j	Maximum Operating Junction Temperature		150	°C
T_{stg}	Storage Temperature		-55 to 150	°C

(*) When mounted on 1 inch² FR-4 board, 2 oz of Cu, t ≤ 10s

ELECTRICAL CHARACTERISTICS (T_j = 25 °C unless otherwise specified)

TAB.2 OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	30			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_C = 125°C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 16 V			±100	nA

TAB.3 ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250 µA	1			V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V I_D = 4 A V_{GS} = 4.5 V I_D = 4 A		0.018 0.020	0.022 0.025	Ω Ω

TAB.4 DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	V_{DS}=15 V I_D = 4 A		8.5		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		857 147 20		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

TAB.5 SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 15 V I_D = 4 A R_G = 4.7 Ω V_{GS} = 10 V (Resistive Load, Figure 1)		12 14.5		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}= 15 V I_D= 8 A V_{GS}= 4.5 V (see test circuit, Figure 2)		7.0 2.5 2.3	10	nC nC nC

TAB.6 SWITCHING OFF

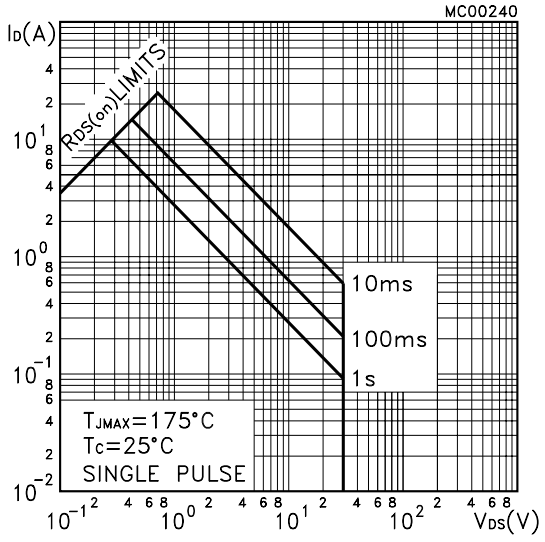
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD} = 15 V I_D = 4 A R_G = 4.7Ω, V_{GS} = 10 V (Resistive Load, Figure 1)		23 8		ns ns

TAB.7 SOURCE DRAIN DIODE

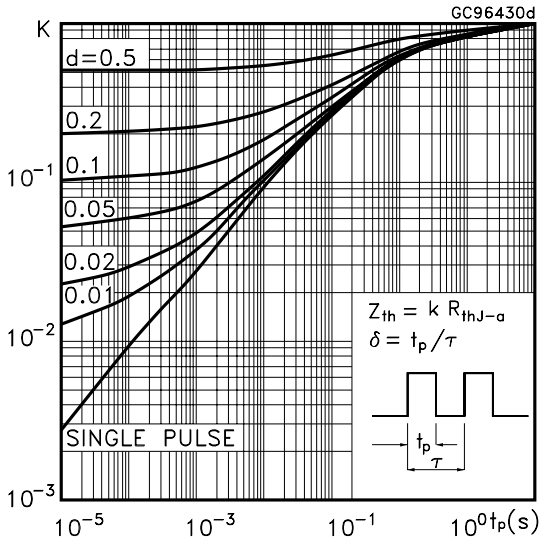
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (•)	Source-drain Current Source-drain Current (pulsed)				8 32	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 4 A V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 8 A di/dt = 100A/µs V_{DD} = 15 V T_j = 150°C (see test circuit, Figure 3)		15 5.7 0.76		ns nC A

(*)Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(•)Pulse width limited by safe operating area.

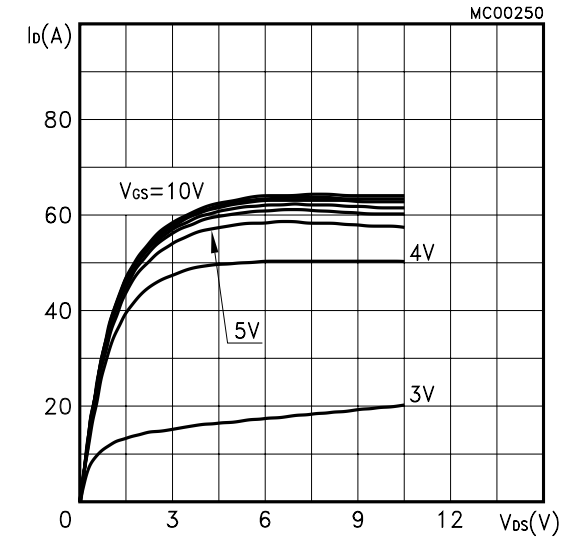
Safe Operating Area



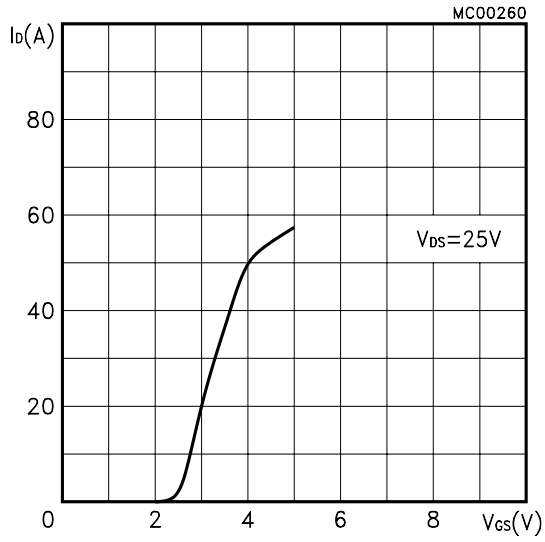
Thermal Impedance



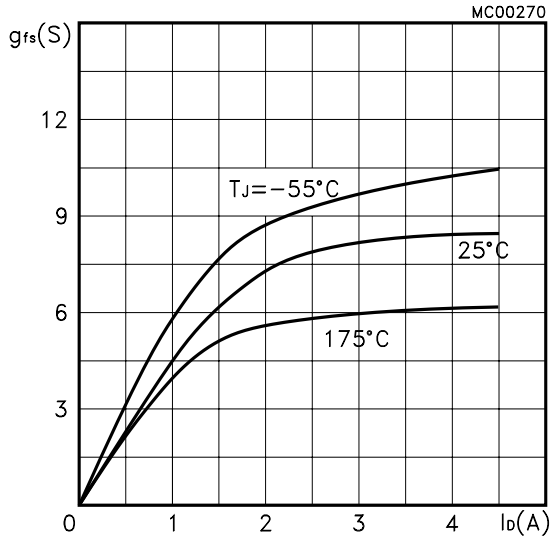
Output Characteristics



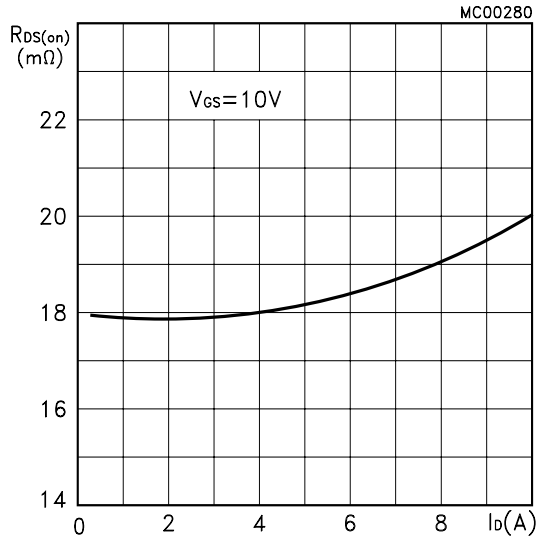
Transfer Characteristics



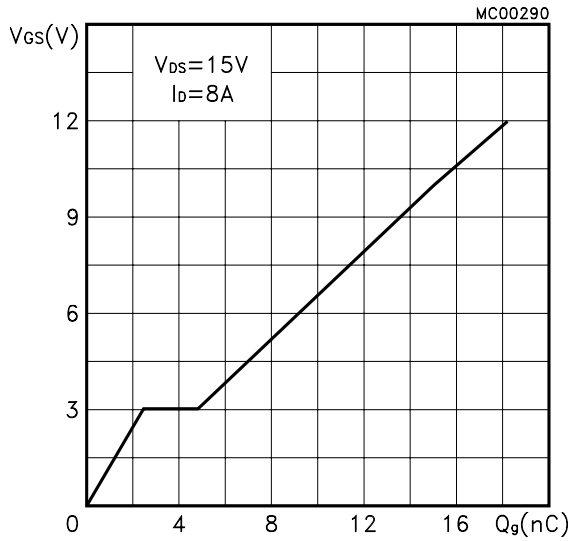
Transconductance



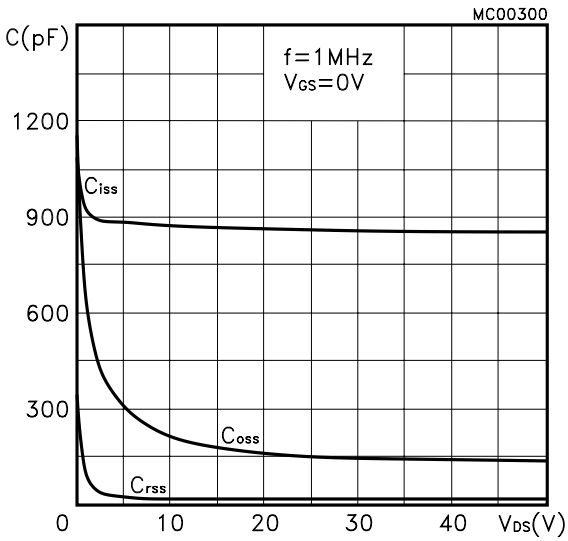
Static Drain-source On Resistance



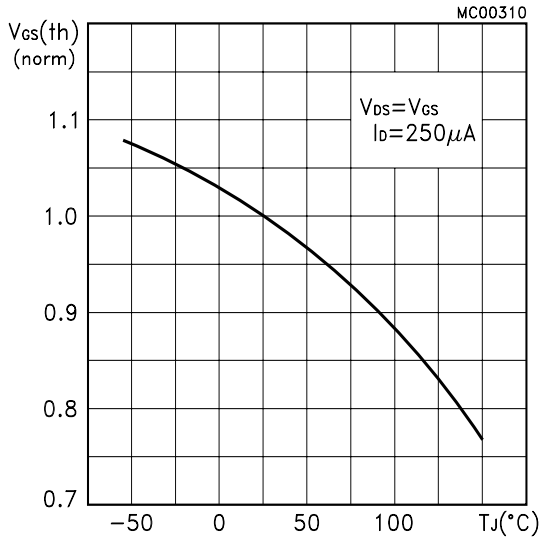
Gate Charge vs Gate-source Voltage



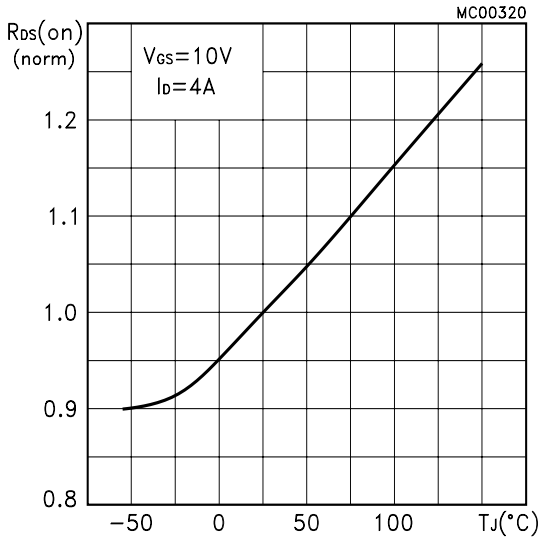
Capacitance Variations



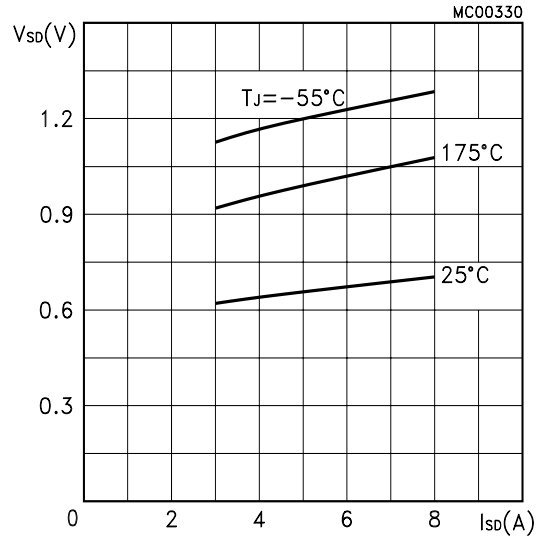
Normalized Gate Threshold Voltage vs Temperature



Normalized on Resistance vs Temperature



Source-drain Diode Forward Characteristics



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Normalized Breakdown Voltage Temperature.

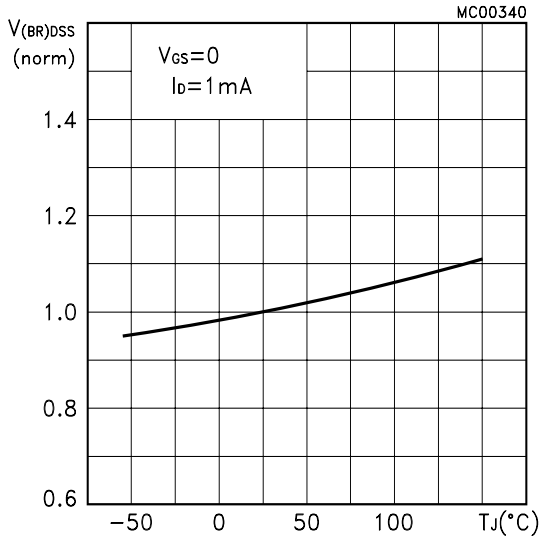

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Fig. 1: Switching Times Test Circuits For Resistive Load

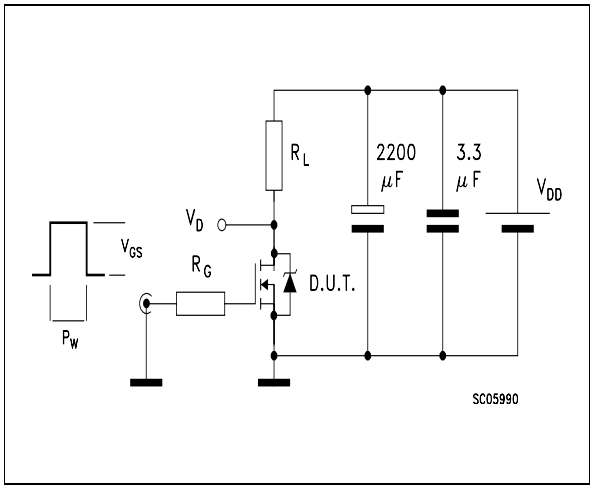


Fig. 2: Gate Charge test Circuit

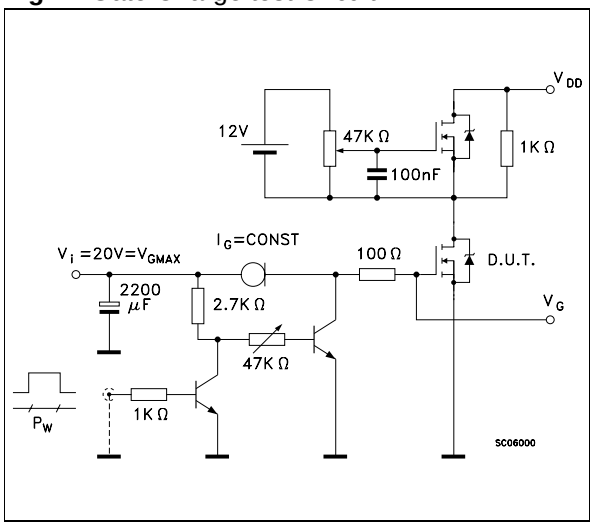
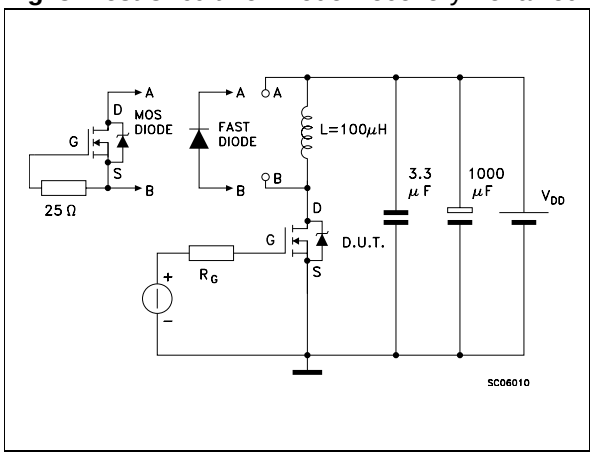
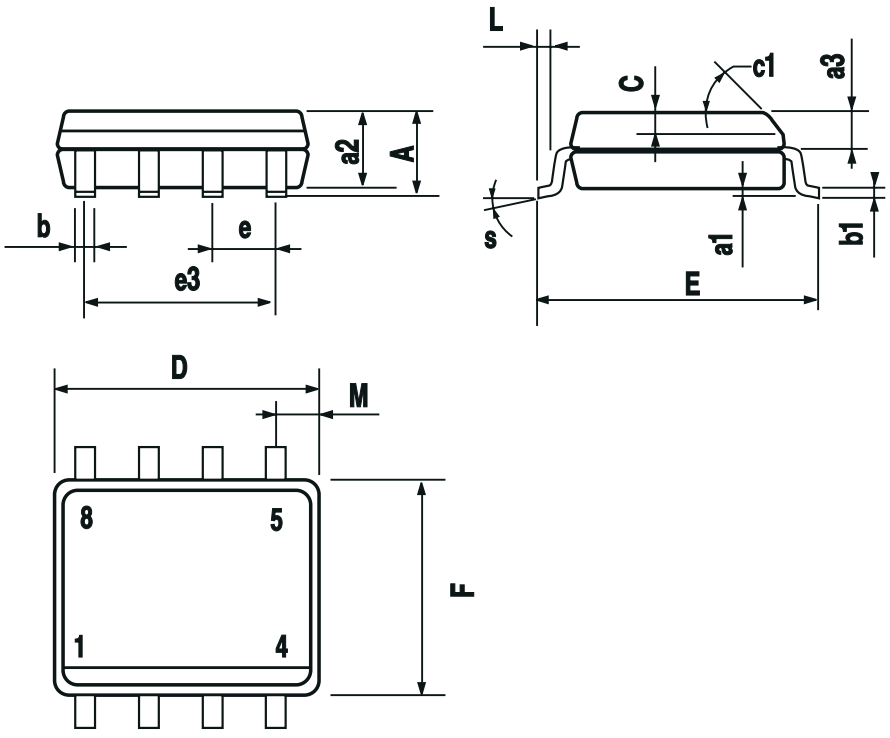


Fig. 3: Test Circuit For Diode Recovery Behaviour



SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



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Revision History

Date	Revision	Description of Changes
Tuesday 15 June 2004	0.2	FIRST ISSUE