

SD200 / SD201 / SD202 / SD203 / SSTSD201 / SSTSD203

FEATURES

- High gain 8.0 dB min @ 1 GHz
- Low Noise 5.0 dB max @ 1 GHz
(SD202, SD203, SSTSD203)
- Low Interelectrode Capacitances

APPLICATIONS

- High Gain VHF/UHF Amplifiers
- Oscillators
- Mixers

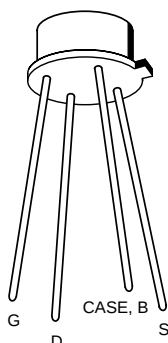
DESCRIPTION

The SD200 series is manufactured utilizing Calogic's proprietary DMOS design and processing techniques. The device is designed to operate well through 1 GHz while maintaining excellent frequency response, power gain, and low noise. The DMOS structure is an inherently low capacitance and very high speed design resulting in a device that bridges JFETS and GaAs products in performance characteristics.

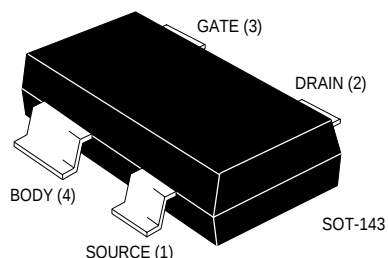
ORDERING INFORMATION

Part	Package	Temperature Range
SD200DC	4 Lead TO-52 Package	-55°C to +125°C
SD201DC	4 Lead TO-52 Package	-55°C to +125°C
SD202DC	4 Lead TO-52 Package	-55°C to +125°C
SD203DC	4 Lead TO-52 Package	-55°C to +125°C
SSTSD201	Surface Mount SOT-143	-55°C to +125°C
SSTSD203	Surface Mount SOT-143	-55°C to +125°C
XSD200	Sorted Chips in Carriers	-55°C to +125°C
XSD201	Sorted Chips in Carriers	-55°C to +125°C
XSD202	Sorted Chips in Carriers	-55°C to +125°C
XSD203	Sorted Chips in Carriers	-55°C to +125°C

PIN CONFIGURATION

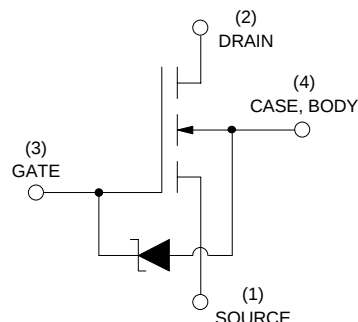


CD10-1 SD201, SD203, zener protected
CD10-2 SD202, SD204, non-zener



PART MARKINGS (SOT-143)	
P/N	MARKING
SSTSD201	201
SSTSD203	203

SCHEMATIC DIAGRAM



BODY INTERNALLY CONNECTED TO CASE.
DIODE PROTECTION ON SD201/SD203 ONLY.

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PARAMETER Breakdown Voltages	SD200	SD201	SD202	SD203	UNIT
V _{DS}	+25	+25	+20	+20	V
V _{DB}	+25	+25	+20	+20	V
V _{GS}	±40	-0.3	±40	-0.3	V
		+20		+20	V
V _{GB}	±40	-0.3	±40	-0.3	V
		+20		+20	V
V _{GD}	±40	-0.3	±40	-0.3	V
		+20		+20	V

I _D	Continuous Drain Current	50 mA
P _T	Power Dissipation (at or below T _C = +25°C)	1.8 W
	Linear Derating Factor	18 mW/°C
P _D	Power Dissipation (at or below T _A = +25°C)	360 mW
	Linear Derating Factor	3.6 mW/°C
T _j	Operating Junction Temperature Range	-55°C to +125°C
T _s	Storage Temperature Range	-65°C to +175°C

SYMBOL	PARAMETER		200, 201			202, 203			UNIT	TEST CONDITIONS	
			MIN	TYP	MAX	MIN	TYP	MAX			
STATIC											
BV _{DS}	Drain-Source Breakdown Voltage		25	30		20	25		V	I _D = 1.0μA, V _{GS} = V _{BS} = 0	
BV _{DB}	Drain-Body Breakdown Voltage		25			20			V	I _D = 1.0μA, V _{GB} = 0 Source OPEN	
I _{D(OFF)}	Drain-Source OFF Current				1.0				μA	V _{DS} = 25 V	V _{GS} = V _{BS} = 0
							1.0	V _{DS} = 20 V			
I _{GBS}	Gate-Body Leakage Current	SD200			±0.1				nA	V _{GV} = ±40 V	V _{DB} = V _{SB} = 0
		SD202					±0.1				
		SD201			1.0				μA	V _{GB} = 20 V	
		SD203					1.0				
V _{GS(th)}	Gate Threshold Voltage		0.1	1.0	2.0	0.1	1.0	2.0	V	V _{DS} = V _{GS} , I _D = 1μA, V _{SB} = 0	
r _{DS(ON)}	Drain-Source ON Resistance			40	70		35	50	ohms	V _{GS} = 5 V, I _D = 1 mA, V _{SB} = 0	
DYNAMIC											
g _{fs}	Common-Source Forward Transcondconductance		13	14		17	20		mS	I _D = 20 mA, V _{DS} = 15 V f = 1 KHz, V _{SB} = 0	
C _{iss}	Common-Source Input Capacitance			2.4	3.0		3.0	3.6	pF	I _D = 20 mA	V _{DS} = 15 V f = 1 MHz V _{SB} = 0
C _{oss}	Common-Source Output Capacitance			1.0	1.2		1.0	1.2		V _{GS} = 0	
C _{rss}	Common-Source Reverse Transfer Capacitance			0.2	0.3		0.2	0.3			
G _{ps}	Common-Source Power Gain		8.0	10		8.0	10		dB		V _{DS} = 15 V f = 1 GHz I _D = 20 mA V _{SB} = 0
NF	Noise Figure			4.5	6.0		4.0	5.0			
P _i	Intercept Point			29			29		dBm	Δf = 2 MHz	