Not Recommended for New Designs
See MPC972 or MPC974

Low Voltage PLL Clock Driver

MPC970

LOW VOLTAGE
PLL CLOCK DRIVER

FA SUFFIX
52–LEAD TQFP PACKAGE
CASE 848D–03

The MPC970 is a 3.3V compatible, PLL based clock driver devices targeted for high performance RISC or CISC processor based systems.

- Fully Integrated PLL
- Output Frequency Up to 250MHz
- Compatible with PowerPC™ and Pentium™ Processors
- Output Frequency Configuration
- On–Board Crystal Oscillator
- 52–Lead TQFP Packaging
- ±50ps Typical Cycle–to–Cycle Jitter

The MPC970 was designed specifically to drive today's PowerPC 601 and Pentium processors while providing the necessary performance to address higher frequency PowerPC 601 as well as PowerPC 603 and PowerPC 604 applications. The 2x_PCLK output can toggle at up to 250MHz while the remaining outputs can be configured to drive the other system clocks for MPC 601 based systems. As the processor based clock speeds increase the processor bus will likely run at one third or even one fourth the processor clock. The MPC970 supports the necessary waveforms to drive the BCLKEN input signal of the MPC 601 when the processor bus is running at a lower frequency than the processor. The MPC970 uses an advanced PLL design which minimizes the jitter generated on the outputs. The jitter specification is well within the requirements of the Pentium processor and meets the stringent preliminary specifications of the PowerPC 603 and PowerPC 604 processors. The application section of this data sheet deals in more detail with driving PowerPC and Pentium processor based systems.

The external feedback option of the MPC970 provides for a near zero delay between the reference clock input and the outputs of the device. This feature is required in applications where a master clock is being picked up off the backplane and regenerated and distributed on a daughter card. The advanced PLL of the MPC970 eliminates the dead zone of the phase detector and minimizes the jitter of the PLL so that the phase error variation is held to a minimum. This phase error uncertainty makes up a major portion of the part–to–part skew of the device.

For single clock driver applications the MPC970 provides an internal oscillator and internal feedback to simplify board layout and minimize system cost. By using the on–board crystal oscillator the MPC970 acts as both the clock generator and distribution chip. The external component is a relatively inexpensive crystal rather than a more expensive oscillator. Since in single board applications the delay between the input reference and the outputs is inconsequential an internal feedback option is offered. The internal feedback simplifies board design in that the system designer need not worry about noise being coupled into the feedback line due to board parasitics and layout. The internal feedback is a fixed divide by 32 of the VCO. This divide ratio ensures that the input crystals will be ≤20MHz, thus keeping the crystal costs down and ensuring availability from multiple vendors.

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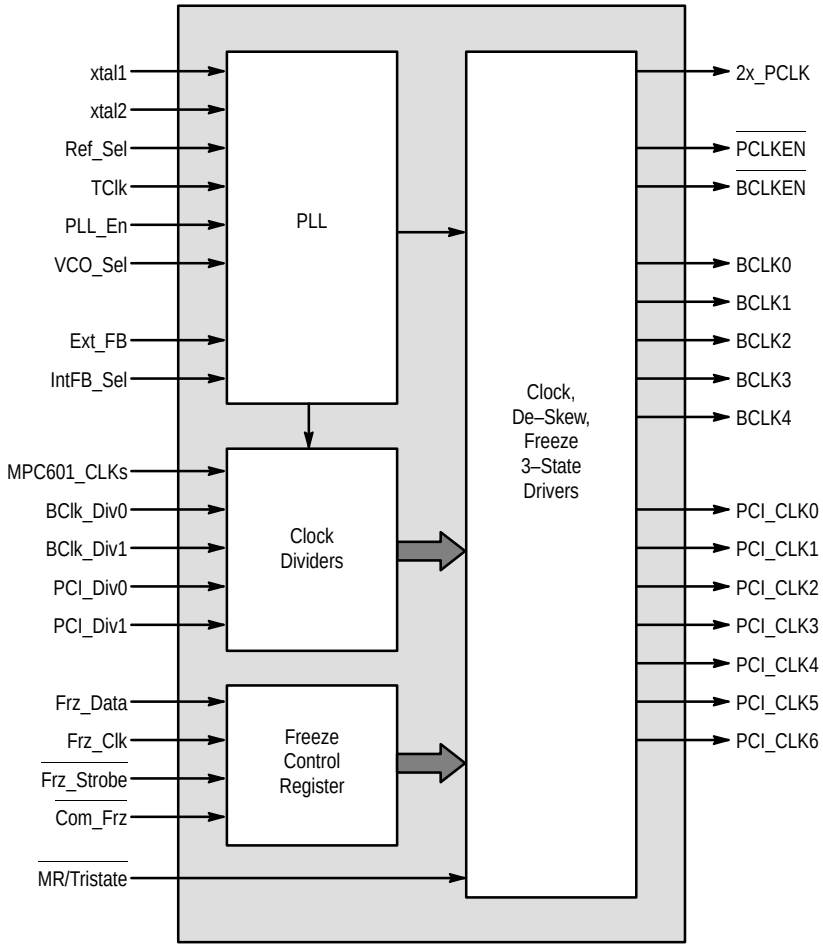


Figure 1. Enable/Disable Scheme

The MPC970 offers a very flexible output enable/disable scheme. This enable/disable scheme helps facilitate system debug as well as provide unique opportunities for system power down schemes to meet the requirements of “green” class machines. The MPC970 allows for the enabling of each output independently via a serial input port or a common enable/disable of all outputs simultaneously via a parallel control pin. When disabled or “frozen” the outputs will be locked in the “LOW” state, however the internal state machines will continue to run. Therefore when “unfrozen” the outputs will activate synchronous and in phase with those outputs which were not frozen. The freezing and unfreezing of outputs occurs only when they are already in the “LOW” state, thus the possibility of runt pulse generation is eliminated. A power–on reset will ensure that upon power up all of the outputs will be active.

For IC and board level testing a $\overline{\text{MR/Tristate}}$ input is provided. When pulled “LOW” all outputs will tristate and all internal flip flops will be reset. In addition the internal PLL can be bypassed and the fanout dividers and output buffers can be driven directly by the TClk input pin. Note that in this mode it will take a number of input clock pulses to cause output transitions as the TClk is fed through the internal dividers.

The MPC970 is fully 3.3V (3.6V for PowerPC 601 designs) compatible and requires no external loop filter components. All inputs accept LVCMOS/LVTTL compatible levels while the outputs provide LVCMOS levels with the capability to drive 50Ω transmission lines. For series terminated lines each MPC970 output can drive two 50Ω lines in parallel thus effectively doubling the fanout of the device.

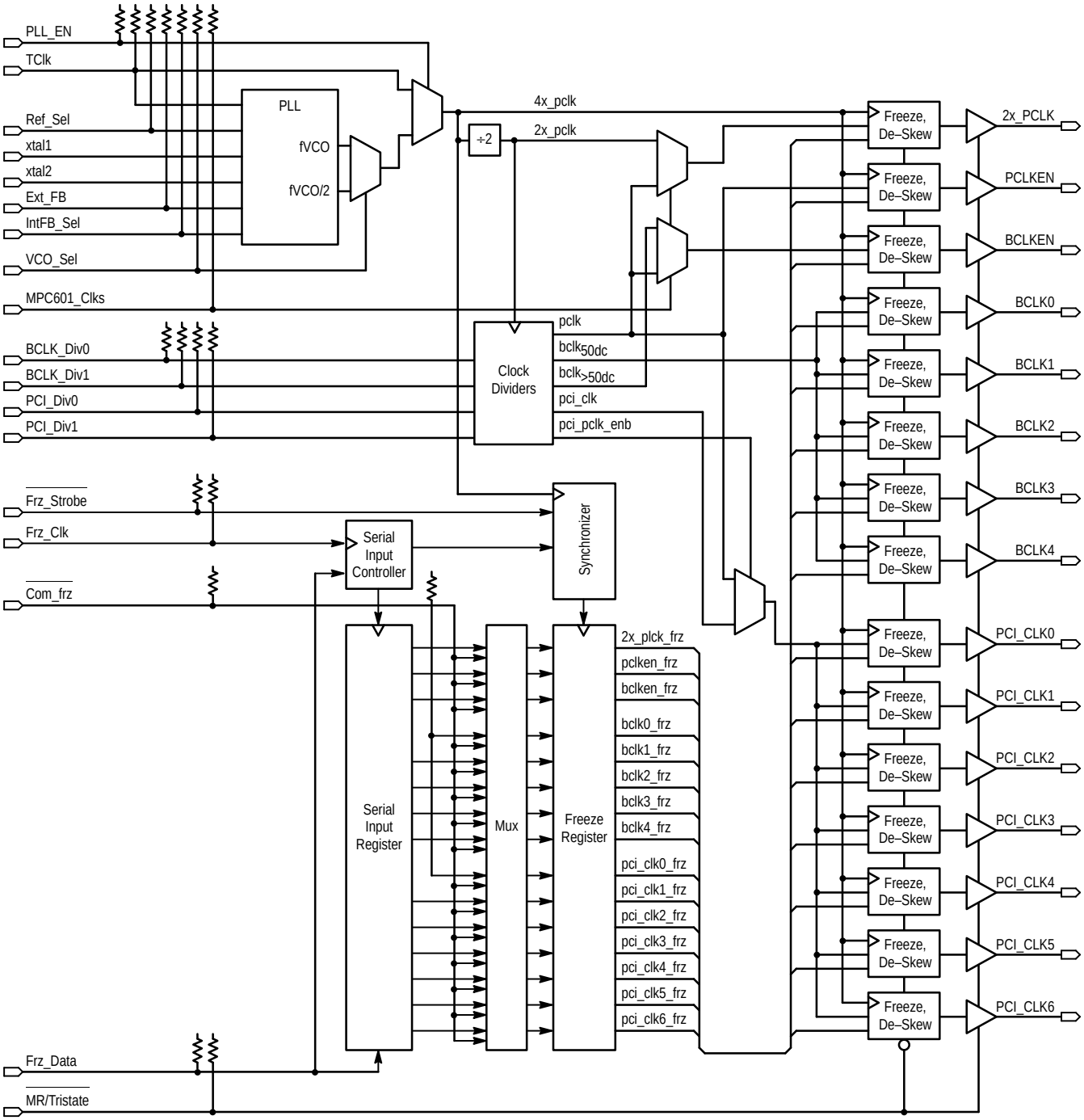


Figure 2. Simplified Block Diagram

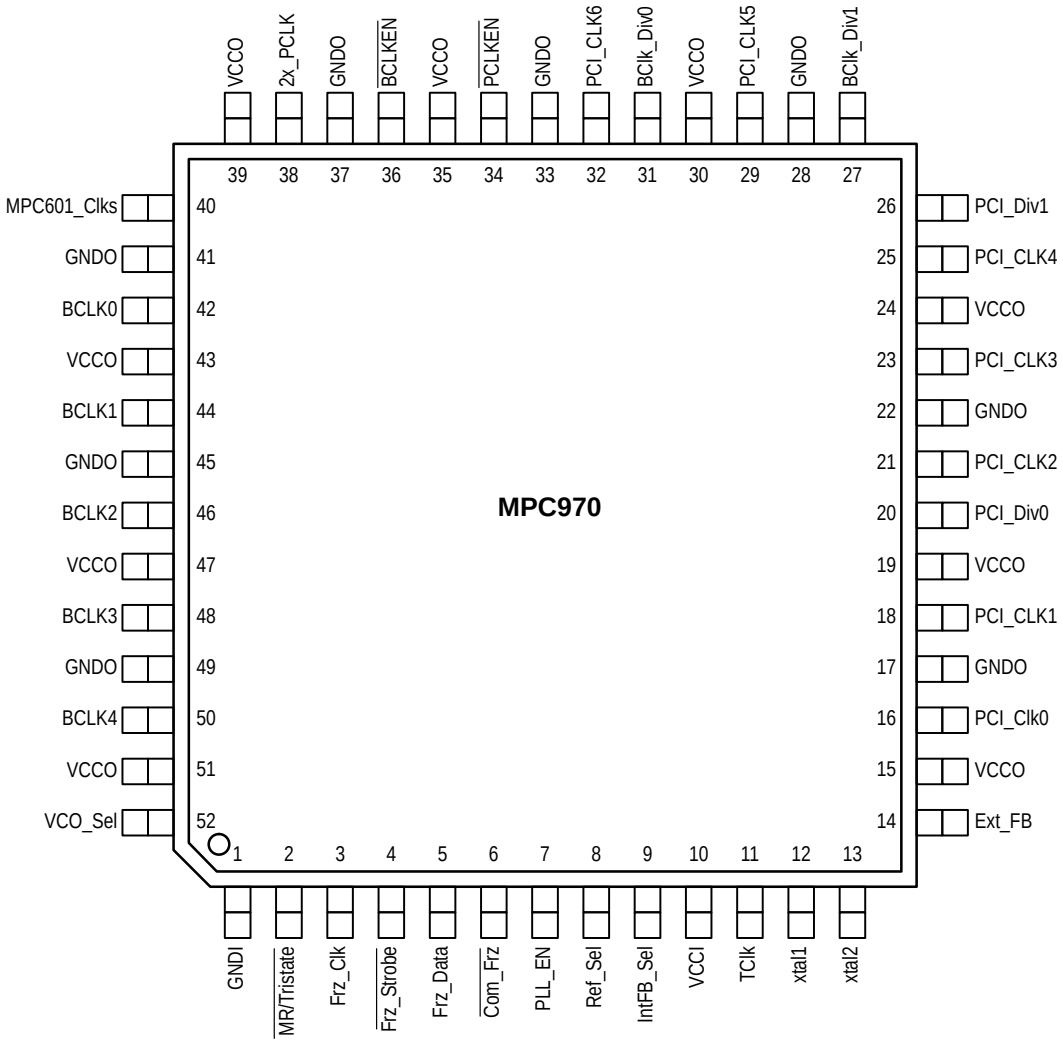


Figure 3. 52–Lead Pinout (Top VIew)

FUNCTION TABLE 1

MPC601_Clks	2x_PCLK	PCLKEN	BCLKEN	BCLK	PCI_CLK
0	VCO/4	VCO/4	VCO/4	X	X
1	VCO/2	VCO/4	BCLK*	X	X

* Output is purposely delayed vs 2x_PCLK output.

FUNCTION TABLE 2

PCI_Div1	PCI_Div0	PCI_CLK	BCLK_Div1	BCLK_Div0	BCLK
0	0	BLCK	0	0	PCLKEN
0	1	BCLK/2	0	1	PCLKEN/2
1	0	BCLK/3	1	0	PCLKEN/3
1	1	PCLKEN	1	1	PCLKEN/4

FUNCTION TABLE 3

Control Pin	Logic ‘0’	Logic ‘1’
VCO_Sel	fVCO/2	fVCO
Ref_Sel	TCLK	Crystal Osc
PLL_En	Bypass PLL	Enable PLL
IntFB_Sel	Ext Feedback	Int Feedback

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

DC CHARACTERISTICS (T_A = 0 to 70°C)

Symbol	Characteristic		Min	Max	Unit	Condition
V_{CC}	Power Supply Voltage		3.0	3.8	V	
I_{CC}	Quiescent Power Supply			250	mA	
V_{IL}	Input Voltage LOW	LVCMOS Inputs		$0.3V_{DD}$	V	
V_{IH}	Input Voltage HIGH	LVCMOS Inputs	$0.7V_{DD}$		V	
I_{IH}	Input Current HIGH	LVCMOS Inputs		–100	µA	$V_{IN} = V_{CC}$
I_{IL}	Input Current LOW		–200		µA	V_{IN} = GND
V_{OH}	Output Voltage HIGH		V_{DD}–0.2		V	I_{OH} = –20mA (Note 1.)
V_{OL}	Output Voltage LOW			0.2	V	I_{OL} = 20mA (Note 1.)
I_{OZ}	Tristate Output Leakage Current		–10	10	µA	$V_{OH} = V_{CC}$ or GND
C_{IN}	Input Capacitance			4	pF	
C_{pd}	Power Dissipation Capacitance				pF	
C_{OUT}	Output Capacitance			8	pF	

1. The MPC970 outputs can drive series or parallel terminated 50Ω (or 50Ω to V_{CC}/2) transmission lines on the incident edge (see Applications Info section).

PLL INPUT REFERENCE CHARACTERISTICS (T_A = 0 to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls		3.0	ns	
f_{ref}	Reference Input Frequency	10	Note 2.	MHz	
f_{refDC}	Reference Input Duty Cycle	25	75	%	

2. Maximum input reference is limited by the VCO lock range and the feedback divider.

AC CHARACTERISTICS (T_A = 0 to 70°C)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
f_{Xtal}	Crystal Oscillator Frequency	10		25	MHz	Note 3.
F_{out}	Maximum 2x_PCLK Output Frequency			200	MHz	Note 4.
t_{DC}	Output Duty Cycle (Notes 4., 5.)	45 35		55 65	%	F_{out} < 200MHz F_{out} ≥ 200MHz
$V_{OH}AC$	AC Output HIGH Voltage	2.4 2.2			V	F_{out} < 200MHz F_{out} ≥ 200MHz
$V_{OL}AC$	AC Output LOW Voltage			0.4 0.6	V	F_{out} < 200MHz F_{out} ≥ 200MHz
t_{pw}	2x_PCLK Pulse Width (Notes 4., 5.)	1.75	2.27		ns	F_{out} = 200MHz
t_{per}	Minimum Clock Out Period	4.85	4.91		ns	F_{out} = 200MHz
f_{VCO}	VCO Lock Range	200		700	MHz	
t_{jitter}	Output Jitter (Notes 4., 5.)		±50 110 76	±100 190 210	ps	PLL Jitter 2x_P Period Variation Period Variation (Other)
t_{skew}	Output–to–Output Skew (Notes 4., 5.) 2x_PCLCK, PCLKEN, BCLKEN, BCLK 2x_PCLK, PCLKEN, BCLK PCI_CLK BCLK All			 550 550 450 550 800	ps	 MPC601_Clks = ‘0’ MPC601_Clks = ‘1’
t_{delay}	Propagation Delay 2x_PCLK to BCLKEN	100		850	ps	MPC601_Clks = ‘1’
t_r, t_f	Output Rise/Fall Time (Notes 4., 5.)	0.15		1.5	ns	0.8 to 2.0V
t_{lock}	PLL Lock Time			10	ms	
t_{PZL}	Output Enable Time $\overline{MR}$/Tristate to Outputs			8	ns	
t_{PHZ}, t_{PLZ}	Output Disable Time $\overline{MR}$/Tristate to Outputs			10	ns	
f_{MAX}	Maximum Frz_Clk Frequency			20	MHz	
t_s	Setup Time Frz_Data to Frz_Clk Com_Frz to Frz_Strobe	8 5				
t_h	Hold Time Frz_Clk to Frz_Data Frz_Strobe to Com_Frz	8 5				

3. See Applications Info section for more crystal information.
4. Drive 50Ω transmission lines.
5. Measured at 1.4V.

DETAILED PIN DESCRIPTIONS

The following gives a brief description of the functionality of the MPC970 I/O. Unless explicitly stated all inputs are LVCMOS/LVTTL compatible with internal pull up resistors. All outputs are LVCMOS level outputs which are capable of driving two series terminated 50Ω transmission lines on the incident edge.

xtal1, xtal2

For the MPC970 the xtal1 and xtal2 pins represent the external crystal connections to the internal oscillator. The crystal oscillator is completely self contained, there are no external components required. The oscillator is specified to function for crystals of up to 50MHz. Exact crystal specifications are outlined in the applications section.

VCO_Sel

The VCO_Sel pin allows the user to further divide the internal VCO frequency for the generation of lower frequencies at the outputs. The VCO_Sel pin should be used to set the VCO into its most optimum range. Refer to the applications section for more details on the VCO frequency range. A logic '1' on the VCO_Sel pin will bypass the internal ÷2.

TClk

The TClk input serves a dual purpose; it can be used as either a reference clock input for the PLL from an external frequency source or it can be used as a board level test clock in the PLL bypass mode.

PLL_En

The PLL_En pin allows the TClk input to be routed around the PLL for system test and debug. When pulled low the MPC970 will be placed in the test mode. Note that the TClk input will be routed through the divider chain. For instance in the PowerPC 601 microprocessor clock generation mode the TClk input will toggle twice for each toggle on the 2x_PCLK output. Depending on the states of the frequency divider select pins this ratio may be higher.

Frz_Data

Frz_Data is the serial data input for the output freeze function of the device. Refer to the applications section for more information on the freeze functionality.

Frz_Clk

Frz_Clk is the serial freeze logic clock input. Refer to the applications section for more information on the freeze functionality.

$\overline{\text{Frz\_Strobe}}$

The Frz_Strobe input is used to freeze or unfreeze all of the outputs simultaneously. Refer to the applications section for more information on the freeze functionality.

$\overline{\text{Com\_Frz}}$

The Com_Frz input allows the user to enable/disable all of the outputs with the control of a single pin. The action will take place upon a high to low transition of the Frz_Strobe input.

BClk_Div0:1

The BClk_Div inputs are used to program the VCO divide ratio for the BCLK outputs. These inputs also set the divide ratio of the BCLKEN output to be equal in frequency to the BCLK outputs when the device is in the MPC601_Clks mode. The BClk_Div inputs set the frequency as follows:

BClk_Div1	BClk_Div0	BCLK Frequency
0	0	PCLKEN
0	1	PCLKEN/2
1	0	PCLKEN/3
1	1	PCLKEN/4

In most applications these inputs will be strapped to the appropriate power rails.

PCI_Div0:1

The PCI_Div inputs set the division ratio for the PCI_CLKs. The PCI_CLKs are set relative to the BCLK or the PCLKEN output such that you can upgrade the processor bus and maintain the PCI bus frequency in the currently defined ≤ 33MHz range. The PCI_Div inputs set the PCI_CLKs as follows:

PCI_Div1	PCI_Div0	PCI_CLK Frequency
0	0	BCLK
0	1	BCLK/2
1	0	BCLK/3
1	1	PCLKEN

In a typical application these inputs will be strapped to the appropriate power rail.

MPC601_Clks

The MPC601_Clks input will configure the outputs to drive the PowerPC 601 microprocessor when pulled HIGH or left open. When pulled LOW it will configure the 2xPCLK, PCLKEN and BCLKEN all into a VCO/4 mode. In this mode the MPC970 will have three more outputs available to drive clock loads on the processor bus for PowerPC 603, PowerPC 604 or Pentium microprocessor based systems.

Ext_FB

The Ext_FB pin is an input to the phase detector of the PLL which is tied to an external feedback output. Typically this feedback will be one of the lowest frequency outputs of the MPC970.

IntFB_Sel

The IntFB_Sel input selects whether the internal feedback signal or an external feedback signal is routed to the phase detector of the PLL. The default mode, pulled HIGH via the internal pull up resistor, is to select the internal feedback.

MR/Tristate

The MR/Tristate input when pulled LOW will reset all of the internal flip flops and also tristate all of the clock outputs. This input is used primarily for IC and board level test.

Ref_Sel

The Ref_Sel input allows the user to choose between two sources for the PLL reference frequency. For the MPC970, LOW on Ref_Sel will choose the LVCMOS TCLK input. For the MPC970, a HIGH on Ref_Sel will choose the crystal oscillator input.

2x_PCLK

In general the outputs are named based on the implementation in a PowerPC 601 microprocessor based system. In the MPC601_Clk mode the 2x_PCLK will run at half the internal VCO frequency. With a maximum internal VCO frequency of 1000MHz this output could theoretically toggle at 500MHz, in practice however the output can toggle only as fast as 300MHz. This frequency will be required on future enhancements to the MPC 601 microprocessor. When the MPC970 is taken out of the MPC601_Clk mode the 2xPCLK will run at a VCO/4 frequency. This divide ratio will place this output frequency in the present and future processor bus speeds of the PowerPC 603, PowerPC 604 and Pentium microprocessors. The 2x_PCLK output is a 50% duty cycle LVCMOS output.

PCLKEN

The PCLKEN output is designed to drive the PCLKEN input of the PowerPC 601 microprocessor when the MPC970 is in the MPC601_Clk mode. The PCLKEN output frequency is one half that of the 2x_PCLK output, a divide by four of the internal VCO. The PCLKEN output runs at the same frequency regardless of the state of the frequency divide controls. The toggle frequency of this output is well placed for driving the PowerPC 603, PowerPC 604 and Pentium processor buses. The PCLKEN output is a 50% duty cycle LVCMOS output.

BCLKEN

The BCLKEN output is designed to drive the BCLKEN input of the PowerPC 601 microprocessor when the MPC970 is in the MPC601_Clks mode. The BCLKEN toggles at the same frequency as the BCLK outputs as described earlier. However when the BCLKEN output is a divide by three or a divide by four of the PCLKEN output the duty cycle is 66/33 and 75/25 respectively per the requirement of the MPC 601 processor. In addition to meet the HOLD time spec for the BCLKEN input of the MPC 601 the BCLKEN output of the MPC970 lags the 2xPCLK output by no less than 100ps. When the MPC970 is not in the MPC601_Clks mode the BCLKEN output is set at a fixed divide by four from the internal VCO. In addition in this mode the BCLKEN output does NOT lag the other outputs, but rather is synchronous within the Output–to–Output skew spec of the device.

BCLK0:4

The BCLK outputs are designed to drive the clock loads on the processor bus of either the PowerPC or Pentium microprocessors. The most common practice in “non MPC 601” applications will be to place these outputs in the PCLKEN/1 mode and combine them with the above outputs to drive all of the loads on the processor bus. The division ratios do allow for the swap of these outputs with the PCI_CLK outputs if more clocks are needed to drive the processor bus. For PowerPC 601 microprocessor based systems the division ratios allow the processor internal speeds to be increased while maintaining reasonable speeds for the L2 cache and the PCI bridge chip. The BCLK outputs are 50% duty cycle LVCMOS outputs.

PCI_Clk0:6

As the name would suggest the PCI_CLK outputs are designed to drive the PCI bus clock loads in a typical microprocessor based system. The division ratios allow for these outputs to remain in the ≤ 33MHz PCI bus speeds for various common processor bus speeds as well as higher future processor bus speeds. These outputs can also be programmed to run at the processor bus speeds if more processor bus clocks are required. The PCI_CLK outputs are 50% duty cycle LVCMOS outputs.

APPLICATIONS INFORMATION

Programming the MPC970

The MPC970 is very flexible in the programming of the frequency relationships of the various outputs as well as the relationships between the input references and outputs. The purpose of this section is to outline the various relationships. Although not exhaustive the hope is that enough information is supplied to allow the customers to tailor the I/O relationships for their specific applications.

The VCO used in the MPC970 is a differential ring oscillator. The VCO exhibits a very wide frequency range to allow for a great deal of flexibility to the end user. Special design techniques were used in the overall PLL design to keep the relatively high gain of the VCO from significantly impacting the jitter of the PLL.

Table 1 tabulates the various output frequencies for the different modes defined by the division select input pins. In this table the VCO_Sel pin is high so that the ÷2 prescaler is bypassed. Note that the ÷32 feedback is always fed directly from the VCO and is thus unaffected by the level on the VCO_Sel input. Table 1 shows each of the output frequencies as a function of the VCO frequency. The two VCO ranges can be used to plug in values to get the actual frequencies. When the internal feedback option is used the multiplication factor of the device will equal 32 divided by the

output divide ratio. If the VCO_Sel pin is “LOW” the multiplication factor will be reduced further by 2. (See “Using the On–Board Crystal Oscillator” section of this datasheet.)

Using the External Feedback Feature of the MPC970/71

In applications where the relationship between the output waveforms and the input waveforms are critical the external feedback option will likely be used. Table 1 and Table 2 are still appropriate for establishing the potential output frequency relationships. The input reference frequency for external feedback applications will be equal to the frequency of the feedback signal. As a result the use of the external feedback yields a number of potential input to output frequency multiplication factors which are not available using the internal feedback. Using the external feedback the device can function as a zero delay buffer and could multiply the input from 4 to as much as 48. In practice however the multiplication factor is limited by the loop dynamics of the PLL. The MPC970 PLL was optimized for an input reference frequency or greater than 10MHz. Frequencies lower than 10MHz will tend to pass through the filter and add jitter to the PLL. In addition the PLL was optimized for feedback divide ratios of between 8 and 64. The user should avoid using the device with feedback divide ratios outside of this range. For the external feedback case the feedback divide ratio will include the ÷2 (if VCO_Sel is LOW) plus the output divider for the feedback output. If, for instance the MPC970 is to be used as a zero delay buffer the VCO_Sel pin should be pulled LOW and all of the outputs should be set in a VCO/4 mode. This would produce a feedback ratio of ÷8. Several potential configurations using the external feedback are pictured in Figure 4 through Figure 7.

The external feedback option of the MPC970 is critical for applications in which more than one clock driver need to be synchronized. The external feedback option ensures that the feed through delay is the same as the feedback delay. This functionality removes propagation delay variation as a factor in the determination of part to part skew. The low jitter PLL used in the MPC970 has a near zero deadband phase detector and very little part to part variability. The result is a very low phase error variability in the product. When coupled with the output to output skew the phase error variability accounts for the part to part skew of the device. From the specification table one sees that the worst case part to part skew of the device is 800ps, assuming that there is zero skew in the multiple reference inputs. For multiple MPC970 applications if the lowest generated output frequency is used as the feedback signal the devices will be guaranteed to be synchronized. For applications where the lowest frequency is not used as the reference or where the internal feedback is used there is no way to guarantee that the multiple devices will be phase synchronized.

Table 1. Programmable Output Frequency Relationships (MPC601_Clks = ‘HIGH’; VCO_Sel = ‘HIGH’)

INPUTS				OUTPUTS				
PCI_Div1	**PCI_Div0**	**BCLK_Div1**	**BCLK_Div0**	**2x_PCLK**	**PCLKEN**	**BCLKEN***	**BCLK**	**PCI_CLK**
0	0	0	0	VCO/2	VCO/4	VCO/4	VCO/4	VCO/4
0	0	0	1	VCO/2	VCO/4	VCO/8	VCO/8	VCO/8
0	0	1	0	VCO/2	VCO/4	VCO/12	VCO/12	VCO/12
0	0	1	1	VCO/2	VCO/4	VCO/16	VCO/16	VCO/16
0	1	0	0	VCO/2	VCO/4	VCO/4	VCO/4	VCO/8
0	1	0	1	VCO/2	VCO/4	VCO/8	VCO/8	VCO/16
0	1	1	0	VCO/2	VCO/4	VCO/12	VCO/12	VCO/24
0	1	1	1	VCO/2	VCO/4	VCO/16	VCO/16	VCO/32
1	0	0	0	VCO/2	VCO/4	VCO/4	VCO/4	VCO/12
1	0	0	1	VCO/2	VCO/4	VCO/8	VCO/8	VCO/24
1	0	1	0	VCO/2	VCO/4	VCO/12	VCO/12	VCO/36
1	0	1	1	VCO/2	VCO/4	VCO/16	VCO/16	VCO/48
1	1	0	0	VCO/2	VCO/4	VCO/4	VCO/4	VCO/4
1	1	0	1	VCO/2	VCO/4	VCO/8	VCO/8	VCO/4
1	1	1	0	VCO/2	VCO/4	VCO/12	VCO/12	VCO/4
1	1	1	1	VCO/2	VCO/4	VCO/16	VCO/16	VCO/4

* BCLK_En output is delayed relative to other outputs

Table 2. Programmable Output Frequency Relationships (MPC601_Clks = 'LOW'; VCO_Sel = 'HIGH')

INPUTS				OUTPUTS				
PCI_Div1	**PCI_Div0**	**BCLK_Div1**	**BCLK_Div0**	**2x_PCLK**	**PCLKEN**	**BCLKEN***	**BCLK**	**PCI_CLK**
0	0	0	0	VCO/4	VCO/4	VCO/4	VCO/4	VCO/4
0	0	0	1	VCO/4	VCO/4	VCO/4	VCO/8	VCO/8
0	0	1	0	VCO/4	VCO/4	VCO/4	VCO/12	VCO/12
0	0	1	1	VCO/4	VCO/4	VCO/4	VCO/16	VCO/16
0	1	0	0	VCO/4	VCO/4	VCO/4	VCO/4	VCO/8
0	1	0	1	VCO/4	VCO/4	VCO/4	VCO/8	VCO/16
0	1	1	0	VCO/4	VCO/4	VCO/4	VCO/12	VCO/24
0	1	1	1	VCO/4	VCO/4	VCO/4	VCO/16	VCO/32
1	0	0	0	VCO/4	VCO/4	VCO/4	VCO/4	VCO/12
1	0	0	1	VCO/4	VCO/4	VCO/4	VCO/8	VCO/24
1	0	1	0	VCO/4	VCO/4	VCO/4	VCO/12	VCO/36
1	0	1	1	VCO/4	VCO/4	VCO/4	VCO/16	VCO/48
1	1	0	0	VCO/4	VCO/4	VCO/4	VCO/4	VCO/4
1	1	0	1	VCO/4	VCO/4	VCO/4	VCO/8	VCO/4
1	1	1	0	VCO/4	VCO/4	VCO/4	VCO/12	VCO/4
1	1	1	1	VCO/4	VCO/4	VCO/4	VCO/16	VCO/4

* BCLK_En output is coincident with other outputs

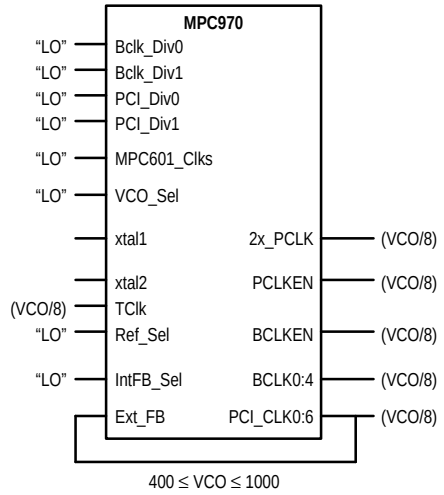


Figure 4. External Feedback Configuration 1

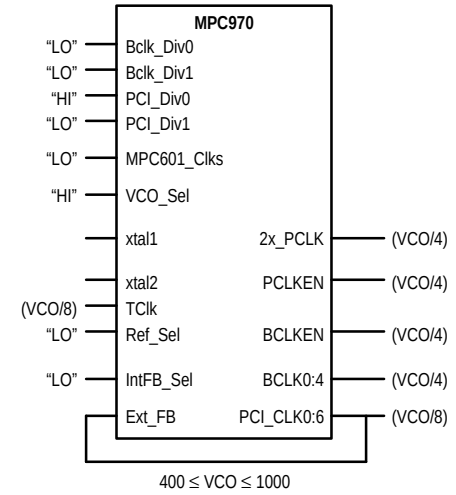


Figure 5. External Feedback Configuration 2

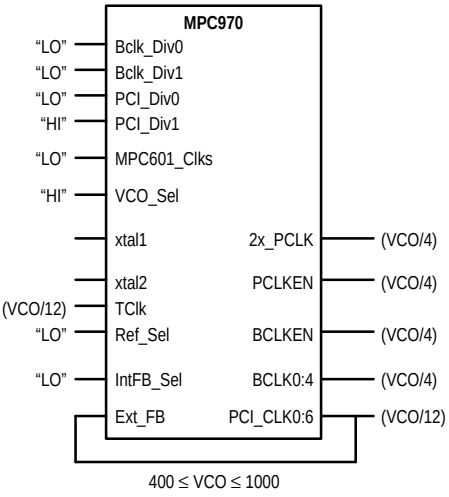


Figure 6. External Feedback Configuration 3

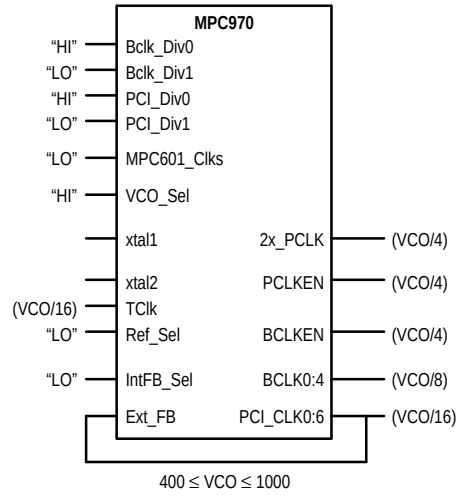


Figure 7. External Feedback Configuration 4

Using the On–Board Crystal Oscillator

The MPC970 features an on–board crystal oscillator to allow for seed clock generaytion as well as final distribution. The on–board oscillator is completely self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC970 as possible to avoid any board level parasitics. To facilitate co–location surface mount crystals are recommended, but not required. In addition, with crystals with a higher shunt capacitance, it may be necessary to place a 1k resistor across the two crystal leads.

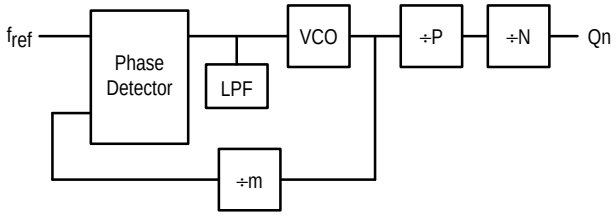
The oscillator circuit is a series resonant circuit as opposed to the more common parallel resonant circuit, this eliminates the need for large on–board capacitors. Because the design is a series resonant design for the optimum frequency accuracy a series resonant crystal should be used (see specification table below). Unfortunately most off the shelf crystals are characterized in a parallel resonant mode. However a parallel resonant crystal is physically no different than a series resonant crystal, a parallel resonant crystal is simply a crystal which has been characterized in its parallel resonant mode. Therefore in the majority of cases a parallel specified crystal can be used with the MPC970 with just a minor frequency error due to the actual series resonant frequency of the parallel resonant specified crystal. Typically a parallel specified crystal used in a series resonant mode will exhibit an oscillatory frequency a few hundred ppm lower than the specified value. For most processor implementations a few hundred ppm translates into kHz inaccuracies, a level which does not represent a major issue.

Table 3. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental at Cut
Resonance	Series Resonance*
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80Ω
Correlation Drive Level	100µW
Aging	5ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

The MPC970 is a clock driver which was designed to generate outputs with programmable frequency relationships and not a synthesizer with a fixed input frequency. As a result the crystal input frequency is a function of the desired output frequency. For a design which utilizes the external feedback to the PLL the selection of the crystal frequency is straight forward; simply chose a crystal which is equal in frequency to the fed back signal. To determine the crystal required to produce the desired output frequency for an application which utilizes internal feedback the block diagram of Figure 8 should be used. The P and the M values for the MPC970 are also included in Figure 8. The M values can be found in the configuration tables included in this applications section.



$$f_{ref} = \frac{f_{VCO}}{m}, \quad f_{VCO} = fQn \cdot N \cdot P$$

$$\therefore\ f_{ref} = \frac{fQn \cdot N \cdot P}{m}$$

m = 32
P = 1 (VCO_Sel=‘1’), 2(VCO_Sel=‘0’)

Figure 8. PLL Block Diagram

For the MPC970 clock driver, the following will provide an example of how to determine the crystal frequency required for a given design.

Given:

2x_PCLK = 200MHz
PCLKEN = 100MHz
BCLK = 50MHz
PCI_CLK = 25MHz
VCO_SEL = ‘1’

$$f_{ref} = \frac{fQn \cdot N \cdot P}{m}$$

From Table 3

PCI_CLK = VCO/16 then N = 16
or
PCLKEN = VCO/4 then N = 4

From Figure 8

m = 32 and P = 1

$$f_{ref} = \frac{25 \cdot 16 \cdot 1}{32} = 12.5\text{MHz} \text{ or } \frac{100 \cdot 4 \cdot 1}{32} = 12.5\text{MHz}$$

Driving Transmission Lines

The MPC970 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions brochure (BR1333/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel

terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC970 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 9 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC970 clock driver is effectively doubled due to its capability to drive multiple lines.

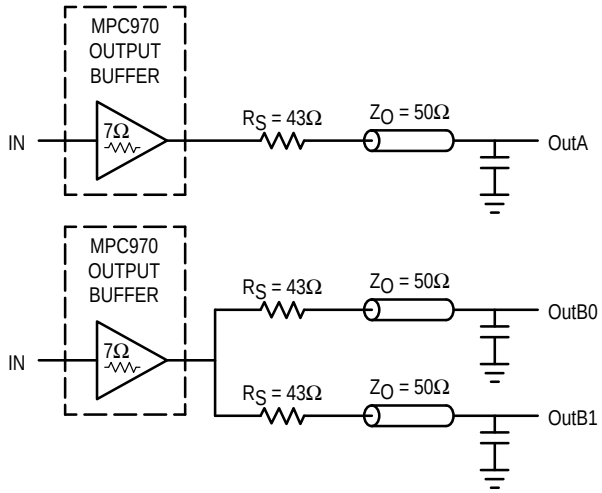


Figure 9. Single versus Dual Transmission Lines

The waveform plots of Figure 10 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC970 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC970. The output waveform in Figure 10 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$VL = VS (Zo / Rs + Ro + Zo) = 3.0 (25/53.5) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 11 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

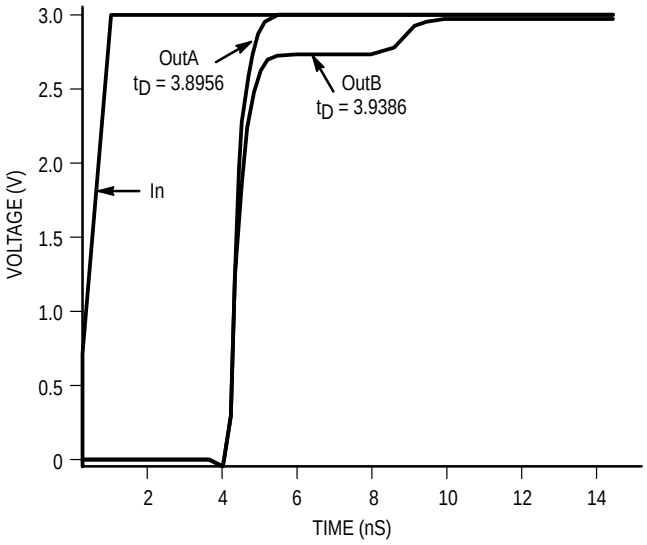
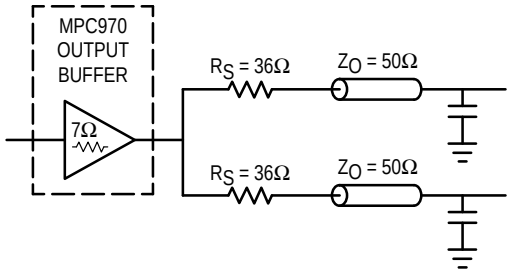


Figure 10. Single versus Dual Waveforms



$$7\Omega + 36\Omega \parallel 36\Omega = 50\Omega \parallel 50\Omega$$
$$25\Omega = 25\Omega$$

Figure 11. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

Using the Output Freeze Circuitry

With the recent advent of a “green” classification for computers the desire for unique power management among system designers is keen. The individual output enable control of the MPC970 allows designers, under software control, to implement unique power management schemes into their designs. Although useful, individual output control at the expense of one pin per output is too high, therefore a simple serial interface was derived to economize on the control pins.

The freeze control logic provides two mechanisms through which the MPC970 clock outputs may be frozen (stopped in the logic ‘0’ state):

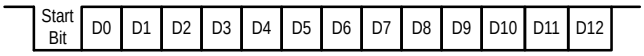
The first freeze mechanism allows serial loading of the 13–bit Serial Input Register, this register contains one programmable freeze enable bit for 13 of the 15 output clocks. The BCLK0 and PCI_CLK0 outputs cannot be frozen with the serial port, this avoids any potential lock up situation

should an error occur in the loading of the Serial Input Register. The user may programmably freeze an output clock by writing logic ‘0’ to the respective freeze enable bit. Likewise, the user may programmably unfreeze an output clock by writing logic ‘1’ to the respective enable bit.

The second freeze mechanism allows all 15 clocks to be frozen simultaneously by placing a logic ‘0’ on the Com_Frz input and then issuing a low going pulse on the Frz_Strobe input. Likewise, all 15 clocks can be simultaneously unfrozen by placing logic ‘1’ on the Com_Frz input and then issuing a low–going pulse on the Frz_Strobe input. Note that all 15 clocks are affected by the Frz_Strobe freeze logic.

The freeze logic will never force a newly–frozen clock to a logic ‘0’ state before the time at which it would normally transition there. The logic simply keeps the frozen clock at logic ‘0’ once it is there. Likewise, the freeze logic will never force a newly–unfrozen clock to a logic ‘1’ state before the time at which it would normally transition there. The logic re–enables the unfrozen clock during the time when the respective clock would normally be in a logic ‘0’ state, eliminating the possibility of ‘runt’ clock pulses.

The user may write to the Serial Input register through the Frz_Data input by supplying a logic ‘0’ start bit followed serially by 13 NRZ freeze enable bits. After the 13th freeze enable bit the Frz_Data signal must be left in (or returned to) a logic ‘1’ state (Figure 12). The period of each Frz_Data bit equals the period of the free–running Frz_Clk signal. The Frz_Data serial transmission should be timed so the MPC970 can sample each Frz_Data bit with the rising edge of the free–running Frz_Clk signal.



D0 is the control bit for 2x_PCLK
D1 is the control bit for PCLKEN
D2 is the control bit for BCLKEN
D3–D6 are the control bits for BCLK1–BCLK4
D7–D12 are the control bits for PCI_CLK1–PCI_CLK6

Figure 12. Freeze Data Input Protocol

The user can combine the two freeze capabilities to simplify system level implementation. The serial input port can be used to establish the freeze mask to disable the appropriate outputs. The Frz_Strobe input can then be used to unfreeze the outputs without having to serially load an “all unfrozen” freeze mask.

Driving the PowerPC 601 Microprocessor

The MPC601 processor requires three clock inputs from the MPC970 clock driver. A 2x_PCLK input at twice the internal MPC 601 clock rate and the PCLKEN and BCLKEN signals used to mask internal clock edges. The PCLKEN signal always runs at one half the 2x_PCLK signal while the BCLKEN signal can run at 1x, 1/2x, 1/3x or 1/4x the PCLK input signal depending on the speed of the processor bus. When the BCLKEN signal is running at 1/3 or 1/4 the PCLK input the input duty cycle must be 66/33 and 75/25 respectively. In addition, as shown in Figure 13, to satisfy the BCLKEN to 2x_PCLK Hold specification the BCLKEN signal must be at least coincident with the 2x_PCLK edge. To simplify board level implementation it would be desirable that the BCLKEN signal actually lag the 2x_PCLK by a few hundred picoseconds. The MPC970 insures that its BCLKEN output always lags the 2x_PCLK input by at least 300ps.

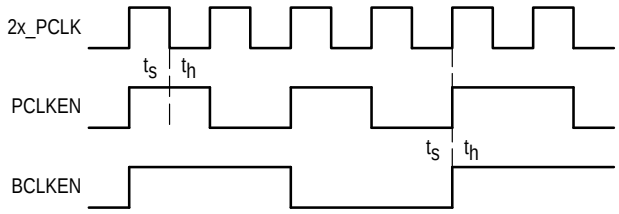


Figure 13. MPC601 Setup and Hold Times

Table 4 illustrates some typical MPC 601 system frequencies which can be realized using the MPC970 clock driver.

Table 4. Common MPC601 System Frequencies

2x_PCLK	PCLK	BCLK	PCI_CLK
240	120	60(1/2x)	30(1/2x)
240	120	40(1/3x)	20(1/2x)
240	120	30(1/4x)	30(1x)
200	100	50(1/2x)	25(1/2x)
200	100	33(1/3x)	33(1x)
200	100	25(1/4x)	25(1x)
160	80	40(1/2x)	20(1/2x)
160	80	20(1/4x)	20(1x)
132	66	66(1x)	33(1/2x)
132	66	33(1/2x)	33(1x)

Driving the PowerPC 603, PowerPC 604 and Pentium Microprocessors

The PowerPC 603, PowerPC 604 and Pentium processors differ from the MPC 601 processor in that the processor input clocks are at the same frequency as the processor bus. A typical system for these processors will include 8 – 16 clock loads on the processor bus. When the MPC970 is taken out of the MPC601_Clk mode there are a total of 8 “non PCI_CLK” outputs which can be run at the processor bus speeds for these microprocessors. Since each output can drive two series terminated transmission lines the MPC970 can support point to point clock distribution for up to 16 loads on the processor bus. In addition there will be 7 PCI_CLK outputs which can drive up to 14 loads on the PCI bus.

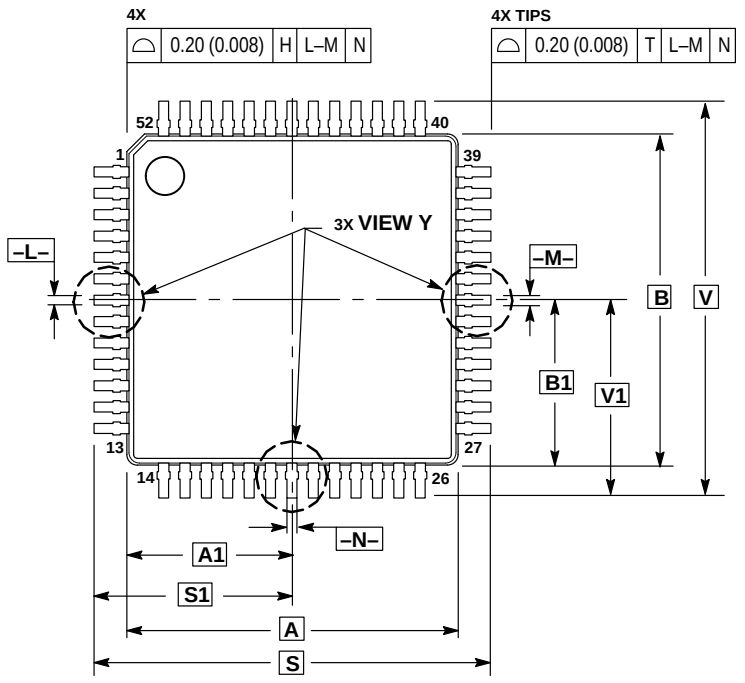
If more clock loads are present on the processor bus the PCI_CLKs can be configured to drive processor bus clock loads in addition to the BCLKs or alternatively the clocking roles of the BCLKs and PCI_CLKs can be reversed. Table 3 illustrates some useful frequency combinations for driving PowerPC 603, PowerPC 604 or Pentium microprocessor based systems.

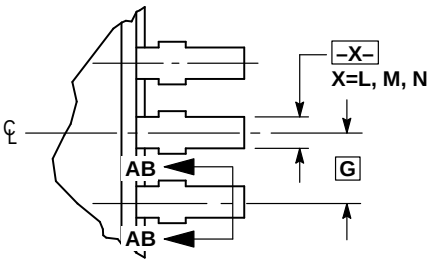
Table Table 5. Common PowerPC 603, PowerPC 604 and Pentium System Frequencies

2x_PCLK	PCLK	BCLK	PCI_CLK
80	80	80(1x)	26(1/3x)
75	75	75(1x)	25(1/3x)
66	66	66(1x)	33(1/2x)
66	66	66(1x)	66(1x)
66	66	33(1/2x)	66(PCLKEN)
60	60	60(1x)	30(1/2x)

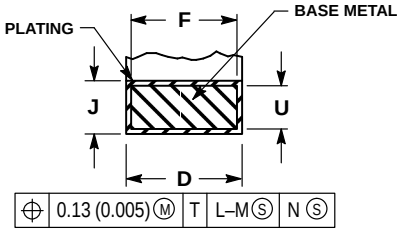
OUTLINE DIMENSIONS

FA SUFFIX
TQFP PACKAGE
CASE 848D–03
ISSUE C

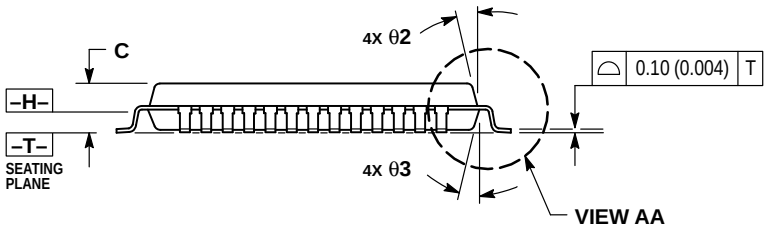




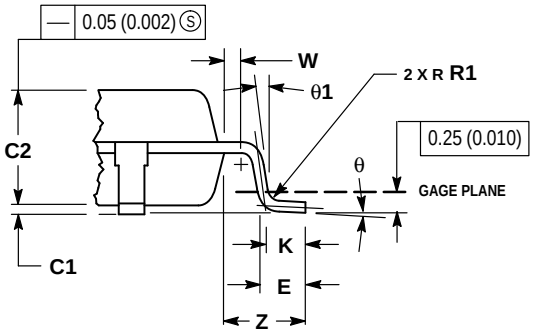
VIEW Y



SECTION AB–AB
ROTATED 90° CLOCKWISE



VIEW AA



VIEW AA

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
A1	5.00 BSC		0.197 BSC	
B	10.00 BSC		0.394 BSC	
B1	5.00 BSC		0.197 BSC	
C	—	1.70	—	0.067
C1	0.05	0.20	0.002	0.008
C2	1.30	1.50	0.051	0.059
D	0.20	0.40	0.008	0.016
E	0.45	0.75	0.018	0.030
F	0.22	0.35	0.009	0.014
G	0.65 BSC		0.026 BSC	
J	0.07	0.20	0.003	0.008
K	0.50 REF		0.020 REF	
R1	0.08	0.20	0.003	0.008
S	12.00 BSC		0.472 BSC	
S1	6.00 BSC		0.236 BSC	
U	0.09	0.16	0.004	0.006
V	12.00 BSC		0.472 BSC	
V1	6.00 BSC		0.236 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	7°	0°	7°
θ1	0°	—	0°	—
θ2	12° REF		12° REF	
θ3	5°	13°	5°	13°

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