MOTOROLA
■ **SEMICONDUCTOR** ■
TECHNICAL DATA

MJ8504
MJ8505

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJ8504 and MJ8505 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times
   75 ns Inductive Fall Time —25°C (typ)
   150 ns Inductive Crossover Time —25°C (typ)
   1.25 μs Inductive Storage Time —25°C (typ)

Operating Temperature Range —65 to + 200°C

100°C Performance Specified for:
   Reverse-Biased SOA with Inductive Loads
   Switching Times with Inductive Loads
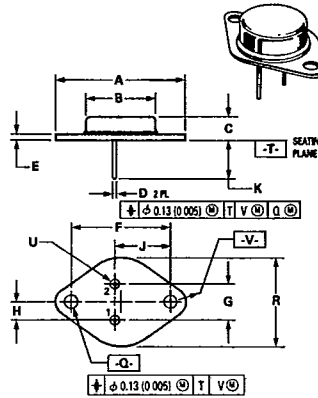   Saturation Voltages
   Leakage Currents

10 AMPERE

NPN SILICON
POWER TRANSISTORS

700 and 800 VOLTS
175 WATTS

Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14 5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO 204AA OUTLINE SHALL APPLY.

MAXIMUM RATINGS

Rating	Symbol	MJ8504	MJ8505	Unit
Collector-Emitter Voltage	V_{CEO}	700	800	Vdc
Collector-Emitter Voltage	V_{CEV}	1200	1400	Vdc
Emitter Base Voltage	V_{EB}	8.0	8.0	Vdc
Collector Current — Continuous	I_C	10	10	Adc
Peak (1)	I_{CM}	15	15	
Base Current — Continuous	I_B	8	8	Adc
Peak (1)	I_{BM}	12	12	
Total Power Dissipation @ T_C = 25°C	P_D	175	175	Watts
@ T_C = 100°C		100	100	
Derate above 25°C		1.0	1.0	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	—65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ⩽ 10%.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

CASE 1-06
TO-204AA
(TO-3)

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) MJ8504		$V_{CEO(sus)}$	700	–	–	Vdc
(I_C = 100 mA, I_B = 0) MJ8505			800	–	–	
Collector Cutoff Current		I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	–	0.25	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			–	–	5.0	
Collector Cutoff Current		I_{CER}	–	–	5.0	mAdc
(V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)						
Emitter Cutoff Current		I_{EBO}	–	–	1.0	mAdc
(V_{EB} = 7.0 Vdc, I_C = 0)						
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$		See Figure 12		
Clamped Inductive SOA with Base Reverse Biased		RBSOA		See Figure 13		
ON CHARACTERISTICS (1)						
DC Current Gain		h_{FE}	7.5	–	–	–
(I_C = 1.5 Adc, V_{CE} = 5.0 Vdc)						
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 5.0 Adc, I_B = 2.0 Adc)			–	–	2.0	
(I_C = 10 Adc, I_B = 4.0 Adc)			–	–	5.0	
(I_C = 5.0 Adc, I_B = 2.0 Adc, T_C = 100°C)			–	–	3.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 5.0 Adc, I_B = 2.0 Adc)			–	–	1.5	
(I_C = 5.0 Adc, I_B = 2.0 Adc, T_C = 100°C)			–	–	1.5	
DYNAMIC CHARACTERISTICS						
Output Capacitance		C_{ob}	90	–	450	pF
(V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)						
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 500 Vdc, I_C = 5.0 A,	t_d	–	0.050	0.20	μs
Rise Time	I_{B1} = 2.0 A, $V_{BE(off)}$ = 5.0 Vdc, t_p = 50 μs,	t_r	–	0.175	2.0	μs
Storage Time	Duty Cycle < 2.0%)	t_s	–	1.25	4.0	μs
Fall Time		t_f	–	0.60	2.0	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 5.0 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 2.0 A,	t_{sv}	–	1.75	5.5	μs
Crossover Time	$V_{BE(off)}$ = 5 Vdc. T_C = 100°C	t_c	–	0.400	2.0	μs
Storage Time	(I_C = 5.0 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 2.0 A,	t_{sv}	–	1.25	–	μs
Crossover Time	$V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_c	–	0.150	–	μs
Fall Time		t_{fi}	–	0.075	–	μs

(1) Pulse Test: PW - 300 μs, Duty Cycle < 2%.

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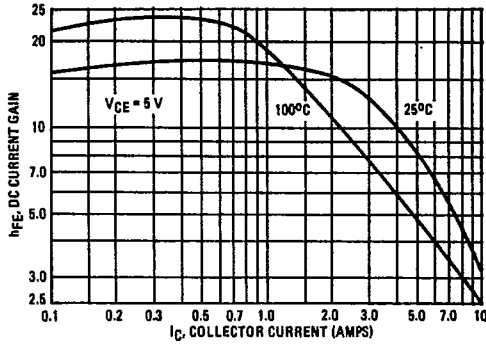**FIGURE 1 — DC CURRENT GAIN**

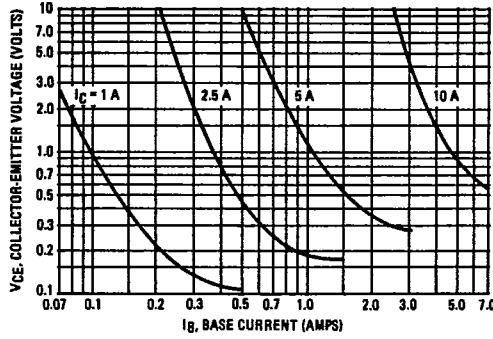**FIGURE 2 — COLLECTOR SATURATION REGION**

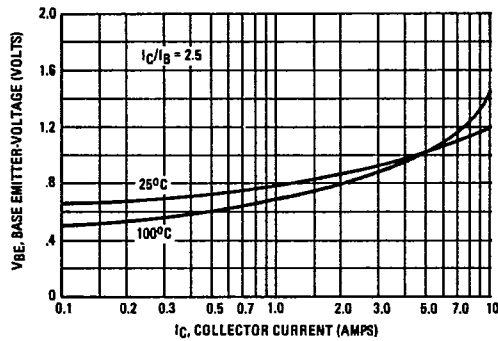**FIGURE 3 — COLLECTOR-EMITTER SATURATION REGION**
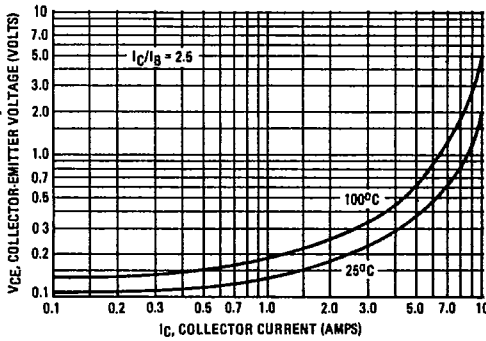
FIGURE 4 — BASE EMITTER VOLTAGE
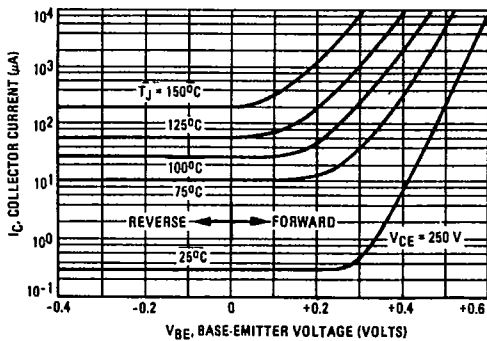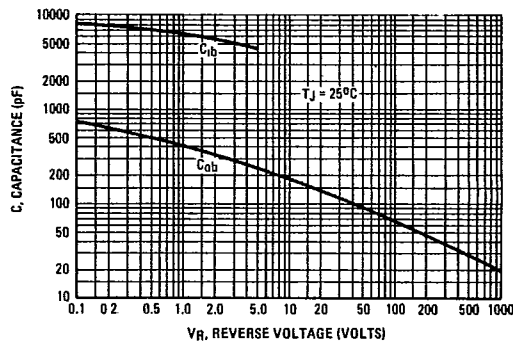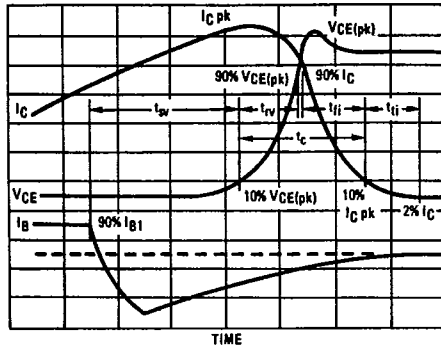

FIGURE 5 — COLLECTOR CUTOFF REGION

FIGURE 6 — CAPACITANCE

SWITCHING TIMES NOTE

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% $V_{CE(pk)}$

t_{rv} = Voltage Rise Time, 10—90% $V_{CE(pk)}$

t_{fi} = Current Fall Time, 90—10% I_C

t_{ti} = Current Tail, 10—2% I_C

t_c = Crossover Time, 10% $V_{CE(pk)}$ to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2 \ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 8 — PEAK REVERSE BASE CURRENT
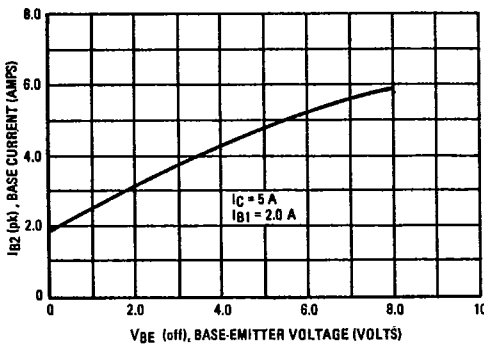
RESISTIVE SWITCHING PERFORMANCE
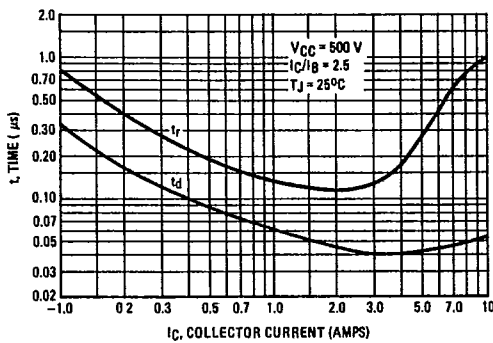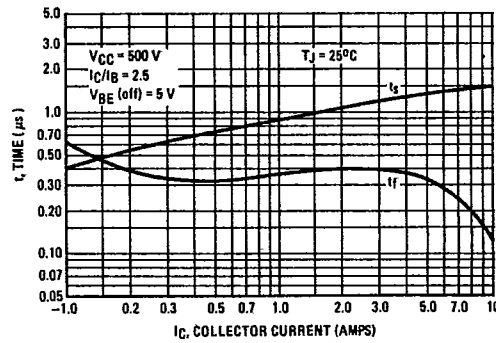
FIGURE 9 — TURN-ON SWITCHING TIMES

FIGURE 10 — TURN-OFF SWITCHING TIMES

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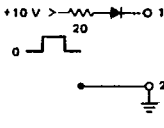**TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE**
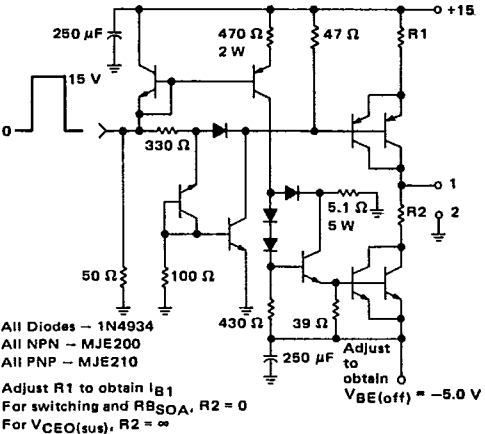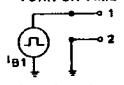
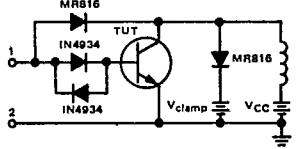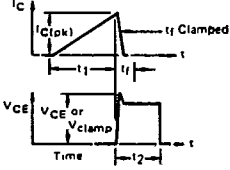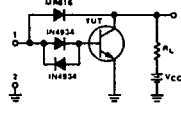|	V_CEO(sus)	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	+10 V >—⋀⋀—▶⊢—o 1 20 0 ⊓_ o 2 PW Varied to Attain I_C = 100 mA .	 All Diodes — 1N4934 All NPN — MJE200 All PNP — MJE210 Adjust R1 to obtain I_B1 For switching and RBSOA, R2 = 0 For V_CEO(sus), R2 = ∞	**TURN ON TIME** I_B1 adjusted to obtain the forced h_FE desired **TURN OFF TIME** Use inductive switching driver as the input to the resistive test circuit
CIRCUIT VALUES	L_coil = 80 mH V_CC = 10 V R_coil = 0.7 Ω	L_coil = 180 μH R_coil = 0.05 Ω V_clamp = 500 V V_CC = 20 V	V_CC = 500 V R_L = 100 Ω Pulse Width = 50 μs
TEST CIRCUITS		**INDUCTIVE TEST CIRCUIT** **OUTPUT WAVEFORMS** $t_1 \approx \dfrac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \dfrac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	**RESISTIVE TEST CIRCUIT**

FIGURE 11 — THERMAL RESPONSE

$R_{\theta JC}(t) = r(t) R_{\theta JC}$
$R_{\theta JC} = 1.0°C/W$
$T_{J(pk)} - T_C = P_{(pk)} R_{\theta JC}(t)$

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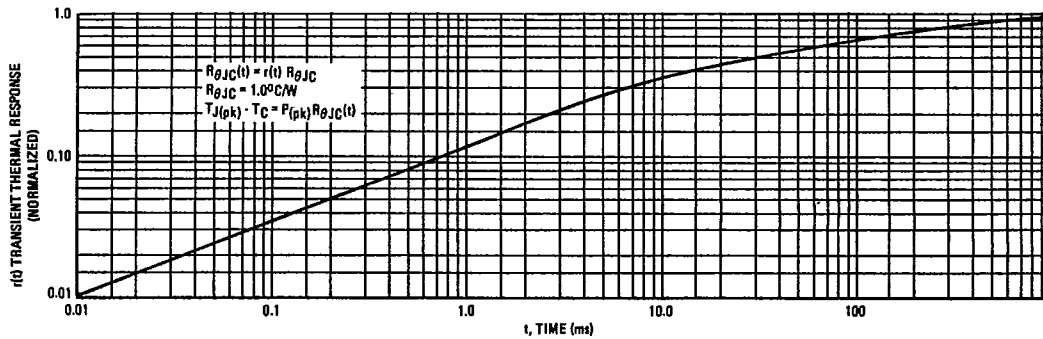
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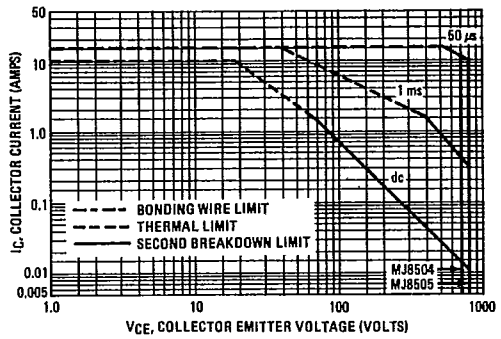## SAFE OPERATING AREA INFORMATION

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

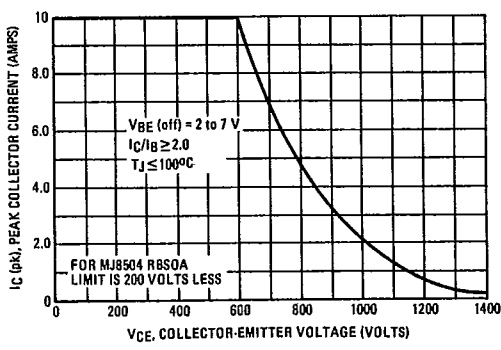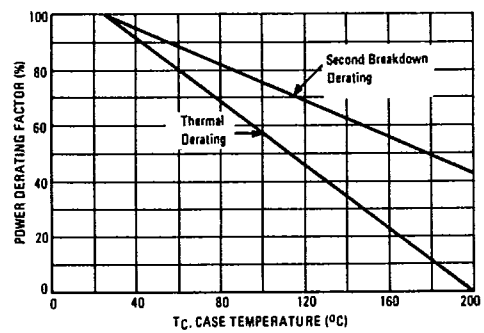### FIGURE 13 — RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

FIGURE 14 — POWER DERATING