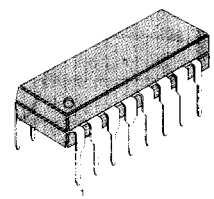
VIDEO AND SOUND IF AMPLIFIER FOR MONOCHROME TV RECEIVERS

The KA2913A, KA2917 are silicon monolithic integrated circuits designed for the VIF and SIF stage in B/W television receivers.
KA2913A: for Forward AGC type
KA2917: for Reverse AGC type

16 DIP



FUNCTION

VIF stage

- Three controlled IF amplifier stages
- Video demodulator controlled by the picture carrier
- Black noise and white noise inverter
- DC amplifier for RF AGC output
- Peak AGC

SIF stage

- Three controlled IF amplifier stages
- Quadrature detector

FEATURE

VIF stage

- **High gain, wide band IF amplifier: 50dB (Typ.) at 45MHz**
- **Gain reduction with excellent stability: 55dB (Typ.) at 45MHz**
- **Excellent DG/DP characteristics: DG 7% (Typ.), DP 3.5 deg. (Typ.)**
- **Excellent S/N characteristics due to delayed 3-stage AGC action.**
- **Fast AGC action due to noise inverter and peak AGC.**
- **Switch off the video part with VTR switch.**
- **Dual differentiel AFT output**

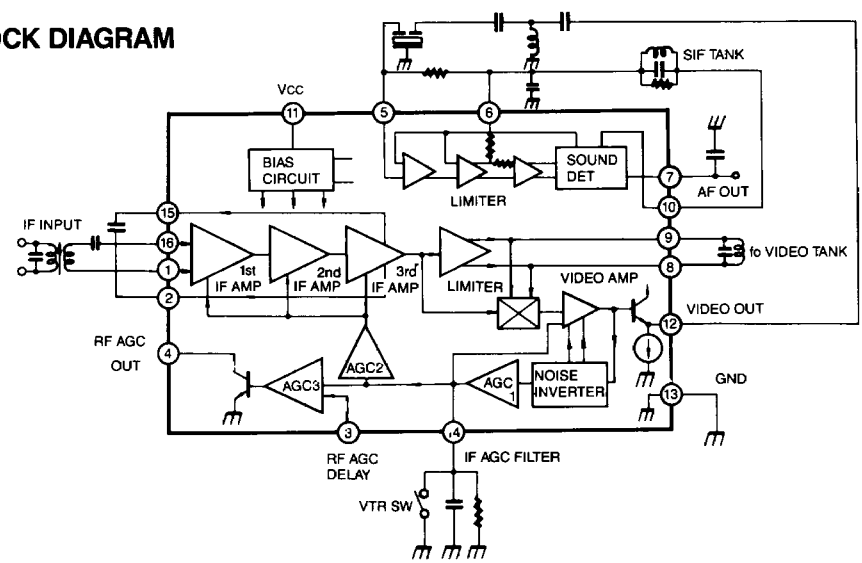
SIF stage

- **Excellent limiter characteristics.**
- **Excellent AM rejection.**
- **Large undistorted audio output voltage with quadrature detector.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2913A	16 DIP	−20 ~ +65°C
KA2917		

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage (Pin 11)	V_{CC}	15	V
Open Loop Voltage (Pin 4)	V_4	15	V
Video DC Output Current (Pin 12)	I_{12}	6	mA
Power Dissipation (Note)	P_D	1.4	W
Ambient Temperature	T_a	−20 ~ 65	°C
Storage Temperature	Tstg	−55 ~ 150	°C

Note: Derated above T_a = 25°C in the proportion of 11.2 mW/°C.

ELECTRICAL CHARACTERISTICS

VIF Stage (T_a = 25°C, V_{CC} = 12V, V_{CC} = 12V, f_P = 45.75MHz, f_S = 41.25MHz)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Recommended Supply Voltage	V_{CC} (V_{11})	—	10.8	12.0	13.2	V	—
Supply Current	I_{CC} (I_{11})	S_1: On, S_3: 2, S_5: 2, S_4: 1	35	50	65	mA	1
Video DC Output Voltage	V_{12}	S_1: Off, S_3: 2, S_5: 2, S_4: 1	5.2	5.5	5.8	V	1
Terminal Voltage 5	V_5	S_1: On, S_3: 2, S_5: 2, S_4: 1	3.5	4.4	5.3	V	1
Terminal Voltage 7	V_7	S_1: On, S_3: 2, S_5: 2, S_4: 1	4.6	6.0	7.2	V	1
RF AGC Residual Output Voltage	V_4 Sat	S_1: Off, S_3: 2, S_5: 2, S_4: 1	—	—	0.5	V	1
RF AGC Leak Current	I_4 Leak	S_1: Off, S_3: 1, S_5: 1, S_4: 2	—	—	1	μA	1
Video Sensitivity	v_1 Pin-16	(Note 1)	60	150	250	μV_{rms}	2
AGC Range	ΔA (IF)	(Note 2)	60	64	—	dB	2
SYNC TIP Level Voltage	V_{SYNC} (V_{12})	(Note 3)	2.3	2.5	2.7	V	2
Maximum IF Input Voltage	v_{IN} Max PIF	(Noite 4)	100	120	—	mV_{rms}	2
White Noise Threshold	V_W TH (V_{12})	(Note 5)	5.8	6.2	6.6	V	2
White Noise Clamp Level	V_{WCL} (V_{12})	(Note 5)	3.7	4.1	4.5	V	2
Black Noise Threshold	V_B TH (V_{12})	(Note 5)	1.4	1.6	1.8	V	2

ELECTRICAL CHARACTERISTICS
VIF Stage ($T_a = 25°C$, $V_{CC} = 12V$, $f_P = 45.75MHz$, $f_S = 41.25MHz$)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit	Test Fig
Black Noise Clamp Level	V_B CL (V_{12})	(Note 5)		2.9	3.3	3.7	V	2
Video Frequency Response	f_{ew}	(Note 6)		4.5	5.5	—	MHz	3
Suppression of Carrier	CL	(Note 7)		40	50	—	dB	4
Suppression of 2nd Carrier	I_{2nd}	(Note 8)		40	50	—	dB	4
Suppression of Sound Carrier/ Color Subcarrier	I_{920}	(Note 9)		33	38	—	dB	4
Differential Phase	DP	(Note 10)		—	3.5	5	deg	5
Differential Gain	DG	(Note 10)		—	7	10	%	5
VIF Input Impedance	R_{IN} (VIF)	(Note 11)		1.5	3.0	6.0	KΩ	6
	C_{IN} (VIF)			—	3.0	10.0	pF	
Max. Available Current	$I_{4\ MAX}$	(Note 12)	KA2917	0.3	—	—	mA	1
			KA2913A	7	—	—	mA	
RF AGC Delay Point Range	V_{IN} Delay	(Note 13)		5.0	7.0	9.0	V	2
Video Output Level	V_{OUT}	(Note 14)		2.25	2.5	2.75	V	2

ELECTRICAL CHARACTERISTICS
SIF Stage ($T_a = 25°C$, $V_{CC} = 12V$, $f_P = 45.75MHz$, $f_S = 41.25MHz$)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
SIF Output Voltage	S_{OUT}	(Note 15)	200	400	600	mV_{rms}	3
Input Limiting Voltage	V_{IN} (Lim)	(Note 16)	—	200	400	μV_{rms}	8
AM Rejection Ratio	AMR	(Note 17) $R_L = \infty$, $R_D = \infty$	40	45	—	dB	8
Recovered Output Voltage	V_{OD}	(Note 18) $R_L = \infty$, $R_D = \infty$	0.5	0.75	—	V_{rms}	8
Total Harmonic Distortion	THD	(Note 18) $R_L = \infty$, $R_D = \infty$	—	1.0	2.0	%	8
Max. Audio Output Voltage	V_{OM}	(Note 19)	4.0	—	—	V_{P-P}	8
SIF Input Impedance	R_{IN} (SIF)		10	20	30	KΩ	7
	C_{IN} (SIF)		—	3	10	pF	
Audio Output Impedance	$R_{O(AF)}$	(Note 20)	10	15	20	KΩ	9

Note 1) V_{AGC} (TP14 EXT. Applying voltage)=11.5V
VIF in: f=45.75MHz,1kHz 30% AM modulation
Adjust VIF input level v_i so that the detected output of TP12C with high impedance probe will be $0.8V_{P-P}$ and measure the input level.

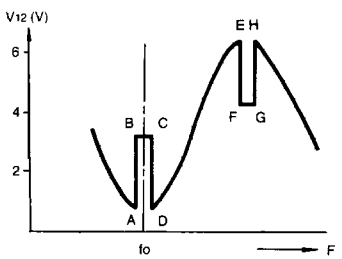
Note 2) V_{AGC} =4V
Measure VIF input level v_i' same as note 1

$$\Delta A = 20 \log \frac{v_i'}{v_i} (dB)$$

Note 3) VIF in: f=45.75MHz CW 15mVrms
Measure the DC level of TP12A.

Note 4) VIF in: f=45.75MHz APL100%, 87.5% AM modulation.
TP14: open
(1) Adjust VIF input level $50mV_{P-P}$ and measure the detected output level v_{oP-P}
(2) Then increase the input level so that the detected output level will be $1.1\times v_{oP-P}$ and measure the input level.

Note 5) V_{AGC} =8V
VIF in: f=45.75MHz±10MHz variable or sweep 15mVrms measure DC level of TP12A



Note 6) V_{AGC} =8V
SG_1: 45.75MHz CW
SG_2: 45.65-27MHz variable
(1) Setting output of SG_1 so that the DC level of TP12A will
(2) Setting output of SG_2 (45.65MHz) so that the AC level of TP12A will be $0.5V_{p-p}$
(3) Decreasing frequency of SG_2 until the AC level of TP12A will be $0.35V_{p-p}$ (−3dB of $0.5V_{p-p}$) then read $f_{SG2} = F$ $f_{BW} = 45.75\text{-}F$ MHz

Note 7) SG_1: 45.75MHz, 1kHz 80% AM modulation 100mVrms
SG_2, SG_3; off
Setting V_{AGC} so that the output AC level of TP12A will be $2.7V_{p-p}$
Measure CL of TP12A after setting to 0% AM of SG_1

Note 8) Measure 2nd of TP12A same as Note 9

Note 9) V_{AGC} =8V
SG_1: 45.75MHz (P: picture) 100mVrms
SG_2: 41.25MHz (S: sound) 32mVrms (−10dB of SG_1)
SG_3: 42.17MHz (C: chroma) 32mVrms (−10dB of SG_1)
(1) Setting V_{AGC} so that the output tip level (lower) of TP12A will be 3.0V DC
(2) Measure the level difference (dB) between the C-level and 920KHz level

Note 10) V_{AGC} =8V
VIF in: f=45.75MHz video signal (RAMP) 87.5% AM $100mV_{P-P}$
Setting ATT so that the SYNC TIP level of TP12A will be 2.5V DC measure DP and DG.

Note 11) V_{AGC} = 5V f=45.75MHz
Measure R_{IN}, C_{IN}

Note 12) S_1: On, S_3: 2, S_5: 1 S_4: 1 for 2917
2 for 2913A

Note 13) TP14: Open
VIF in: 45.75MHz CW 20mVrms
(1) Adjust the voltage of Terminal 3 so that the voltage of Terminal 4 will be 6.0V DC
(2) Measure the Terminal voltage 3

Note 14) TP14: Open
VIP in: 45.75MHz 100% APL 87.5% AM modulation signal amplitude 50m$V_{p\text{-}p}$, measure the detected output voltage (white peak to SYNC TIP)

Note 15) TP14: Open
SG_1: 45.75MHz CW 100mVrms
SG_2: 41.25MHz CW 25mVrms
Measure SIF (4.5MHz) output voltage at TP12A

Note 16) SIF IN: f=4.5MHz FM f_{MOD} = 400Hz $\Delta f = \pm 25$kHz
(1) Adjust SIF input level 100m$V_{P\text{-}P}$ and measure the detected output level υ_{OS}
(2) Then decrease the input level so that the detected output level will be 3dB down of υ_{OS} and measure the input level.

Note 17) SIF IN: f=4.5MHz FM f_{MOD} = 400Hz $\Delta f = \pm 25$kHz
AM 30%
Input level υ_{INs} = 100dBμ

Note 18) SIF IN: f=4.5MHz FM f_{MOD} = 400Hz $\Delta f = \pm 25$kHz
Input level υ_{INs} = 80dBμ

Note 19) SIF in: f=4.4-4.6MHz variable or sweep measure the output DC voltage change

Note 20) SIF IN: f=4.5MHz FM f_{MOD} = 400Hz $\Delta f = \pm 25$kHz
Input level υ_{INS} = 80dBμ
(1) Measure the detected output voltage V_{OA} with $R_X = \infty$
(1) Then, adjust R_X so that the detected output voltage will be $\frac{V_{OA}}{2}$ and measure R_X.

1. DC TEST CIRCUIT

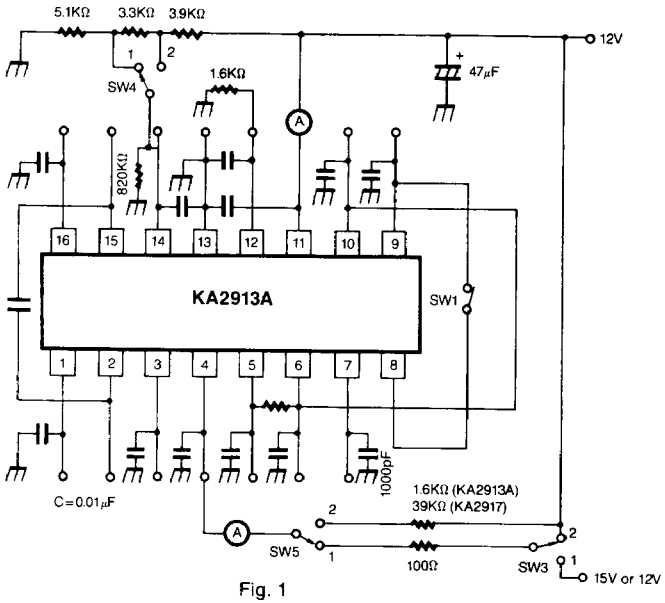


Fig. 1

2. AC TEST CIRCUIT

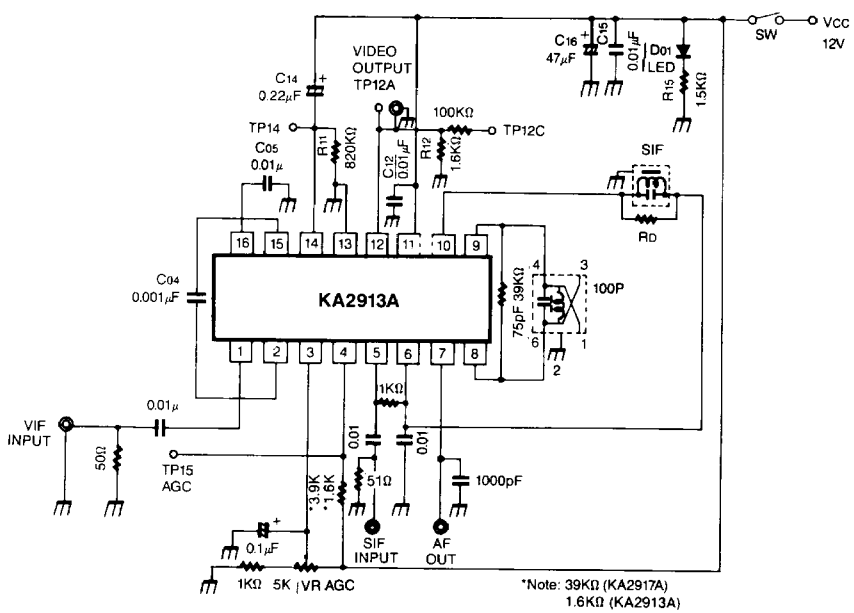


Fig. 2

3. VIDEO FREQUENCY RESPONSE & SIF OUTPUT VOLTAGE TEST CIRCUIT

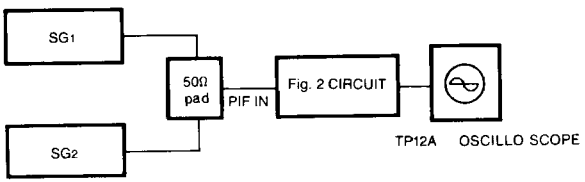


Fig. 3

4. INTER MODULATION TEST CIRCUIT

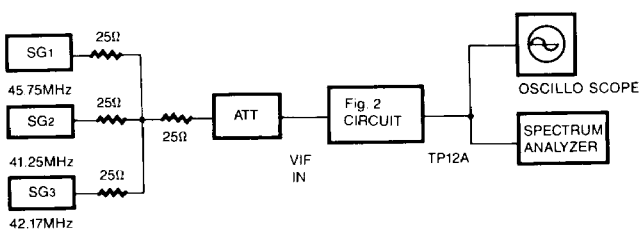
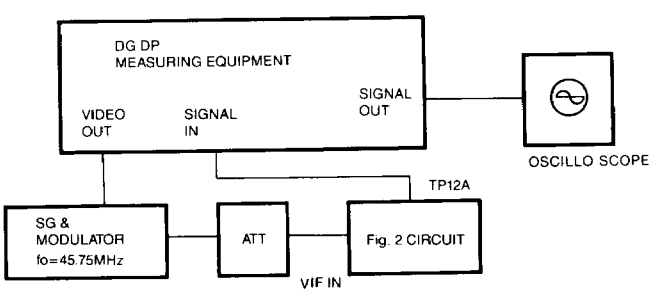


Fig. 4

5. DG, DP TEST CIRCUIT



APL: 50%
ATT: ADJUST SYNC TIP LEVEL TO DC2.5V

Fig. 5

6. INPUT IMPEDANCE TEST CIRCUIT

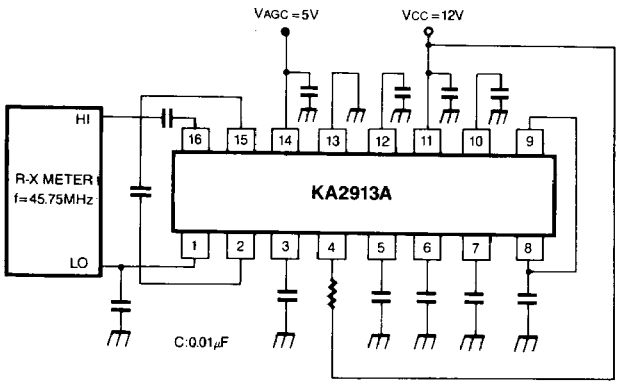


Fig. 6

7. SIF INPUT IMPEDANCE TEST CIRCUIT

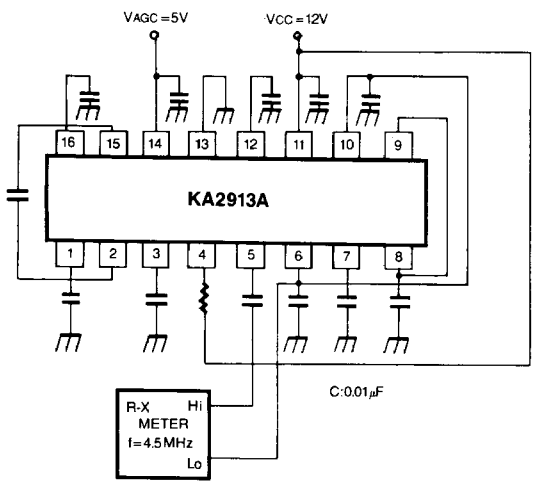


Fig. 7

8. V_{IN} (LIM), AMR, V_{OD}, THD, V_{OM} TEST CIRCUIT

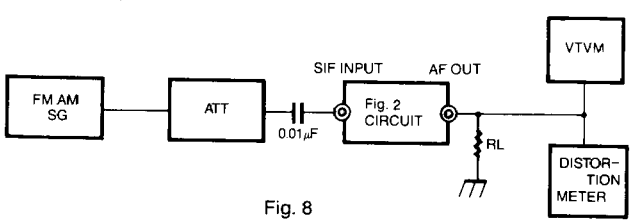


Fig. 8

9. AUDIO OUTPUT IMPEDANCE TEST CIRCUIT

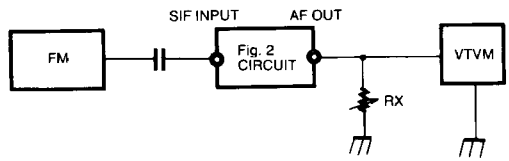


Fig. 9

TYPICAL APPLICATION CIRCUIT