July 1998 File Number 3210.3

PART WITHDRAWN
PROCESS OBSOLETE
NO NEW DESIGNS

Features

- 500V Maximum Rating
- 2A Peak Gate Drive
- Ability to Interface and Drive N-Channel Power Devices With Complimentary Outputs For Buffered FETs
- Fault Output, Overcurrent Detection and Undervoltage Holdoff
- Over 600kHz Sawtooth Oscillator Frequency
- Adjustable Deadtime Control
- Soft-Start Capability
- Low Current Standby State
- Sleep Mode Reduces Bias Current When Not Enabled

Applications

- Switching and Distributed Power Supplies
- Electronic Lighting Supplies

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP5500IP	-40°C to +85°C	20 Lead Plastic DIP
HIP5500IB	-40°C to +85°C	20 Lead Plastic SOIC (W)

High Voltage IC Half Bridge Gate Driver

The HIP5500, a high voltage integrated circuit (HVIC) half-bridge gate driver for standard power MOSFETs, IGBTs, and the new Intersil Buffered MOSFET (RFV10N50BE), can be employed in a wide variety of switching regulator circuits.

The HIP5500 combines the functionality and flexibility of a PWM IC with the convenience of a high voltage half-bridge driver optimized for power supply inverters. It can be used either open-loop or in closed-loop fashion using the SS input for controlling the output waveform duty-cycle.

The HIP5500 incorporates a precision oscillator, adjustable using an external resistor and capacitor. The resistor sets the capacitor charging current and the capacitor sets the integration time of a triangle wave. Another resistor connected to the DIS pin adjusts the dead-time and can be tailored to the application. The oscillator switches at twice the output waveform fundamental frequency. The result is an output waveform whose positive and negative half-cycles are near perfect balance (volt-second equalization).

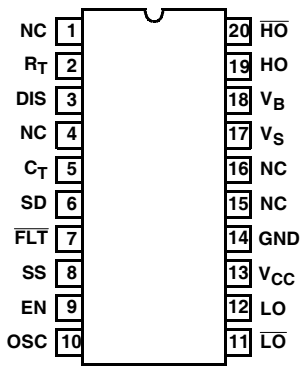
Short-Detect (SD) and Soft-Start (SS) inputs provide alternative means for limiting and regulating respectively the half-bridge output voltage. A capacitor on the SS input will begin charging up once the EN input is made high and causes the duty cycle of each half-cycle to “ramp” the duty cycle of the output waveform.

The SD input can sense a signal proportional to current, providing a means of shortening the conduction periods below that imposed by the SS input.

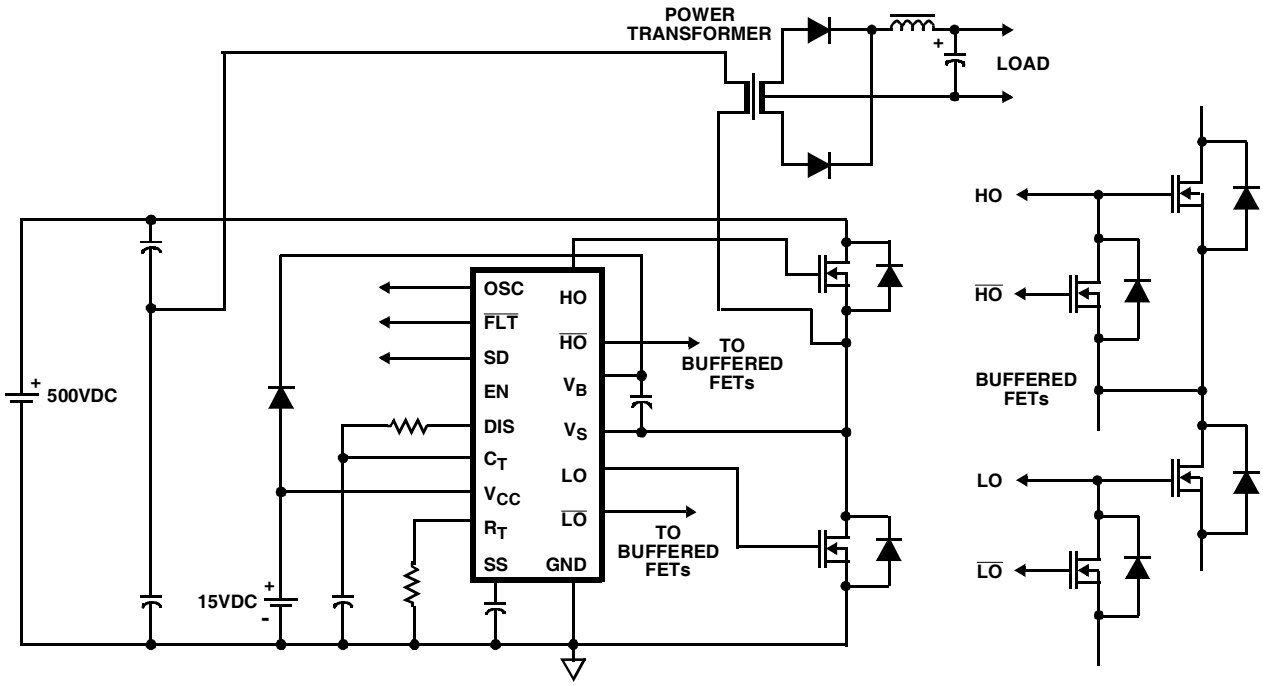
Other circuits within the HIP5500 “match” upper and lower turn-on and turn-off propagation times in order to minimize flux imbalances when driving output transformer loads.

Pinout

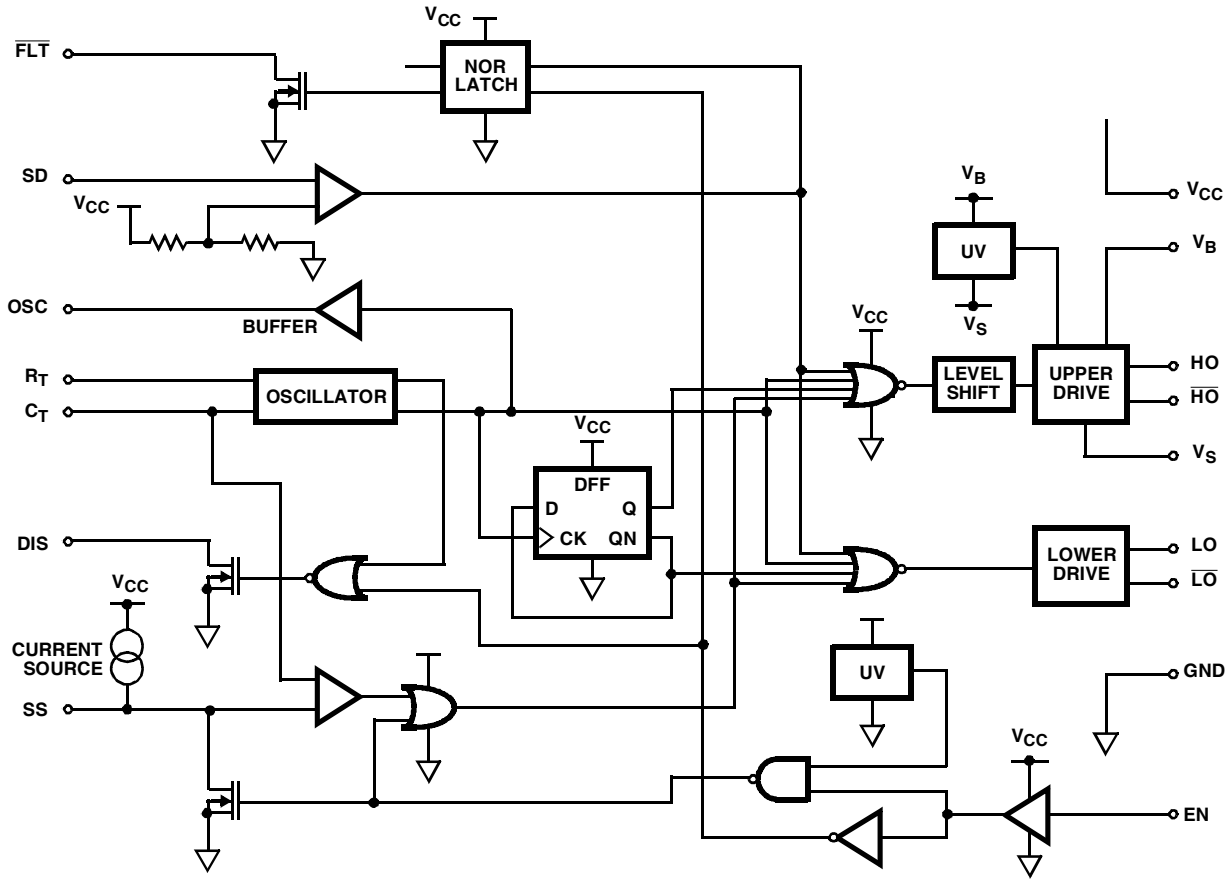
HIP5500 (PDIP, SOIC)
TOP VIEW



Typical Application Block Diagram



Functional Block Diagram



Absolute Maximum Ratings

Offset Supply Voltage, V_S . . . . . $-V_{BS}$ to +500V
Floating Supply Voltage (V_B to V_S) . . . . . -0.3V to +18V
High Side Channel Output Voltage, V_{HO}, V_{NHO} . V_S-0.5 to V_B+0.5
Fixed Supply Voltage, V_{CC} . . . . . -0.5V to +18V
Low Side Channel Output Voltage . . . . . -0.5V to V_{CC} +0.5V
All Other Pin Voltages
(SD, R_T, C_T, DIS, SS, EN and FLT) . . . . . -0.5V to V_{CC} +0.5V
Storage Temperature Range . . . . . -40^oC to $+150^oC$
Junction Temperature. . . . . $+125^oC$
Lead Temperature (Soldering 10s). . . . . $+300^oC$
(SOIC - Lead Tips Only)
Offset Supply Maximum dv/dt, dV_S/dt 50V/ns
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance	θ_{JA}
Plastic DIP Package	$75^oC/W$
Plastic SOIC Package.	$80^oC/W$

See Maximum Power Dissipation vs Temperature Curve Figure 21

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions (T_J = -40^oC to $+125^oC$ Unless Otherwise Noted, All Voltages Referenced to V_{SS})

Offset Supply Voltage, V_S . . . . . -2.0V to +500V
Floating Supply Voltage, V_{BS} (V_B to V_S) . . . . . +10V to +15V
High Side Channel Output Voltage, V_{HO},V_{NHO} . . . . . 0V to V_{BS}
Fixed Supply Voltage, V_{CC} . . . . . +10V to +15V
Low Side Channel Output Voltage, V_{LO},V_{NLO}. . . . . 0V to V_{CC}
All Other Pin Voltages (SD, R_T, C_T, DIS, SS, FLT and EN) 0V to V_{CC}
Discharge Time Constant . . . . . 100ns Min
Discharge Resistor Range, R_{DIS} . . . . . 1kΩ to 50kΩ
Charging Resistor Range, R_T. . . . . .6.8kΩ to 400kΩ
Oscillator Capacitor Range, C_T. . . . . 100pF to 0.1μF
Oscillator Frequency Range . . . . . 300kHz Max
Oscillator Capacitor Charge Current Range, I_{R_T} . . . . .21μA to 5mA

Electrical Specifications V_{CC} = V_{BS} = +15V, V_S = GND = 0V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	T_J = $+25^oC$			T_J = -40^oC TO $+125^oC$		UNITS
			MIN	TYP	MAX	MIN	MAX	
Quiescent V_{CC} Current	I_{QCC}		-	5.5	7.0	-	8.0	mA
Quiescent V_{BS} Current	I_{QBS}		-	300	400	-	435	μA
Quiescent Leakage Current	I_{LK}	(V_S - GND) = 5.0V	-	0.4	3.0	-	-	μA
Standby V_{CC} Current	I_{STBY}	R_T = 0	-	2.0	3.5	-	5.0	mA
SS Current Source	$I_{SFT/PWM}$	$^1/_3V_{CC} < V_{SFT} < {}^2/_3V_{CC}$	70	110	145	60	160	μA
Input Threshold	V_{EN}	Low to High Transition	7.5	7.8	8.5	7.4	8.6	V
Input Hysteresis	V_{EN-HYS}		-	2	-	-	-	V
Undervoltage Threshold	V_{UVHL}	High to Low Transition	7.7	8.6	9.5	7.4	9.6	V
Undervoltage Threshold	V_{UVLH}	Low to High Transition	7.9	8.8	9.7	7.6	9.8	V
Undervoltage Hysteresis	V_{UVHYS}		0.08	0.3	0.7	0.05	0.75	V
Short Detect Threshold	V_{THSD}		3.5	4.0	4.5	3.4	4.6	V
C_T/R_T Current Ratio	I_{CTRAT}	I_{R_T} = 100μA, $V_{CC}/3 < V_{CT} < {}^2/_3V_{CC}$	0.9	1	1.1	0.85	1.15	μA
HO, LO Peak Output Current	I_{OUT}+	Sourcing, LO, HO = GND	1.5	1.95	-	1.0	-	A
HO, LO Peak Output Current	I_{OUT}-	Sinking, LO, HO = V_{CC} = V_{BS}	1.5	2.0	-	1.0	-	A
$\overline{LO}$, $\overline{HO}$ Peak Output Current	I_{BUF}+	Sourcing, $\overline{LO}$, $\overline{HO}$ = Vss	170	250	-	110	-	mA
$\overline{LO}$, $\overline{HO}$ Peak Output Current	I_{BUF}-	Sinking, $\overline{LO}$, $\overline{HO}$ = V_{CC} = V_{BS}	170	230	-	110	-	mA

Electrical Specifications $V_{CC} = V_{BS} = +15V$, V_S = GND = 0V, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	$T_J = +25^oC$			$T_J = -40^oC$ TO $+125^oC$		UNITS
			MIN	TYP	MAX	MIN	MAX	
Soft-Start V_{THRESH}, Low to High	V_TSSHL	C_T = 7.5V	7.5	7.8	8.1	7.4	8.2	V
Soft-Start V_{THRESH}, High to Low	V_TSSLH		7.2	7.5	7.8	7.1	7.9	V
OSC Input Upper Threshold	V_TCTLH		9.8	10.4	11.0	9.7	11.1	V
OSC Input Upper Threshold	V_TCTHL	C_T to DIS	5.0	5.6	6.2	4.9	6.3	V
Oscillator Upper to Lower Threshold Difference	VCTDIF	V_TCTLH - V_TCTHL	4.5	4.8	5.1	4.4	5.2	V
OSC_OUT R_{DS}ON, Sinking	OSCR_{DS}L	I_{OSC_OUT} = -50mA	5	8.5	12	2	17	Ω
OSC_OUT R_{DS}ON, Sourcing	OSCR_DH	I_{OSC_OUT} = 50mA	14	19	30	9	40	Ω
DIS Output On Resistance	R_{DS}DIS	I_{DIS} = 10mA	75	115	150	-	200	Ω
$\overline{FLT}$ Output On Resistance	R_{DS}FLT	I_{FLT} = 5mA	100	165	230	40	320	Ω

Dynamic Electrical Specifications $V_{CC} = V_{BS} = +15V$, GND = 0V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	$T_J = +25^oC$			$T_J = -40^oC$ TO $+125^oC$		UNITS
			MIN	TYP	MAX	MIN	MAX	
Turn-On Rise Time, HO, LO	t_{DR}	C_L = 2000pF	-	-	50	-	-	ns
Turn-Off Fall Time, HO, LO	t_{DF}	C_L = 2000pF	-	-	50	-	-	ns
Turn-On Rise Time, $\overline{HO}$, $\overline{LO}$	t_{DNR}	C_{BUF} = 200pF	-	25	35	-	-	ns
Turn-Off Fall Time, $\overline{HO}$, $\overline{LO}$	t_{DNF}	C_{BUF} = 200pF	-	25	35	-	-	ns
C_T Fall to LO/HO Rise	T_PCTLH	$C_T = V_T$CTHL LO/HO LOAD = 200pF	-	475	700	-	925	ns
C_T Rise to LO/HO Fall	T_PCTHL	$C_T = V_T$CTLH LO/HO LOAD = 200pF	-	475	700	-	925	ns
LO-HO Prop Delay Mismatch	Delmatch	T_PCTLH and T_PCTHL	-	60	-	-	-	ns
C_T Rise to DIS Fall	T_PCTDISHL	$C_T = V_T$CTHL	-	300	450	-	475	ns
C_T Fall to DIS Rise	T_PCTDISLH	$C_T = V_T$CTLH	-	600	800	-	825	ns
Minimum Dead Time	t_{DTMIN}		-	200	-	-	-	ns
Short Detect Propagation Delay	$t_{SDLO/HO}$	SD = V_{THSD}, LO/HO = 200pF	-	425	850	-	1100	ns
Soft-Start Propagation Delay Time	t_{SSDLY}	SS = V_TSSLH, LO/HO = 200pF	-	500	750	-	775	ns

Typical Performance Curves All Curves are V_{CC} = +15V, T_A = +25°C, Unless Otherwise Specified

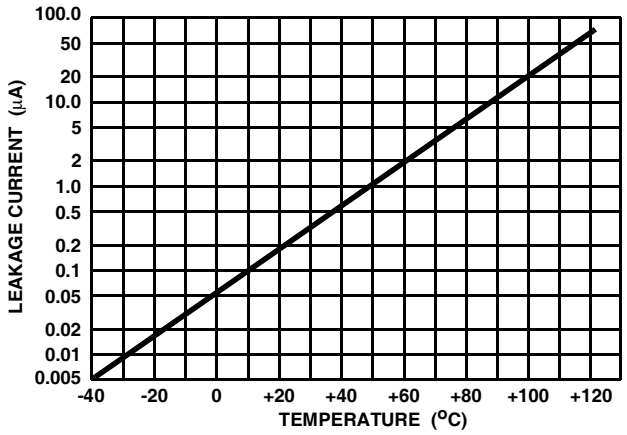


FIGURE 1. OFFSET SUPPLY LEAKAGE CURRENT vs TEMPERATURE AT 300VDC

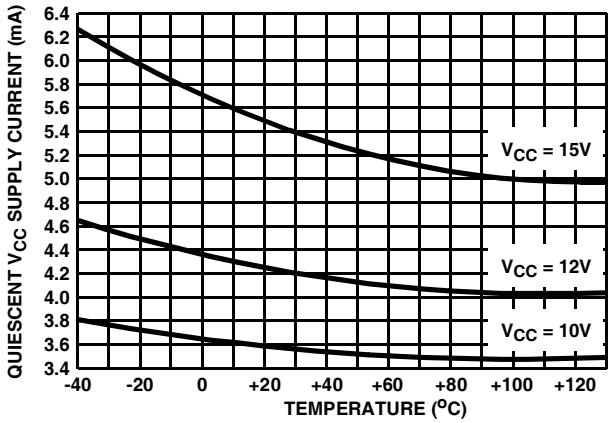


FIGURE 2. QUIESCENT V_{CC} CURRENT vs TEMPERATURE AND V_{CC} SUPPLY VOLTAGE

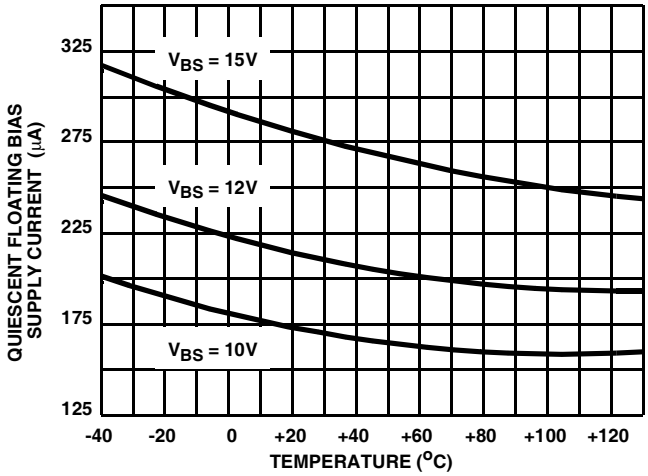


FIGURE 3. QUIESCENT FLOATING BIAS SUPPLY CURRENT vs TEMPERATURE AND V_{BS} SUPPLY VOLTAGE

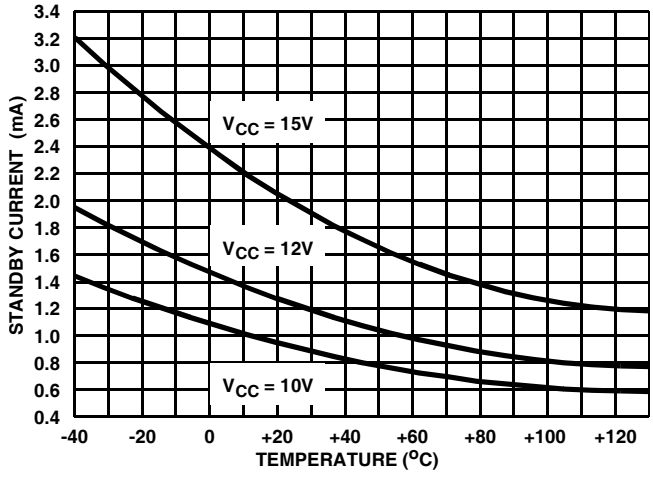


FIGURE 4. QUIESCENT STANDBY CURRENT vs TEMPERATURE AND V_{CC} SUPPLY VOLTAGE

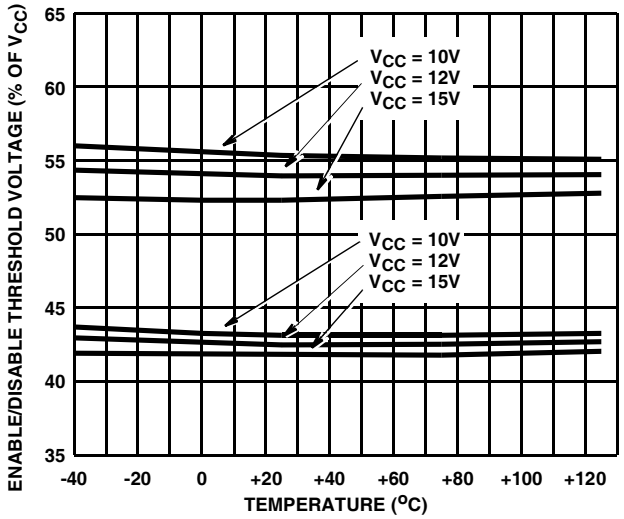


FIGURE 5. ENABLE/DISABLE THRESHOLD (PERCENT V_{CC}) vs TEMPERATURE AND V_{CC} SUPPLY VOLTAGE

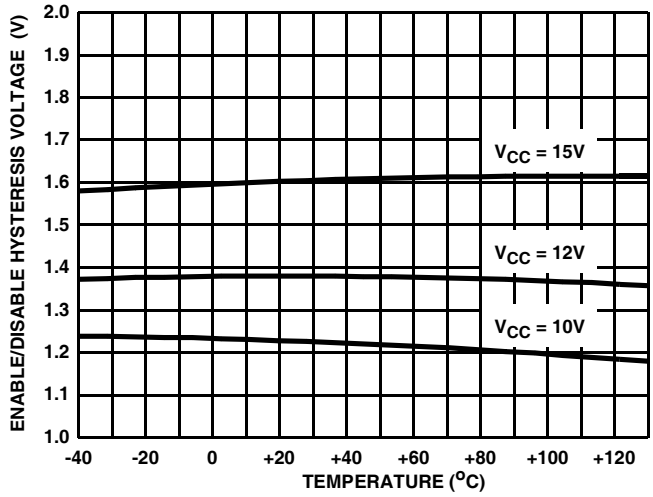


FIGURE 6. ENABLE/DISABLE HYSTERESIS VOLTAGE TEMPERATURE AND V_{CC} SUPPLY VOLTAGE

Typical Performance Curves All Curves are V_{CC} = +15V, T_A = +25°C, Unless Otherwise Specified **(Continued)**

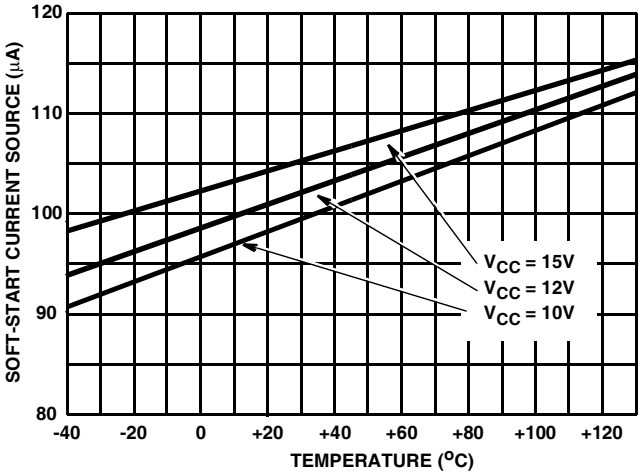


FIGURE 7. SOFT-START CURRENT SOURCE CURRENT vs TEMPERATURE AND V_{CC} SUPPLY VOLTAGE

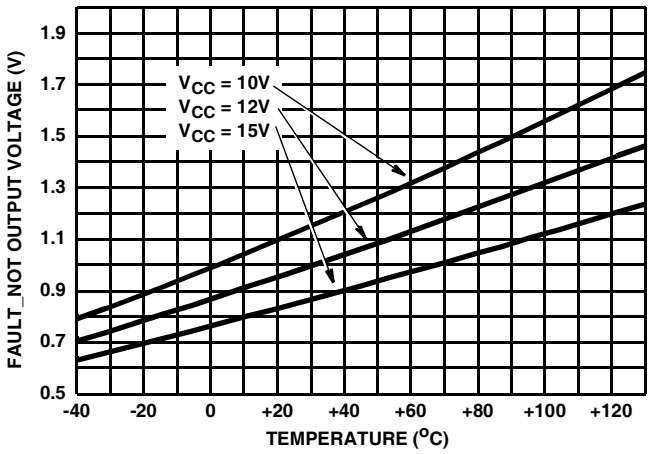


FIGURE 8. FAULT_NOT LOW LEVEL OUTPUT VOLTAGE vs TEMPERATURE AND V_{CC} SUPPLY VOLTAGE, SINKING 5mA

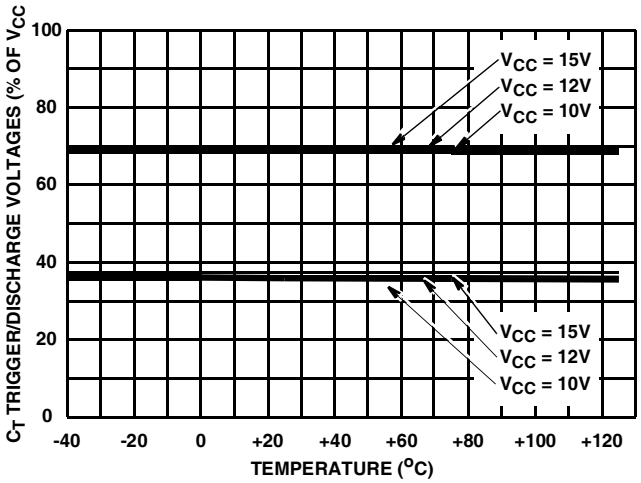


FIGURE 9. C_T RAMP TRIGGER AND DISCHARGE VOLTAGE TRIP POINT vs TEMPERATURE AND V_{CC} SUPPLY VOLTAGE

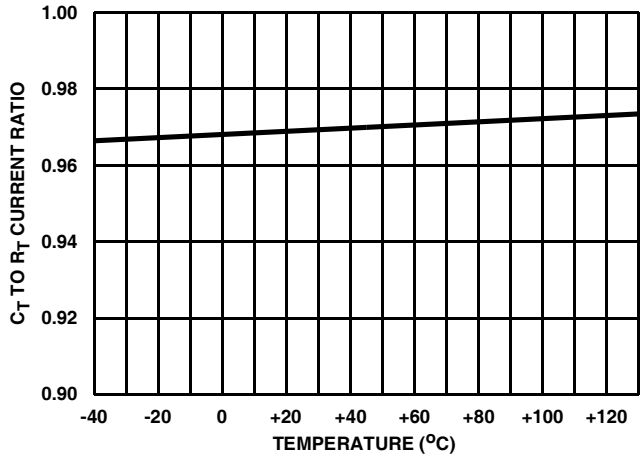


FIGURE 10. C_T TO R_T CURRENT SOURCE RATIO vs TEMPERATURE

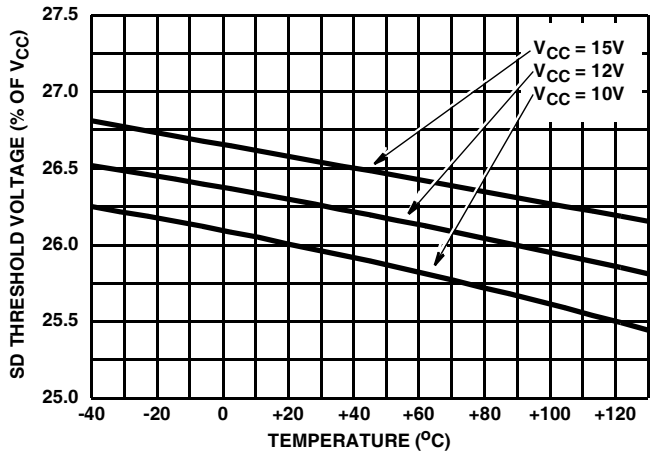


FIGURE 11. SHUTDOWN THRESHOLD VOLTAGE (% OF V_{CC}) vs TEMPERATURE AND V_{CC} SUPPLY VOLTAGE

Typical Performance Curves All Curves are V_{CC} = +15V, T_A = +25°C, Unless Otherwise Specified **(Continued)**

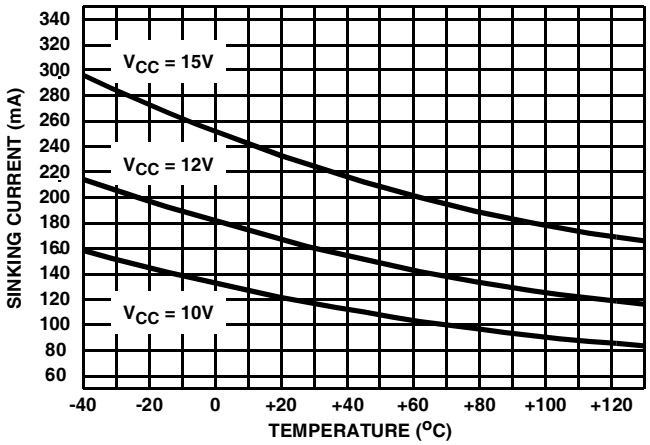


FIGURE 12. BUFFER GATE OUTPUT SHORT CIRCUIT SINKING CURRENT vs TEMPERATURE AND V_{CC} SUPPLY VOLTAGE

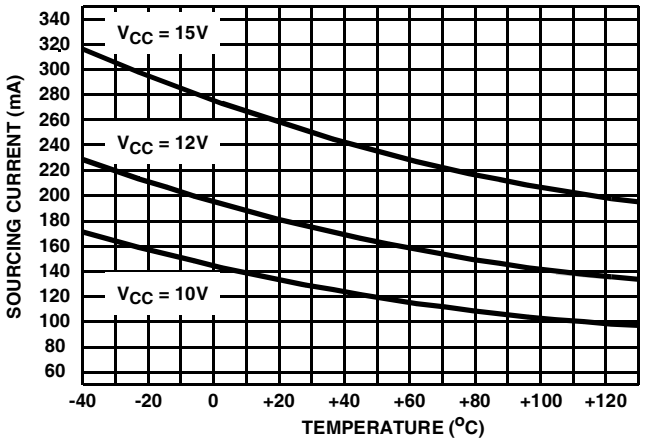


FIGURE 13. BUFFER GATE OUTPUT SHORT CIRCUIT SOURCING CURRENT vs TEMPERATURE AND V_{CC} SUPPLY VOLTAGE

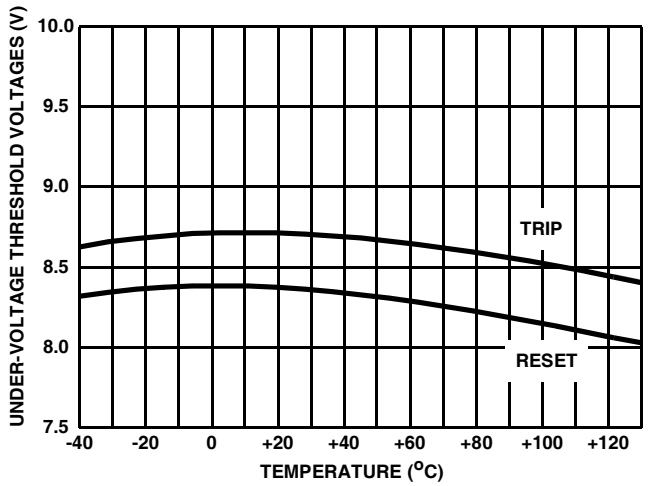


FIGURE 14. LOW-SIDE UNDERVOLTAGE THRESHOLD VOLTAGE (TRIP/RESET) vs TEMPERATURE

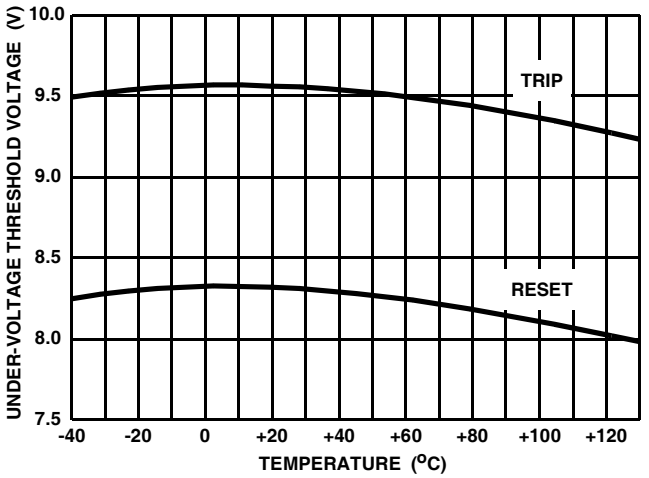


FIGURE 15. HIGH-SIDE UNDERVOLTAGE THRESHOLD VOLTAGE(TRIP/RESET) vs TEMPERATURE

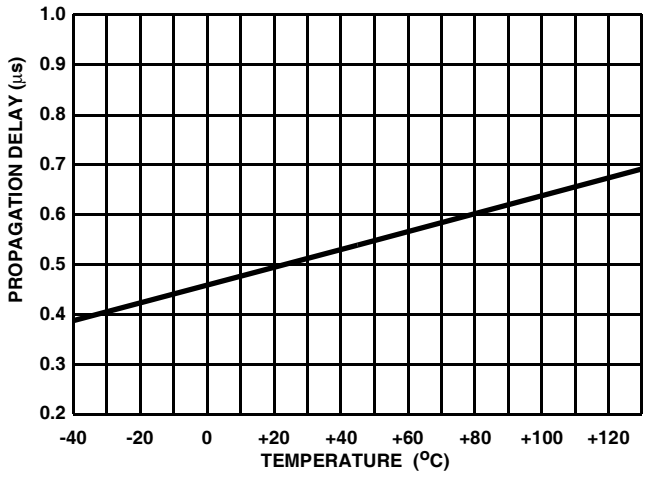


FIGURE 16. PROPAGATION DELAY, C_T TO GATE OUTPUTS vs TEMPERATURE AT V_{CC} = +15V

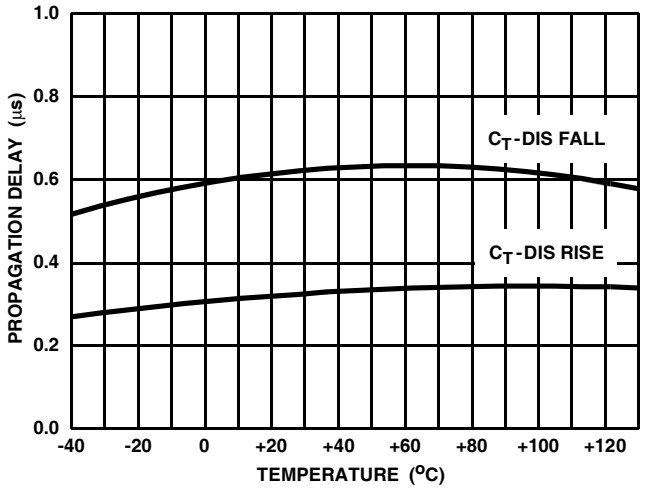


FIGURE 17. PROPAGATION DELAY, C_T TO DIS vs TEMPERATURE AT V_{CC} = +15V

Typical Performance Curves All Curves are V_{CC} = +15V, T_A = +25°C, Unless Otherwise Specified **(Continued)**

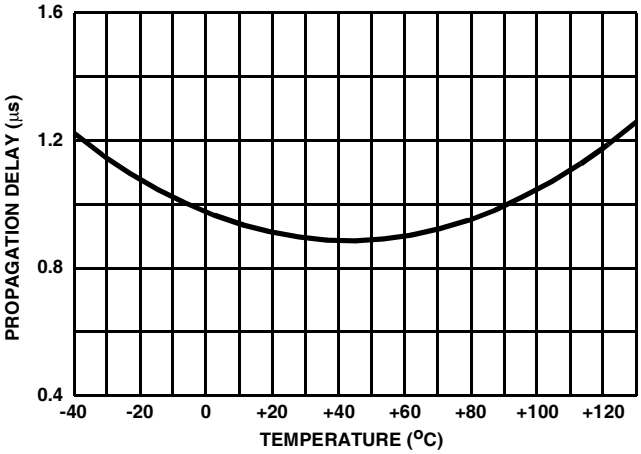


FIGURE 18. PROPAGATION DELAY, SS TO LO GATE RISING vs TEMPERATURE AT V_{CC} = +15V

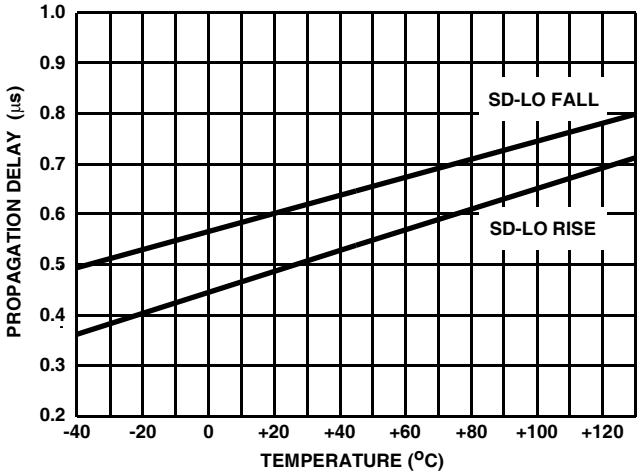


FIGURE 19. PROPAGATION DELAYS, SD TO LO GATE RISE/FALL vs TEMPERATURE AT V_{CC} = +15V

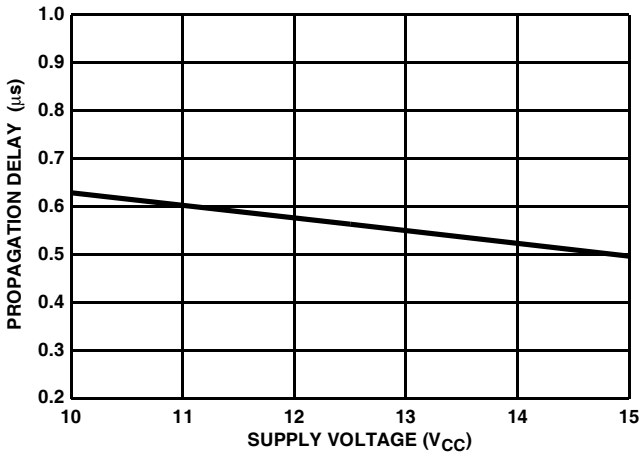


FIGURE 20. PROPAGATION DELAY, C_T TO GATE OUT vs SUPPLY VOLTAGE, V_{CC} AT +25°C FOR RISING AND FALLING GATE OUTPUTS

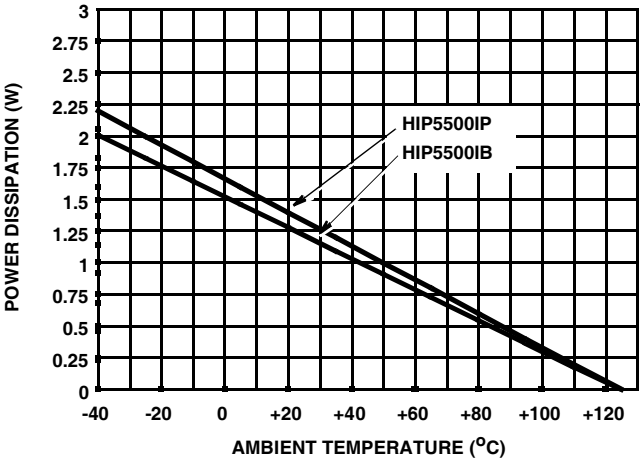


FIGURE 21. MAXIMUM POWER DISSIPATION vs TEMPERATURE

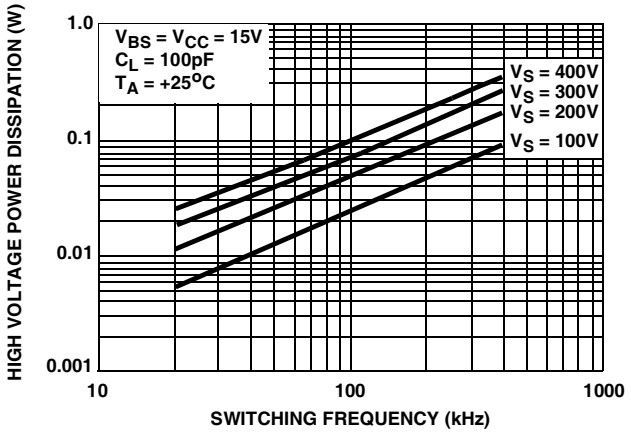
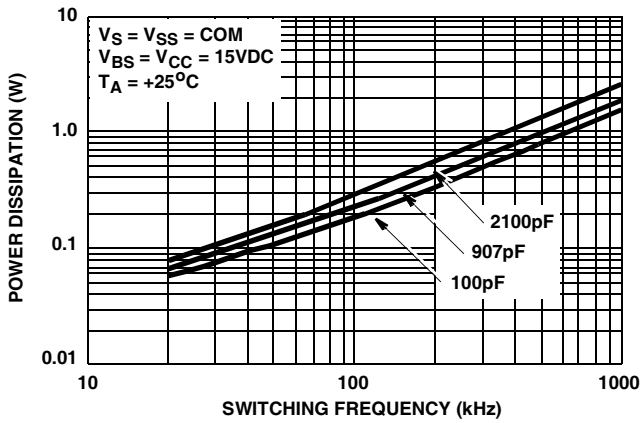


FIGURE 22. HIGH VOLTAGE POWER DISSIPATION vs SWITCHING FREQUENCY



NOTE: All switching losses assumed to be in IC.

FIGURE 23. LOW VOLTAGE POWER DISSIPATION vs FREQUENCY

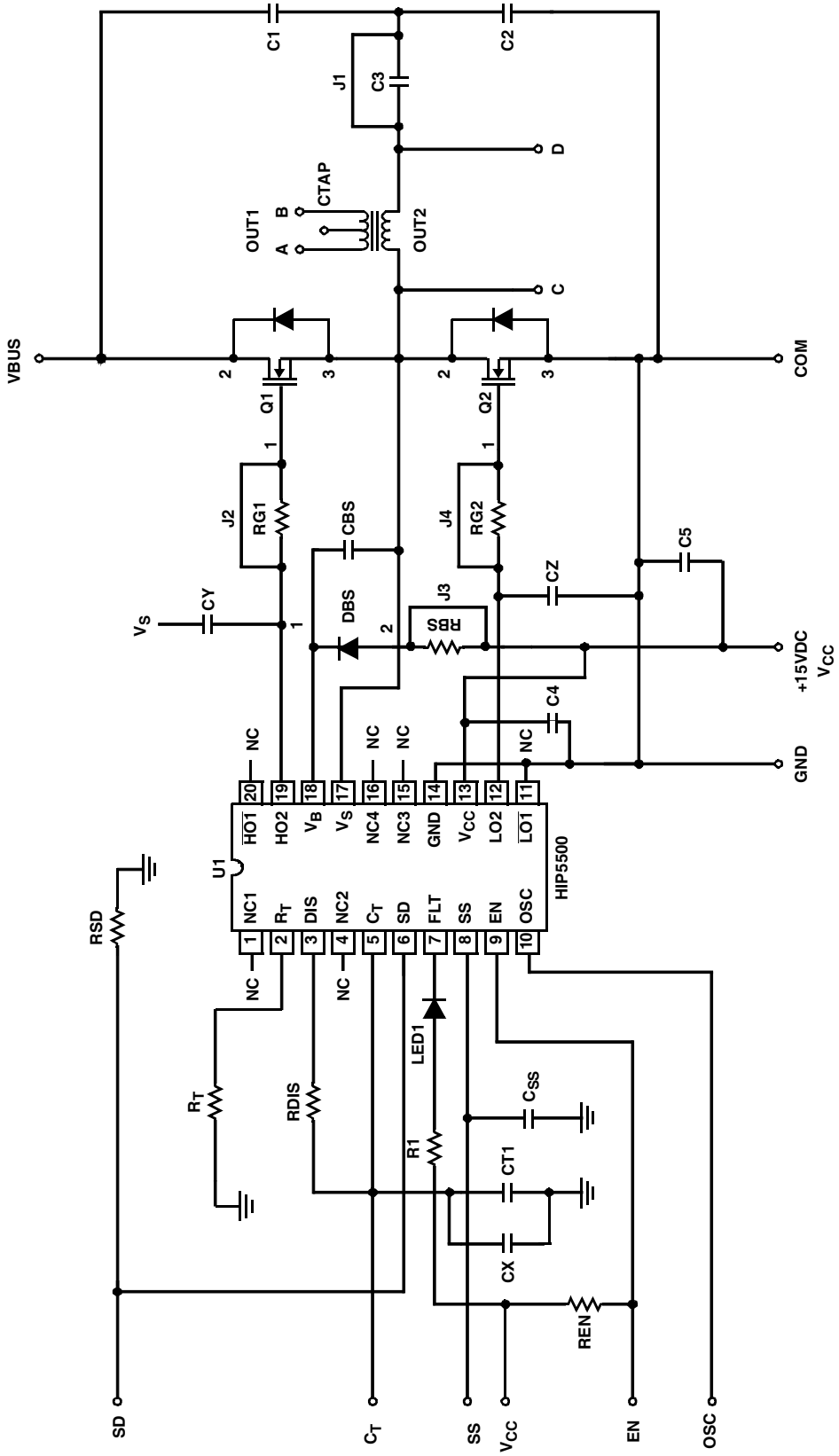


FIGURE 24. EVALUATION BOARD SCHEMATIC

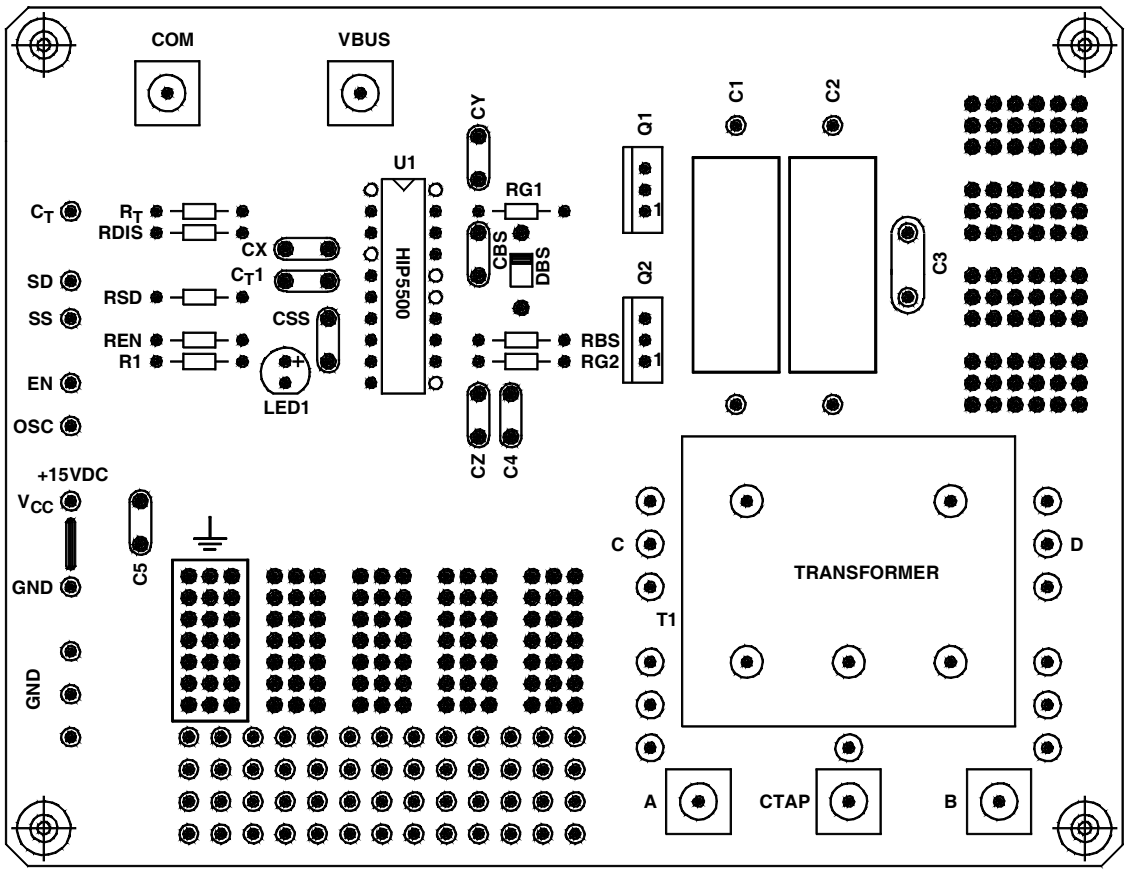
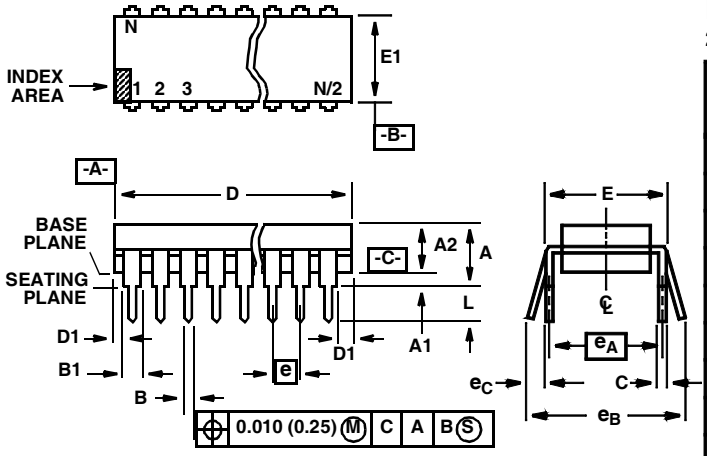


FIGURE 25. HIP5500 EVALUATION BOARD SILKSCREEN

Dual-In-Line Plastic Packages (PDIP)



E20.3 (JEDEC MS-001-AD ISSUE D)
20 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.55	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.980	1.060	24.89	26.9	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	20		20		9

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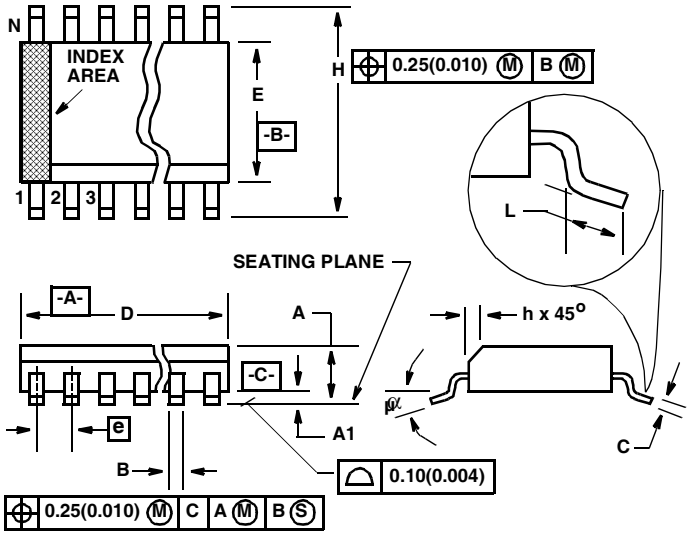
NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Small Outline Plastic Packages (SOIC)



M20.3 (JEDEC MS-013-AC ISSUE C)
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.