intersil

HD-4702/883

June 1998

CMOS Programmable Bit Rate Generator

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1. 2. 1.**
- **HD-4702/883 Provides 13 Commonly Used Bit Rates**
- **Uses a 2.4576MHz Crystal/Input for Standard Frequency Output (16 Times Bit Rate)**
- **Low Power Dissipation**
- **Conforms to EIA RS-404**
- **One HD-4702/883 Controls up to Eight Transmission Channels**
- **Initialization Circuit Facilitates Diagnostic Fault Isolation**
- **On-Chip Input Pull-Up Circuit**

Ordering Information

PART NUMBER	TEMPERATURE RANGE (^oC)	PACKAGE	PKG. NO.
HD1-4702/883	-55 to 125	CERDIP	F16.3

Description

The HD-4702/883 Bit Rate Generator provides the necessary clock signals for digital data transmission systems, such as a UART. It generates 13 commonly used bit rates using an on-chip crystal oscillator or an external input. For conventional operation generating 16 output clock pulses per bit period, the input clock frequency must be 2.4576MHz (i.e., 9600 Baud x 16 x 16, since there is an internal ÷ 16 prescaler). A lower input frequency will result in a proportionally lower output frequency.

The HD-4702/883 can provide multi-channel operation with a minimum of external logic by having the clock frequency C_O and the ÷ 8 prescaler outputs Q_0, Q_1, Q_2 available externally. All signals have a 50% duty cycle except 1800 Baud, which has less than 0.39% distortion.

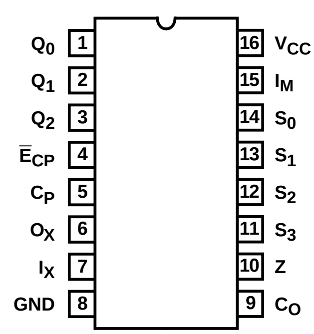
The four rate select inputs (S_0-S_3) select which bit rate is at the output (Z). See Truth Table for Rate Select Inputs for select code and output bit rate. Two of the 16 select codes for the HD-4702/883 do not select an internally generated frequency, but select an input into which the user can feed either a different frequency, or a static level (High or Low) to generate “ZERO BAUD”.

The bit rates most commonly used in modern data terminals (110,150, 300,1200, 2400 Baud) require that no more than one input be grounded for the HD-4702/883, which is easily achieved with a single 5-position switch.

The HD-4702/883 has an initialization circuit which generates a master reset for the scan counter. This signal is derived from a digital differentiator that senses the first high level on the C_P input after the $\overline{E}_{CP}$ input goes low. When $\overline{E}_{CP}$ is high, selecting the crystal input, C_P must be low. A high level on C_P would apply a continuous reset. See Clock Modes and Initialization below.

Pinout

HD-4702/883 (CERDIP)
TOP VIEW



Truth Table

TRUTH TABLE FOR RATE SELECT INPUTS
(Using 2.4576MHz Crystal)

S_3	S_2	S_1	S_0	OUTPUT RATE (Z)
L	L	L	L	MUX Input (I_M)
L	L	L	H	MUX Input (I_M)
L	L	H	L	50 Baud
L	L	H	H	75 Baud
L	H	L	L	134.5 Baud
L	H	L	H	200 Baud
L	H	H	L	600 Baud
L	H	H	H	2400 Baud
H	L	L	L	9600 Baud
H	L	L	H	4800 Baud
H	L	H	L	1800 Baud
H	L	H	H	1200 Baud
H	H	L	L	2400 Baud
H	H	L	H	300 Baud
H	H	H	L	150 Baud
H	H	H	H	110 Baud

NOTE:

1. 19200 Baud by connecting Q_2 to I_M.

CLOCK MODES AND INITIALIZATION

I_X	$\overline{E}_{CP}$	C_P	OPERATION
	H	L	Clocked from I_X
X	L		Clocked from C_P
X	H	H	Continuous Reset
X	L		Reset During First C_P = High Time

NOTE:

2. Actual output frequency is 16 times the indicated output rate, assuming a clock frequency of 2.4576MHz.

H = HIGH Level
L = LOW Level
X = Don't Care
 = Clock Pulse
 = First HIGH Level Clock Pulse after $\overline{E}_{CP}$ goes LOW

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1
Typical Derating Factor . . . . . 1mA/MHz Increase in ICCOP

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55°C to 125°C

Thermal Information

Thermal Resistance, (Typical, Note 3)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	78	23

Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Junction Temperature . . . . . 175°C
Maximum Lead Temperature (Soldering, 10s) . . . . . 300°C

Die Characteristics

Gate Count . . . . . 720 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

TABLE 1. DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

DC PARAMETER	SYMBOL	CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Input High Voltage	V_{IH}	V_{CC} = 4.5V	1, 2, 3	$-55 \le T_A \le 125$	V_{CC} 70%	-	V
Input Low Voltage	V_{IL}	V_{CC} = 4.5V	1, 2, 3	$-55 \le T_A \le 125$	-	V_{CC} 30%	V
Output High Voltage	V_{OH1}	$I_{OH} \le -1\mu A$, V_{CC} = 4.5V, (Note 4)	1, 2, 3	$-55 \le T_A \le 125$	V_{CC} -0.1	-	V
Output Low Voltage	V_{OL1}	$I_{OL} \le +1\mu A$, V_{CC} = 4 5V, (Note 4)	1, 2, 3	$-55 \le T_A \le 125$	-	0.1	V
Input High Current	I_{IH}	$V_{IN} = V_{CC}$. All Other Pins = 0V, V_{CC} = 5.5V	1, 2, 3	$-55 \le T_A \le 125$	-1	+1	µA
Input Low Current (IX Input)	I_{ILX}	V_{IN} = 0V, All Other Pins = V_{CC}, V_{CC} = 5.5V	1, 2, 3	$-55 \le T_A \le 125$	-1	+1	µA
Input Low Current (All Other Inputs)	I_{IL}	V_{IN} = 0V All Other Pins = V_{CC}, V_{CC} = 5.5V (Note 5)	1, 2, 3	$-55 \le T_A \le 125$	-	-100	µA
Output High Current (OX)	I_{OHX}	$V_{OUT} = V_{CC}$ -0.5, V_{CC} = 4.5V Input at 0V or V_{CC} per Logic Function or Truth Table	1, 2, 3	$-55 \le T_A \le 125$	-0.1	-	mA
Output High Current (All Other Outputs)	I_{OH1}	V_{OUT} = 2.5V, V_{CC} = 4.5V Input at 0V or V_{CC} per Logic Function or Truth Table	1, 2, 3	$-55 \le T_A \le 125$	-1.0	-	mA
Output High Current (All Other Outputs)	I_{OH2}	$V_{OUT} = V_{CC}$ -0.5, V_{CC} = 4.5V Input at 0V or V_{CC} per Logic Function or Truth Table	1, 2, 3	$-55 \le T_A \le 125$	-0.3	-	mA
Output Low Current (OX)	I_{OLX}	V_{OUT} = 0.4V, V_{CC} = 4.5V Input at 0V or V_{CC} per Logic Function or Truth Table	1, 2, 3	$-55 \le T_A \le 125$	0.1	-	mA
Output Low Current (All Other Outputs)	I_{OL}	V_{OUT} = 0.4V, V_{CC} = 4.5V Input at 0V or V_{CC} per Logic Function or Truth Table	1, 2, 3	$-55 \le T_A \le 125$	1.6	-	mA

TABLE 1. DC ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

Device Guaranteed and 100% Tested

DC PARAMETER	SYMBOL	CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE (^oC)	MIN	MAX	UNITS
Supply Current (Static)	I_{CC}	$\overline{E}CP = V_{CC}$, CP = 0V, V_{CC} = 5.5V All Other Inputs = GND, (Note 5)	1, 2, 3	$-55 \leq T_A \leq 125$	-	1500	µA
		$\overline{E}CP = V_{CC}$, CP = 0V, V_{CC} = 5.5V All Other Inputs = V_{CC} (Note 5)	1, 2, 3	$-55 \leq T_A \leq 125$	-	1000	µA

NOTES:

4. Interchanging of force and sense conditions is permitted.
5. Input Current and Quiescent Power Supply Current are relatively higher for this device because of active pull-up circuits on all inputs except I_X.

TABLE 2. AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested.

AC PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (^oC)	MIN	MAX	UNITS
Propagation Delay, I_X to C_O	t_{PLH}	V_{CC} = 4.5V $C_L \leq$ 7pF on OX C_L = 50pF (Note 6)	9, 10, 11	$-55 \leq T_A \leq 125$	-	350	ns
Propagation Delay, I_X to C_O	t_{PHL}		9, 10, 11	$-55 \leq T_A \leq 125$	-	275	ns
Propagation Delay, C_P to C_O	t_{PLH}		9, 10, 11	$-55 \leq T_A \leq 125$	-	260	ns
Propagation Delay, C_P to C_O	t_{PHL}		9, 10, 11	$-55 \leq T_A \leq 125$	-	220	ns
Propagation Delay, C_O to Q_n	t_{PLH}		9, 10, 11	$-55 \leq T_A \leq 125$	-	(Note 7)	ns
Propagation Delay, C_O to Qn	t_{PHL}		9, 10, 11	$-55 \leq T_A \leq 125$	-	(Note 7)	ns
Propagation Delay, C_O to Z	t_{PLH}		9, 10, 11	$-55 \leq T_A \leq 125$	-	85	ns
Propagation Delay, C_O to Z	t_{PHL}		9, 10, 11	$-55 \leq T_A \leq 125$	-	75	ns
Output Transition Time (Except O_X)	t_{TLH}		9, 10, 11	$-55 \leq T_A \leq 125$		160	ns
Output Transition Time (Except O_X)	t_{THL}		9, 10, 11	$-55 \leq T_A \leq 125$	-	75	ns
Set-UpTime Select to C_O	t_S		9, 10, 11	$-55 \leq T_A \leq 125$	350	-	ns
Hold Time, Select to C_O	t_H		9, 10, 11	$-55 \leq T_A \leq 125$	0	-	ns
Set-UpTime, I_M to C_O	t_S		9, 10, 11	$-55 \leq T_A \leq 125$	350	-	ns
Hold Time, I_M to C_O	t_H		9, 10, 11	$-55 \leq T_A \leq 125$	0	-	ns
Minimum Clock Pulse Width, Low (Notes 8, 9)	$t_{WCP(L)}$		9, 10, 11	$-55 \leq T_A \leq 125$	120		ns
Minimum Clock Pulse Width, High (Notes 8, 9)	$t_{WCP(H)}$		9, 10, 11	$-55 \leq T_A \leq 125$	120	-	ns
Minimum I_X Pulse Width, Low (Note 9)	$t_{WCP(L)}$		9, 10, 11	$-55 \leq T_A \leq 125$	160	-	ns
Minimum I_X Pulse Width, High (Note 9)	$t_{WCP(H)}$		9, 10, 11	$-55 \leq T_A \leq 125$	160	-	ns

NOTES:

6. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-Up Times (t_S), Hold Times (t_H), and Minimum Pulse Widths (t_W) do not vary with load capacitance.
7. For multichannel operation, Propagation Delay (C_O to Q_n), plus Set-Up Time, Select to C_O, is guaranteed to be $\leq$ 367ns.
8. The first High Level Clock Pulse alter $\overline{E}_{CP}$ goes Low must be at least 350ns long to guarantee reset of all Counters.
9. It is recommended that input rise and fall times to the clock inputs (C_P, I_X) be less than 15ns.

TABLE 3. ELECTRICAL PERFORMANCE SPECIFICATIONS

AC PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE (^oC)	MIN	MAX	UNITS
Input Capacitance	C_{IN}	All Measurements are referenced to device ground, f = 1MHz.	10	T_A = 25	-	7.0	pF
Output Capacitance	C_O		10	T_A = 25	-	15.0	pF
Propagation Delay I_X to C_O	t_{PLH}	V_{CC} = 4.5V $C_L \leq$ 7pF on O_X C_L = 15pF	10, 12	$-55 \leq T_A \leq 125$	-	300	ns
Propagation Delay I_X to C_O	t_{PHL}		10, 12	$-55 \leq T_A \leq 125$	-	250	ns
Propagation Delay C_P to C_O	t_{PLH}		10, 12	$-55 \leq T_A \leq 125$	-	215	ns
Propagation Delay C_P to C_O	t_{PHL}		10, 12	$-55 \leq T_A \leq 125$	-	195	ns
Propagation Delay C_O to Q_n	t_{PLH}		10, 12	$-55 \leq T_A \leq 125$	-	(Note 11)	ns
Propagation Delay C_O to Q_n	t_{PHL}		10, 12	$-55 \leq T_A \leq 125$	-	(Note 11)	ns
Propagation Delay C_O to Z	t_{PLH}		10, 12	$-55 \leq T_A \leq 125$	-	75	ns
Propagation Delay C_O to Z	t_{PHL}		10, 12	$-55 \leq T_A \leq 125$	-	65	ns
Output Transition Time (Except O_X)	t_{TLH}		10, 12	$-55 \leq T_A \leq 125$	-	80	ns
Output Transition Time (Except O_X)	t_{THL}		10, 12	$-55 \leq T_A \leq 125$	-	40	ns

NOTES:

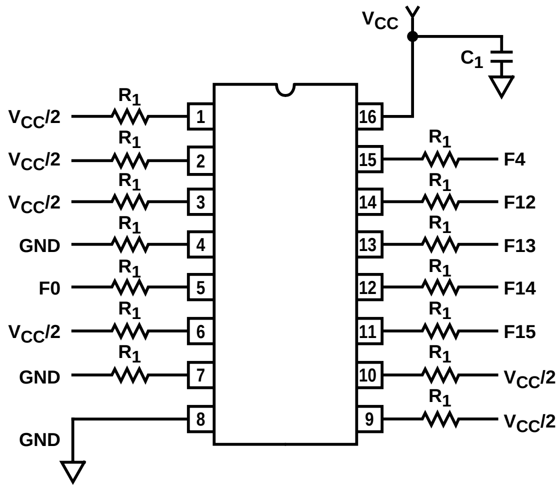
10. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
11. For multichannel operation, Propagation Delay (C_O to Qn) plus Set-Up Time, Select to C_O, is guaranteed to be ≤ 367ns.
12. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-Up Times (t_S), Hold Times (t_H), and Minimum Pulse Widths (t_W) do not vary with load capacitance.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C and D	Samples/5005	1, 7, 9

Burn-In Circuit

HD-4702/883 CERDIP



NOTES:

13. F0 = 100kHz ±10%, F1 = F0/2, F2 = F1/2., ...
14. R_1 = 10kΩ, 1/4W, ±10%.
15. V_{CC} = 5.5V ±0.5V, GND = 0V.
16. C_1 = 0.01μF Min.

Die Characteristics

DIE DIMENSIONS:

100 mils x 97 mils x 19 mils

METALLIZATION:

Type: Si - Al
Thickness: 10kÅ - 12kÅ

GLASSIVATION:

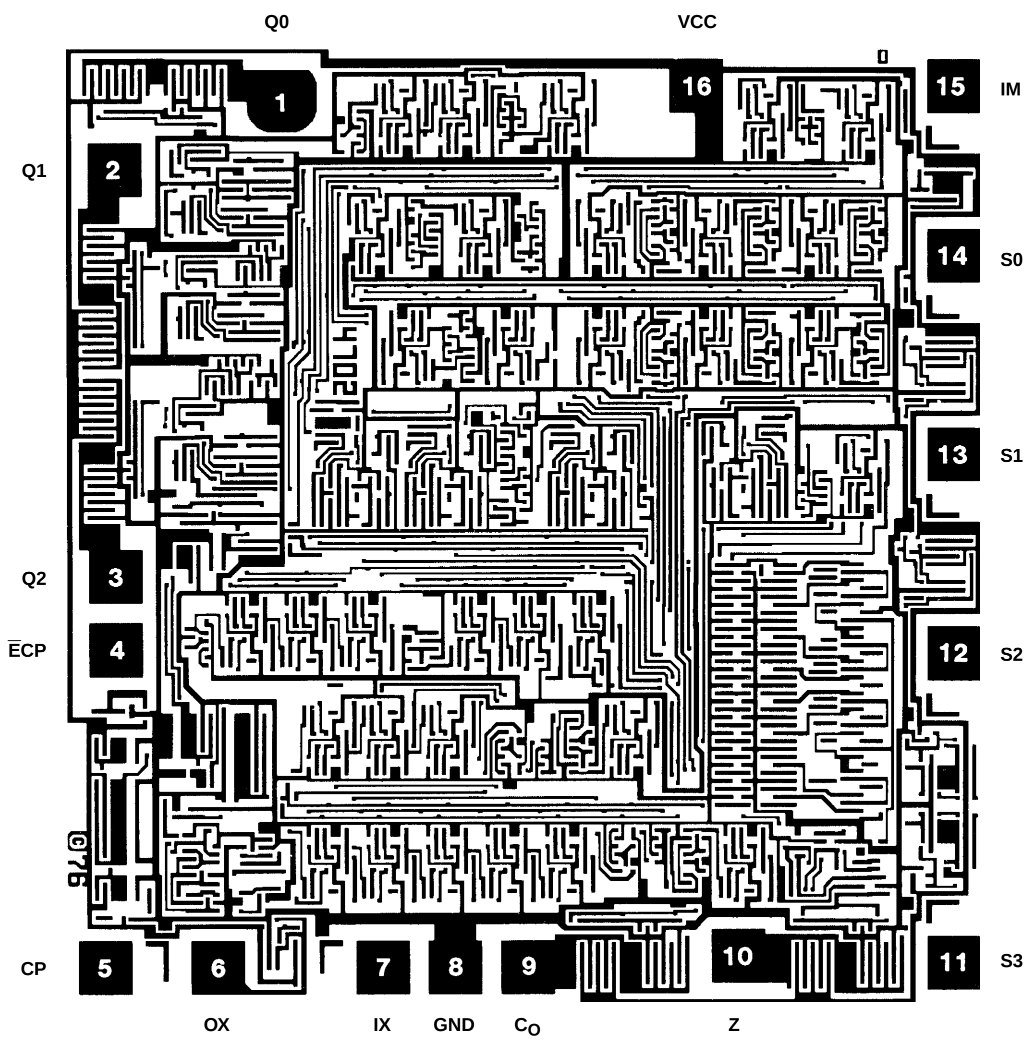
Type: SiO_2
Thickness: 7kÅ - 9kÅ

WORST CASE CURRENT DENSITY:

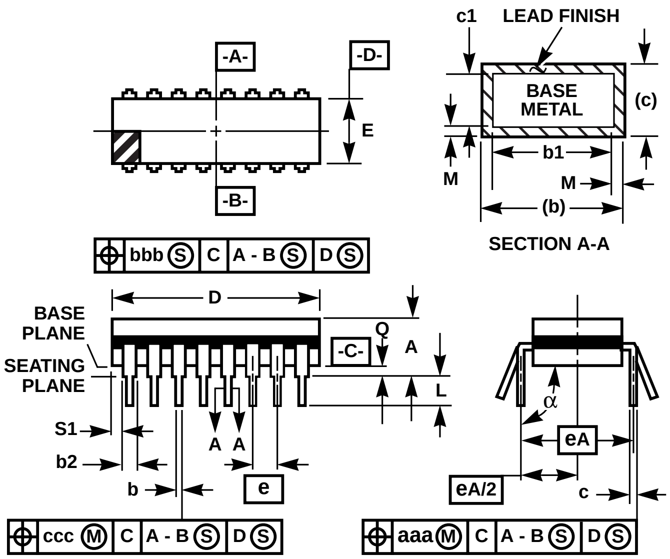
$7.1 \times 10^4 A/cm^2$

Metallization Mask Layout

HD-4702/883



Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F16.3 **MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)**
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

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