DRAM

1 MEG x 16 DRAM

3.3V, EDO PAGE MODE, OPTIONAL EXTENDED REFRESH

AVAILABLE AS MILITARY SPECIFICATIONS

- MIL-STD 883
- SMD Planned

FEATURES

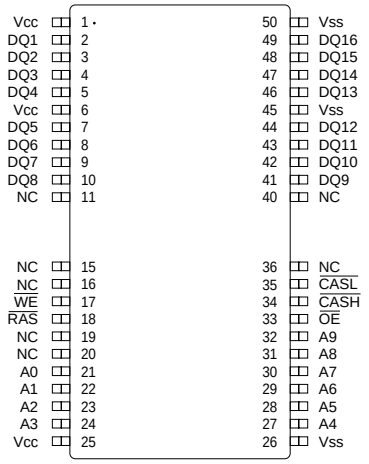
- JEDEC- and industry-standard x16 timing, functions, pinouts and packages
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All device pins are TTL-compatible
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN
- BYTE WRITE access cycles
- 1,024-cycle refresh (10 row-, 10 column-addresses)
- Low power, 0.3mW standby; 180mW active, typical
- Extended Data-Out (EDO) PAGE access cycle
- 5V-tolerant I/Os (5.5V maximum V_{IH} level)

OPTIONS — MARKING

- Timing
  - 60ns access (Contact Factory) — -6
  - 70ns access — -7
  - 80ns access — -8
- Refresh Rate
  - Standard 16ms period — None
- Packages
  - Ceramic SOJ — ECJ — No. 506
  - Ceramic Gull Wing — ECG — No. 604
  - Ceramic LCC — EC — No. 213

PIN ASSIGNMENT (Top View)

44/50-Pin SOJ/LCC/Gull Wing
450mil



KEY TIMING PARAMETERS

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tCAS
-6	105ns	60ns	25ns	30ns	15ns	12ns
-7	125ns	70ns	30ns	35ns	20ns	12ns
-8	150ns	80ns	40ns	40ns	20ns	20ns

GENERAL DESCRIPTION

The AS4LC1M16 is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x16 configuration. The AS4LC1M16 has both BYTE WRITE and WORD WRITE access cycles via two $\overline{CAS}$ pins ($\overline{CASL}$ and $\overline{CASH}$). These function in a similar manner to a single $\overline{CAS}$ of other DRAMs in that either $\overline{CASL}$ or $\overline{CASH}$ will generate an internal $\overline{CAS}$.

The AS4LC1M16 $\overline{CAS}$ function and timing are determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and the last $\overline{CAS}$ to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{CASL}$ transitioning LOW selects an access cycle for the lower byte (DQ1-DQ8) and $\overline{CASH}$ transitioning LOW selects an access cycle for the upper byte (DQ9-DQ16).

Each bit is uniquely addressed through the 20 address bits during READ or WRITE cycles. These are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. The $\overline{CAS}$ function also determines whether the cycle will be a refresh cycle ($\overline{RAS}$ ONLY) or an active cycle (READ, WRITE or READ WRITE) once $\overline{RAS}$ goes LOW.

GENERAL DESCRIPTION (continued)

The CASL and CASH inputs internally generate a CAS signal functioning in a similar manner to the single CAS input of other DRAMs. The key difference is each CAS input (CASL and CASH) controls its corresponding 8 DQ inputs during WRITE accesses. CASL controls DQ1 through DQ8 and CASH controls DQ9 through DQ16. The two CAS controls give the MT4LC1M16E5(S) both BYTE READ and BYTE WRITE cycle capabilities.

A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS (CASL or CASH), whichever occurs last. An EARLY WRITE occurs when WE is taken LOW prior to either CAS falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE falls after CAS (CASL or CASH) was taken LOW. During EARLY WRITE cycles, the data-outputs (Q) will remain High-Z regardless of the state of OE. During LATE WRITE or READ-MODIFY-WRITE cycles, OE must be taken HIGH to disable the data-outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE LOW, no write will occur, and the data-outputs will drive read data from the accessed location.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O. Pin direction is controlled by OE and WE.

PAGE ACCESS

PAGE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined page boundary. The PAGE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the PAGE MODE of operation.

EDO PAGE MODE

The AS4LC1M16 provides EDO PAGE MODE which is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS returns HIGH. EDO provides for CAS precharge time (^{t}CP) to occur without the output data going invalid. This elimination of CAS output control provides for pipeline READs.

FAST-PAGE-MODE DRAMs have traditionally turned the output buffers off (High-Z) with the rising edge of CAS. EDO-PAGE-MODE DRAMs operate similar to FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after CAS goes HIGH during READs, provided RAS and OE are held LOW. If OE is pulsed while RAS and CAS are LOW, data will toggle from valid data to High-Z and back to the same valid data. If OE is toggled or pulsed after CAS goes HIGH while RAS remains LOW, data will transition to and remain High-Z (refer to Figure 1).

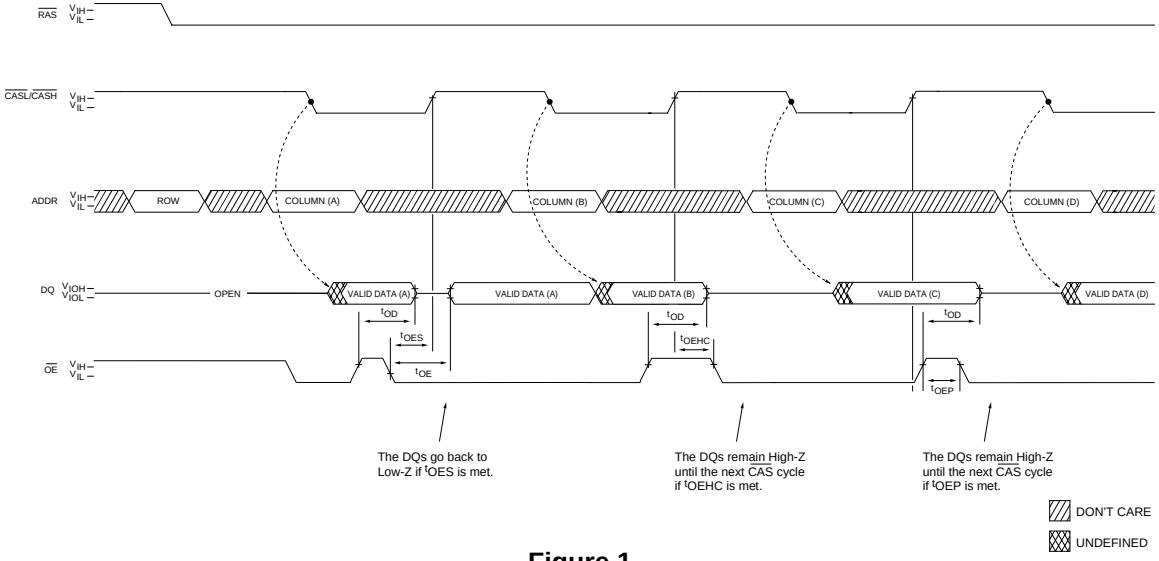


Figure 1
OUTPUT ENABLE AND DISABLE

EDO PAGE MODE (continued)

$\overline{WE}$ can also perform the function of disabling the output drivers under certain conditions, as shown in Figure 2.

During an application, if the DQ outputs are wire OR'd, $\overline{OE}$ must be used to disable idle banks of DRAMs. Alternatively, pulsing $\overline{WE}$ to the idle banks during $\overline{CAS}$ HIGH time will also High-Z the outputs. Independent of $\overline{OE}$ control, the outputs will disable after ^{t}OFF, which is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

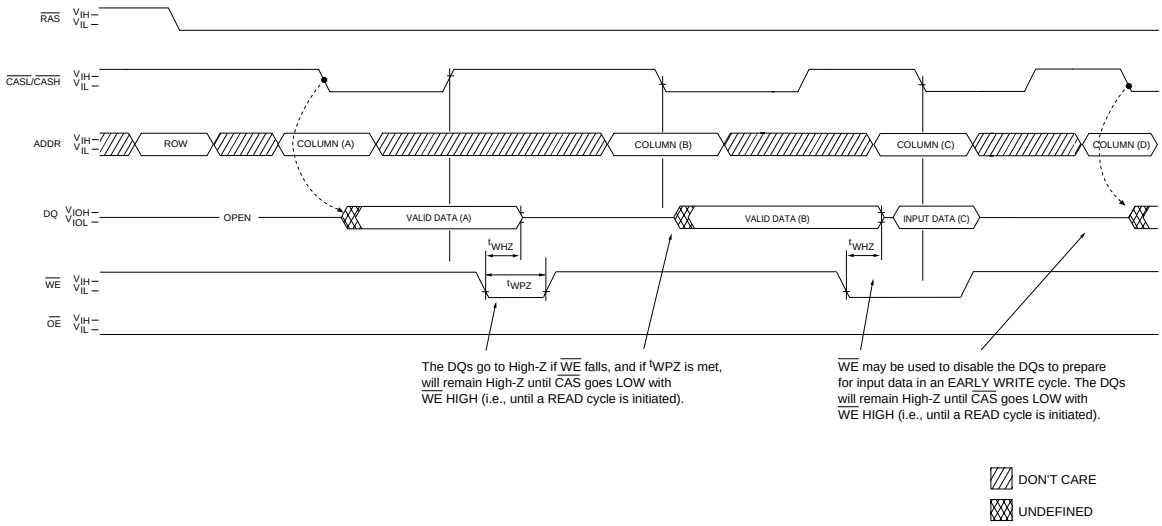


Figure 2
$\overline{WE}$ CONTROL OF DQs

BYTE ACCESS CYCLE

The BYTE WRITEs and BYTE READs are determined by the use of $\overline{CASL}$ and $\overline{CASH}$. Enabling $\overline{CASL}$ will select a lower BYTE access (DQ1-DQ8). Enabling $\overline{CASH}$ will select an upper BYTE access (DQ9-DQ16). Enabling both $\overline{CASL}$ and $\overline{CASH}$ selects a WORD WRITE cycle.

The AS4LC1M16 may be viewed as two 1 Meg x 8 DRAMs that have common input controls, with the exception of the $\overline{CAS}$ inputs. Figure 3 illustrates the BYTE WRITE and WORD WRITE cycles.

Additionally, both bytes must always be of the same mode of operation if both bytes are active. A $\overline{CAS}$ precharge must be satisfied prior to changing modes of operation between the upper and lower bytes. For example, an EARLY WRITE on one byte and a LATE WRITE on the other byte is not allowed during the same cycle. However, an EARLY WRITE on one byte and, after a $\overline{CAS}$ precharge has been satisfied, a LATE WRITE on the other byte is permissable.

REFRESH

Preserve correct memory cell data by maintaining power and executing a $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses are executed at least every 16ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic $\overline{RAS}$ addressing.

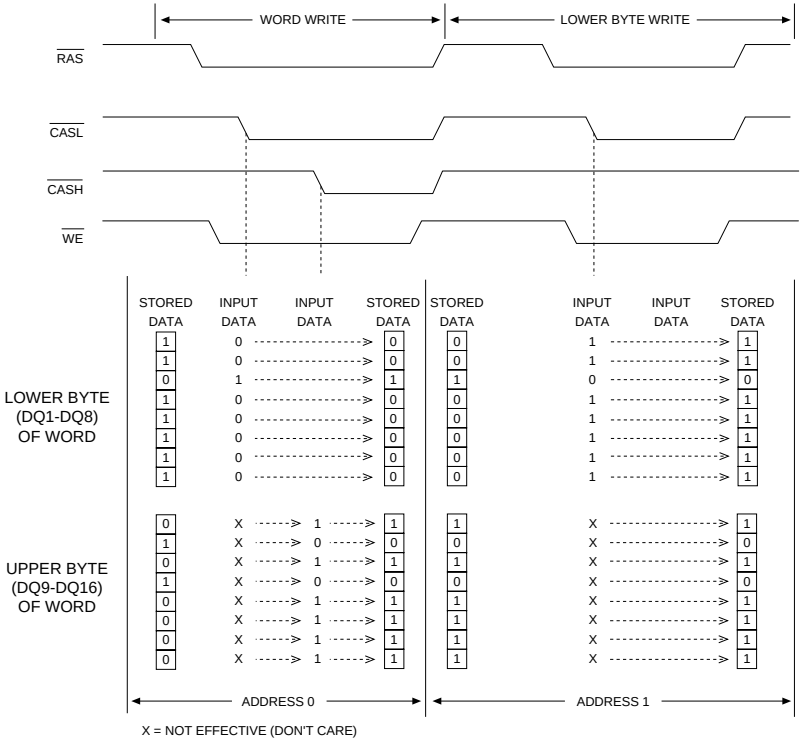
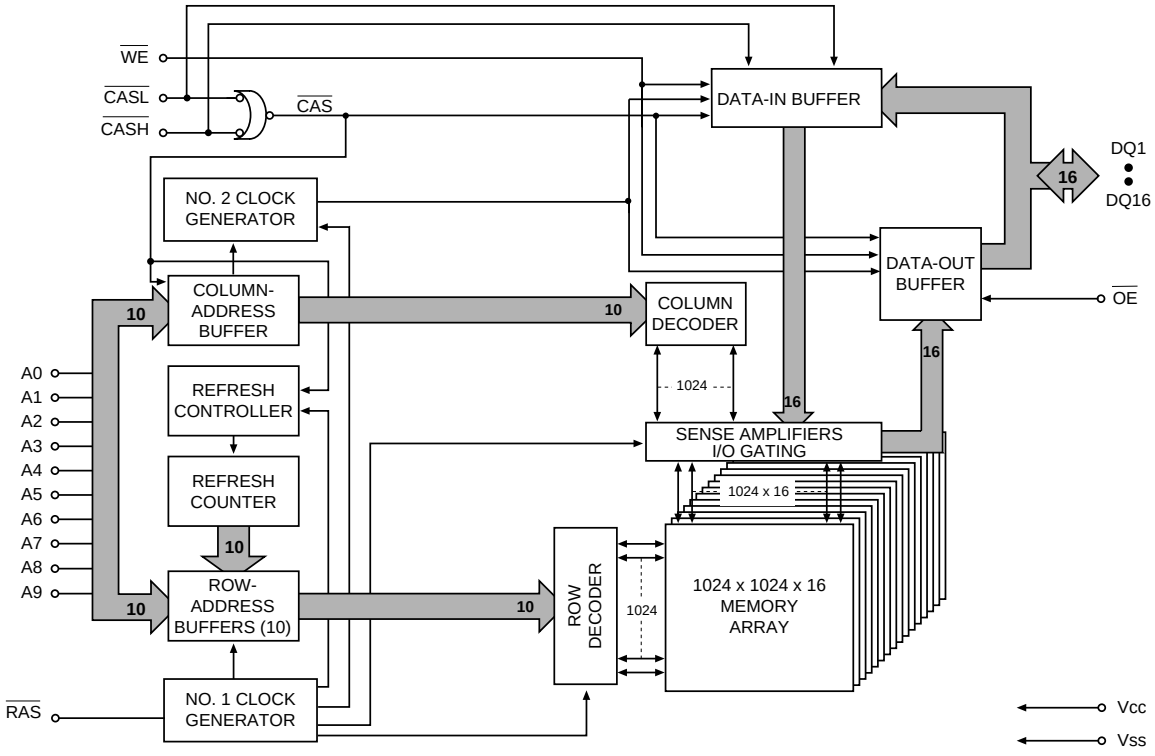


Figure 3
WORD AND BYTE WRITE EXAMPLE

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

FUNCTION		RAS	CASL	CASH	WE	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Upper Byte, Data-Out	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte	
WRITE: WORD (EARLY WRITE)		L	L	L	L	X	ROW	COL	Data-In	
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	
READ WRITE		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
EDO-PAGE-MODE	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
READ	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	2
	Any Cycle	L	L→H	L→H	H	L	n/a	n/a	Data-Out	2
EDO-PAGE-MODE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1
WRITE	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1
EDO-PAGE-MODE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
READ-WRITE	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 2
HIDDEN	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	2
REFRESH	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 3
RAS-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	L	H	X	X	X	High-Z	4

NOTE: 1. These WRITE cycles may also be BYTE WRITE cycles (either CASL or CASH active).
2. These READ cycles may also be BYTE READ cycles (either CASL or CASH active).
3. EARLY WRITE only.
4. Only one CAS must be active (CASL or CASH).

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} pin Relative to V_{SS} ..... -1.0V to +4.6V
Voltage on NC, Inputs or I/O pins
Relative to Vss ..... -1.0V to +5.5V
Operating Temperature, T_A (ambient) ..... T_A(MIN)=-55°C
..... T_C(MAX)=125°C
Storage Temperature ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs (including NC pins)	V_{IH}	2.0	V_{CC}+1	V	
Input Low (Logic 0) Voltage, all inputs (including NC pins)	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 5.5V V_{CC} = 3.6V (All other pins not under test = 0V)	I_I	-2	2	µA	4
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V) V_{CC}=3.6V	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.0mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2.0mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = other inputs = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$ address cycling: ^tRC = ^tRC [MIN])	I_{CC3}	170	155	140	mA	5, 6
OPERATING CURRENT: EDO PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: ^tPC = ^tPC [MIN])	I_{CC4}	130	120	110	mA	5, 6
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	160	145	130	mA	5, 6
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$ address cycling: ^tRC = ^tRC [MIN])	I_{CC6}	150	140	130	mA	5, 7

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Addresses	C_{I1}	7	pF	8
Input Capacitance: $\overline{RAS}$, $\overline{CASL}$,$\overline{CASH}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	8
Input/Output Capacitance: DQ	C_{IO}	8	pF	8

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 2, 3, 6, 9, 10, 11, 12,) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		30		35		40	ns	
Column-address set-up to $\overline{CAS}$ precharge	^tACH	15		15		25		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	45		50		60		ns	
Column-address setup time	^tASC	0		0		0		ns	25
Row-address setup time	^tASR	0		0		0		ns	25
Column-address to $\overline{WE}$ delay time	^tAWD	55		60		65		ns	13
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	14, 26
Column-address hold time	^tCAH	10		12		15		ns	25
$\overline{CAS}$ pulse width	^tCAS	12	10,000	13	10,000	15	10,000	ns	27
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		12		15		ns	7, 28
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ to return HIGH	^tCLCH	10		10		15		ns	29
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	26
Data output hold after next $\overline{CAS}$ LOW	^tCOH	3		3		3		ns	
$\overline{CAS}$ precharge time	^tCP	10		10		10		ns	15, 30
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		40	ns	26
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	28
$\overline{CAS}$ hold time	^tCSH	50		55		60		ns	28
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	5		5		10		ns	7, 25
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	35		40		45		ns	13, 25
Write command to $\overline{CAS}$ lead time	^tCWL	15		15		20		ns	28
Data-in hold time	^tDH	10		12		15		ns	16, 26
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Data-in setup time	^tDS	0		0		0		ns	16, 26
Output disable	^tOD	0	15	0	15	0	15	ns	
Output Enable	^tOE		15		20		20	ns	17, 26
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	12		12		15		ns	18
$\overline{OE}$ HIGH hold from $\overline{CAS}$ HIGH	^tOEHC	10		10		10		ns	18
$\overline{OE}$ HIGH pulse width	^tOEP	10		10		10		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

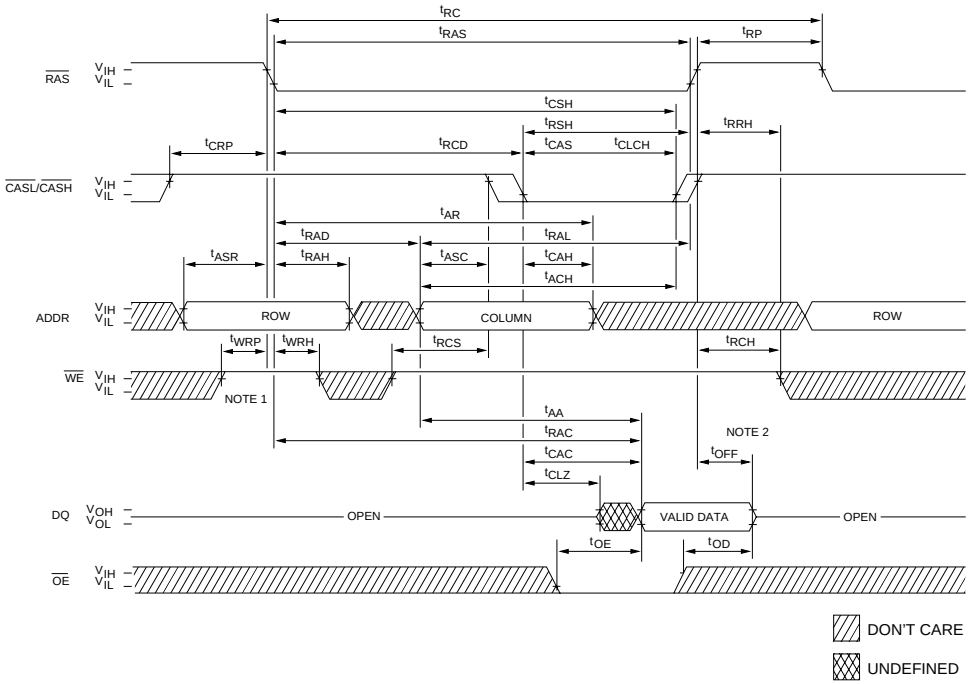
(Notes: 2, 3, 6, 9, 10, 11, 12, 20) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{OE}$ LOW to $\overline{CAS}$ HIGH setup time	^tOES	5		5		10		ns	
Output buffer turn-off delay	^tOFF	0	15	0	15	0	20	ns	20, 26
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	^tPC	30		35		40		ns	31
EDO-PAGE-MODE READ-WRITE cycle time	^tPRWC	75		85		90		ns	31
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	19
$\overline{RAS}$ to column-address delay time	^tRAD	12	30	12	35	15	40	ns	21
Row-address hold time	^tRAH	10		10		10		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
$\overline{RAS}$ pulse width	^tRAS	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ pulse width (EDO PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	14	45	14	50	16	60	ns	22, 25
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	23, 28
Read command setup time	^tRCS	0		0		0		ns	25
Refresh period (1,024 cycles)	^tREF		16		16		16	ms	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	5		5		5		ns	
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	23
$\overline{RAS}$ hold time	^tRSH	13		15		20		ns	32
READ WRITE cycle time	^tRWC	150		180		200		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	80		90		105		ns	13
Write command to $\overline{RAS}$ lead time	^tRWL	15		18		20		ns	
Transition time (rise or fall)	^tT	2	50	2	50	2	50	ns	
Write command hold time	^tWCH	10		12		15		ns	32
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	13, 25
Output disable delay from $\overline{WE}$	^tWHZ	0	13	0	15	0	20	ns	
Write command pulse width	^tWP	10		12		15		ns	
$\overline{WE}$ pulse width to disable at $\overline{CAS}$ HIGH	^tWPZ	10		12		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		10		ns	
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		10		ns	

NOTES

1. All voltages referenced to V_{SS}.
2. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0^{\circ}C \leq T_A \leq 70^{\circ}C$) is assured.
3. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. NC pins are assumed to be left floating and are not tested for leakage.
5. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
6. Column address changed once each cycle.
7. Enables on-chip refresh and address counters.
8. This parameter is sampled. V_{CC} = +3.0V; f = 1 MHz.
9. AC characteristics assume ^{t}T = 2.5ns.
10. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
11. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
12. Measured with a load equivalent to two TTL gates, 100pF and V_{OL} = 0.8V and V_{OH} = 2.0V.
13. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}WCS < {}^{t}WCS$ (MIN) and $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
14. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
15. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
16. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
17. If $\overline{OE}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted. Additionally, $\overline{WE}$ must be pulsed during $\overline{CAS}$ HIGH time in order to place I/O buffers in High-Z.
18. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
19. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}. It is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.
21. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA, provided ^{t}RCD is not exceeded.
22. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC, provided ^{t}RAD is not exceeded.
23. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
24. The first $\overline{CAS}x$ edge to transition LOW.
25. Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input; DQ1-DQ8 by $\overline{CASL}$ and DQ9-DQ16 by $\overline{CASH}$.
26. Each $\overline{CAS}x$ must meet minimum pulse width.
27. The last $\overline{CAS}x$ edge to transition HIGH.
28. Last falling $\overline{CAS}x$ edge to first rising $\overline{CAS}x$ edge.
29. Last rising $\overline{CAS}x$ edge to first falling $\overline{CAS}x$ edge.
30. Last rising $\overline{CAS}x$ edge to next cycle's last rising $\overline{CAS}x$ edge.
31. Last $\overline{CAS}x$ to go LOW.
32. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.

READ CYCLE



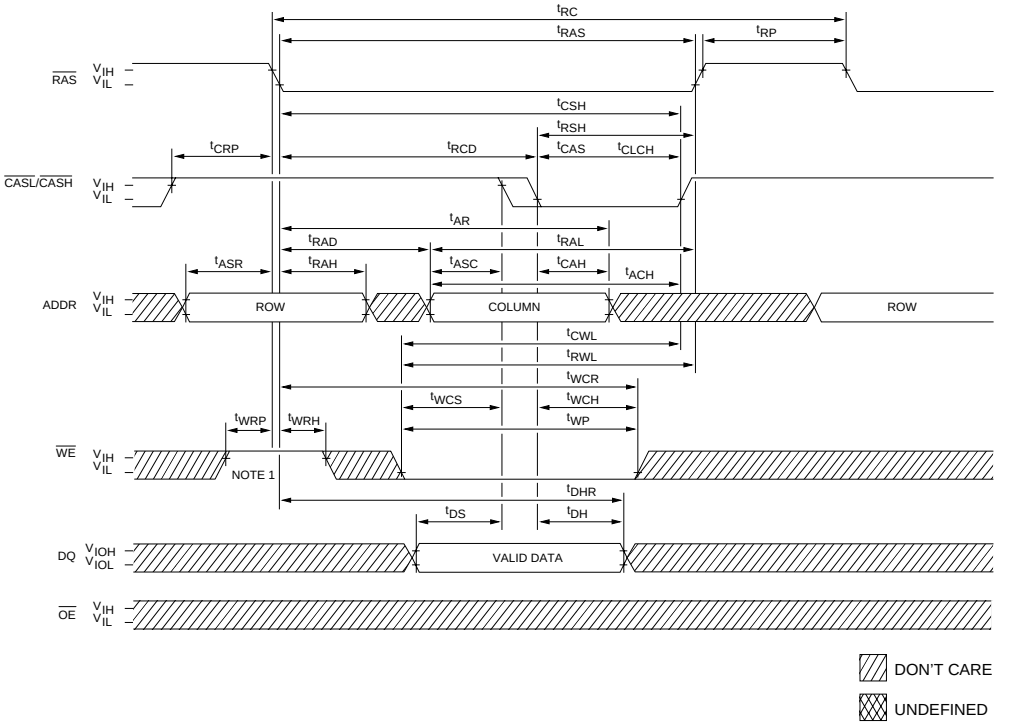
NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.
2. ^{t}OFF is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}AA		30		35		40	ns
^{t}ACH	15		15		20		ns
^{t}AR	45		50		60		ns
^{t}ASC	0		0		0		ns
^{t}ASR	0		0		0		ns
^{t}CAC		15		20		20	ns
^{t}CAH	10		12		15		ns
^{t}CAS	12	10,000	13	10,000	20	10,000	ns
^{t}CLCH	10		10		10		ns
^{t}CLZ	0		0		0		ns
^{t}CRP	5		5		5		ns
^{t}CSH	50		55		60		ns
^{t}OD	0	15	0	15	0	20	ns
^{t}OE		15		20		20	ns
^{t}OFF	0	15	0	15	0	20	ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}RAC		60		70		80	ns
^{t}RAD	12	30	12	35	15	40	ns
^{t}RAH	10		10		10		ns
^{t}RAL	30		35		40		ns
^{t}RAS	60	10,000	70	10,000	80	10,000	ns
^{t}RC	110		130		150		ns
^{t}RCD	14	45	14	50	20	60	ns
^{t}RCH	0		0		0		ns
^{t}RCS	0		0		0		ns
^{t}RP	40		50		60		ns
^{t}RRH	0		0		0		ns
^{t}RSH	13		15		15		ns
^{t}WRH	10		10		10		ns
^{t}WRP	10		10		10		ns

EARLY WRITE CYCLE



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

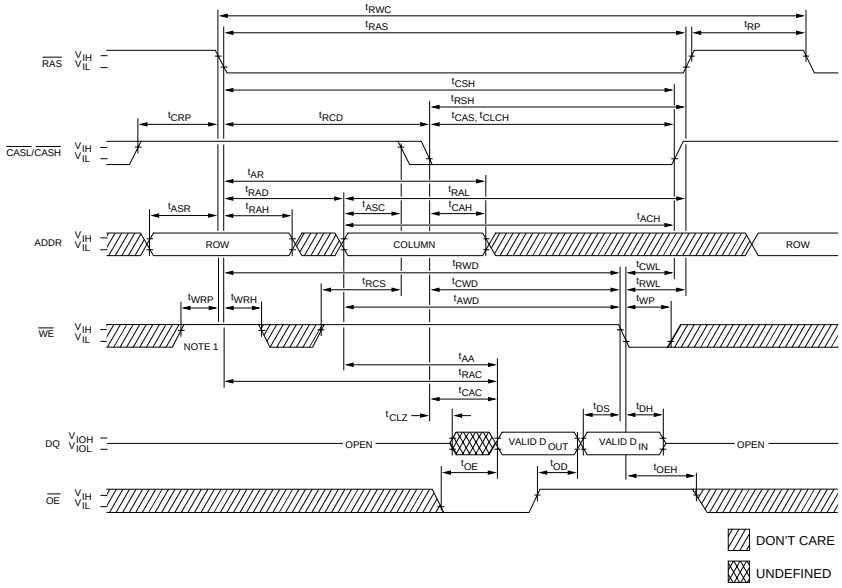
TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}ACH	15		15		20		ns
^{t}AR	45		50		60		ns
^{t}ASC	0		0		0		ns
^{t}ASR	0		0		0		ns
^{t}CAH	10		12		15		ns
^{t}CAS	12	10,000	13	10,000	20	10,000	ns
^{t}CLCH	10		10		10		ns
^{t}CRP	5		5		5		ns
^{t}CSH	50		55		60		ns
^{t}CWL	15		15		20		ns
^{t}DH	10		12		15		ns
^{t}DHR	45		55		55		ns
^{t}DS	0		0		0		ns
^{t}RAD	12	30	12	35	15	40	ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}RAH	10		10		10		ns
^{t}RAL	30		35		40		ns
^{t}RAS	60	10,000	70	10,000	80	10,000	ns
^{t}RC	110		130		150		ns
^{t}RCD	14	45	14	50	20	60	ns
^{t}RP	40		50		60		ns
^{t}RSH	13		15		0		ns
^{t}RWL	15		15		20		ns
^{t}WCH	10		12		15		ns
^{t}WCR	45		55		60		ns
^{t}WCS	0		0		0		ns
^{t}WP	10		12		15		ns
^{t}WRH	10		10		10		ns
^{t}WRP	10		10		10		ns

READ WRITE CYCLE

(LATE WRITE and READ-MODIFY-WRITE cycles)



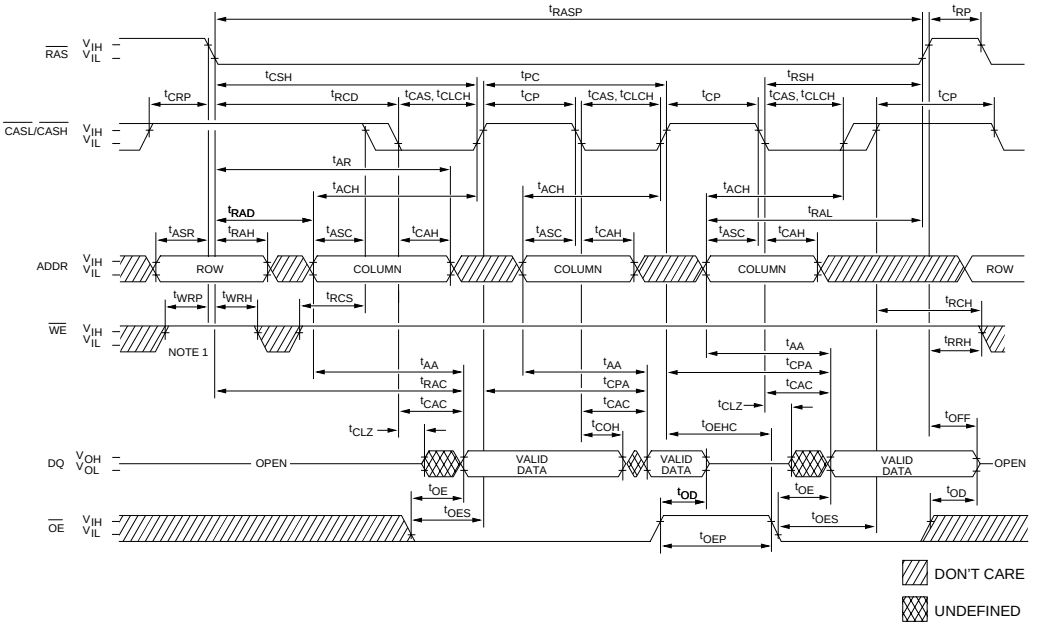
NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}AA		30		35		40	ns
^{t}ACH	15		15		20		ns
^{t}AR	45		50		60		ns
^{t}ASC	0		0		0		ns
^{t}ASR	0		0		0		ns
^{t}AWD	55		60		65		ns
^{t}CAC		15		20		20	ns
^{t}CAH	10		12		15		ns
^{t}CAS	12	10,000	13	10,000	20	10,000	ns
^{t}CLCH	10		10		10		ns
^{t}CLZ	0		0		0		ns
^{t}CRP	5		5		5		ns
^{t}CSH	50		55		60		ns
^{t}CWD	35		40		45		ns
^{t}CWL	15		15		20		ns
^{t}DH	10		12		15		ns
^{t}DS	0		0		0		ns
^{t}OD	0	15	0	15	0	20	ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}OE		15		20		20	ns
^{t}OEH	12		12		15		ns
^{t}RAC		60		70		80	ns
^{t}RAD	12	30	12	35	15	40	ns
^{t}RAH	10		10		10		ns
^{t}RAL	30		35		40		ns
^{t}RAS	60	10,000	70	10,000	80	10,000	ns
^{t}RCD	14	45	14	50	20	60	ns
^{t}RCS	0		0		0		ns
^{t}RP	40		50		60		ns
^{t}RSH	13		15		15		ns
^{t}RWC	150		180		200		ns
^{t}RWD	80		90		105		ns
^{t}RWL	15		15		20		ns
^{t}WP	10		12		15		ns
^{t}WRH	10		10		10		ns
^{t}WRP	10		10		10		ns

EDO-PAGE-MODE READ CYCLE



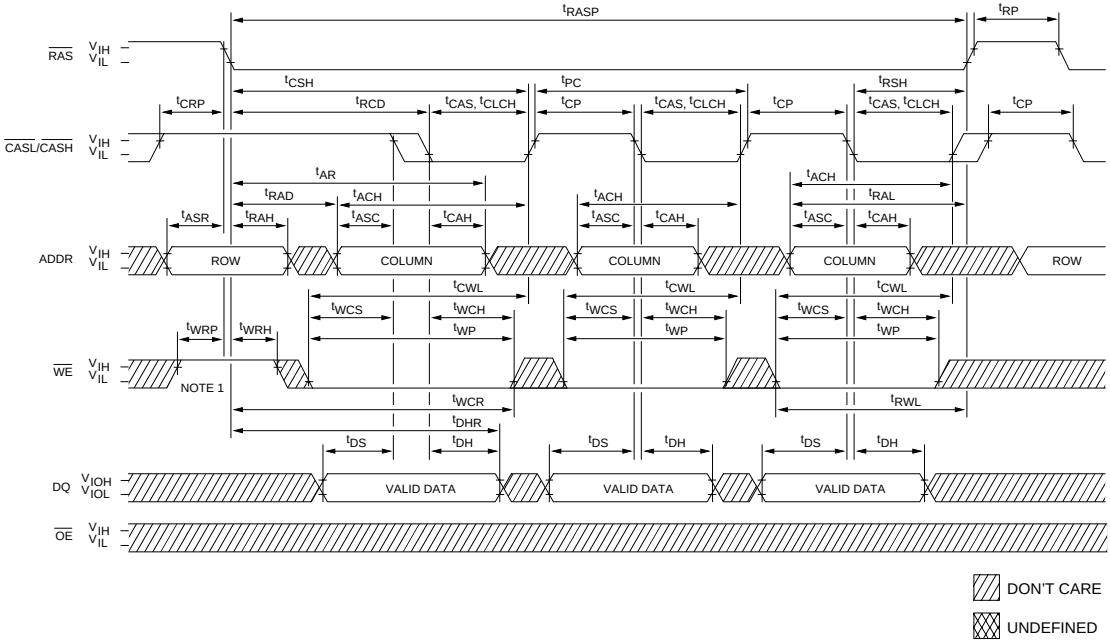
NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tAA		30		35		40	ns
tACH	15		15		20		ns
tAR	45		50		60		ns
tASC	0		0		0		ns
tASR	0		0		0		ns
tCAC		15		20		20	ns
tCAH	10		12		15		ns
tCAS	12	10,000	13	10,000	20	10,000	ns
tCLCH	10		10		10		ns
tCLZ	0		0		0		ns
tCOH	3		3		5		ns
tCP	10		10		10		ns
tCPA		35		40		40	ns
tCRP	5		5		5		ns
tCSH	50		55		60		ns
tOD	0	15	0	15	0	20	ns
tOE		15		20		20	ns
tOEHC	10		10		10		ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tOEP	10		10		10		ns
tOES	5		5		5		ns
tOFF	3	15	3	15	0	20	ns
tPC	30		35		40		ns
tRAC		60		70		80	ns
tRAD	12	30	12	35	15	40	ns
tRAH	10		10		10		ns
tRAL	30		35		40		ns
tRASP	60	100,000	70	100,000	80	100,000	ns
tRCD	14	45	14	50	20	60	ns
tRCH	0		0		0		ns
tRCS	0		0		0		ns
tRP	40		50		60		ns
tRRH	0		0		0		ns
tRSH	13		15		15		ns
tWRH	10		10		10		ns
tWRP	10		10		10		ns

EDO-PAGE-MODE EARLY-WRITE CYCLE



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

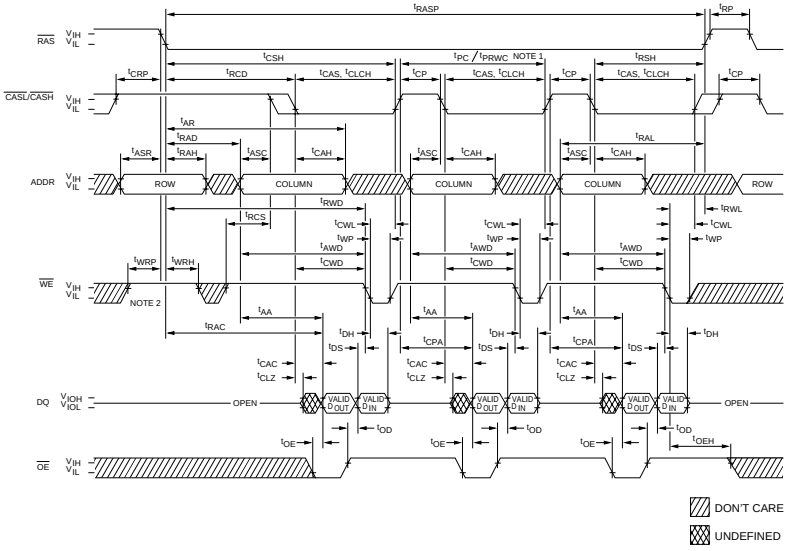
TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}ACH	15		15		20		ns
^{t}AR	45		50		60		ns
^{t}ASC	0		0		0		ns
^{t}ASR	0		0		0		ns
^{t}CAH	10		12		15		ns
^{t}CAS	12	10,000	13	10,000	20	10,000	ns
^{t}CLCH	10		10		10		ns
^{t}CP	10		10		10		ns
^{t}CRP	5		5		5		ns
^{t}CSH	50		55		60		ns
^{t}CWL	15		15		20		ns
^{t}DH	10		12		15		ns
^{t}DHR	45		55		55		ns
^{t}DS	0		0		0		ns
^{t}PC	25		30		40		ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}RAD	12	30	12	35	15	40	ns
^{t}RAH	10		10		10		ns
^{t}RAL	30		35		40		ns
^{t}RASP	60	125,000	70	125,000	80	100,000	ns
^{t}RCD	14	45	14	50	20	60	ns
^{t}RP	40		50		60		ns
^{t}RSH	13		15		15		ns
^{t}RWL	15		15		20		ns
^{t}WCH	10		12		15		ns
^{t}WCR	45		55		60		ns
^{t}WCS	0		0		0		ns
^{t}WP	10		12		15		ns
^{t}WRH	10		10		10		ns
^{t}WRP	10		10		10		ns

EDO-PAGE-MODE READ-WRITE CYCLE

(LATE WRITE and READ-MODIFY-WRITE cycles)



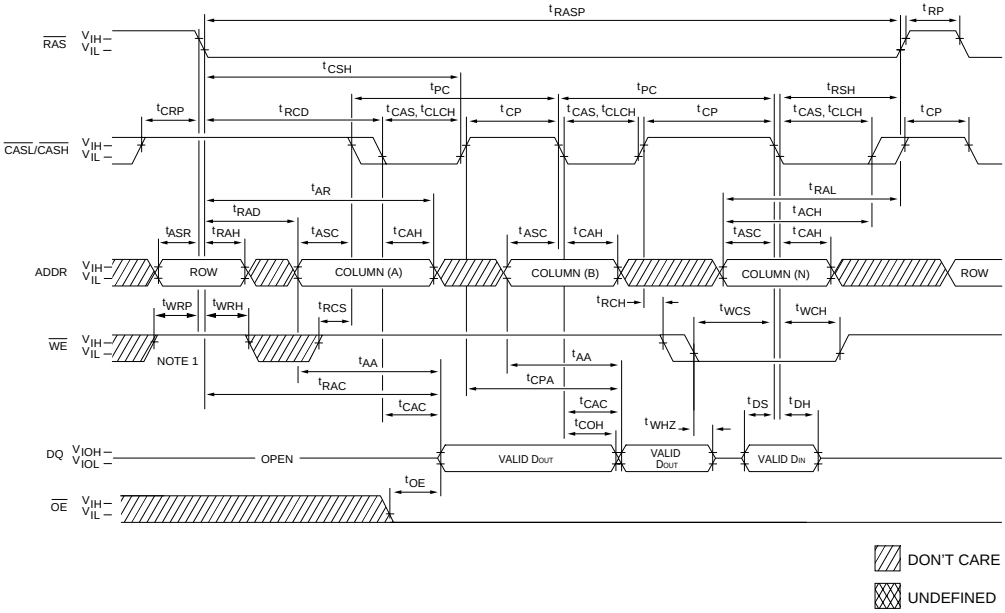
NOTE: 1. tPC is for LATE WRITE cycles only.
2. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tAA		30		35		40	ns
tAR	45		50		60		ns
tASC	0		0		0		ns
tASR	0		0		0		ns
tAWD	55		60		65		ns
tCAC		15		20		20	ns
tCAH	10		12		15		ns
tCAS	12	10,000	13	10,000	20	10,000	ns
tCLCH	10		10		10		ns
tCLZ	0		0		0		ns
tCP	10		10		10		ns
tCPA		35		40		40	ns
tCRP	5		5		5		ns
tCSH	50		55		60		ns
tCWD	35		40		45		ns
tCWL	15		15		20		ns
tDH	10		12		15		ns
tDS	0		0		0		ns
tOD	0	15	0	15	0	20	ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tOE		15		20		20	ns
tOEH	12		12		15		ns
tPC	25		30		40		ns
tPRWC	75		85		90		ns
tRAC		60		70		80	ns
tRAD	12	30	12	35	15	40	ns
tRAH	10		10		10		ns
tRAL	30		35		40		ns
tRASP	60	125,000	70	125,000	80	100,000	ns
tRCD	14	45	14	50	20	60	ns
tRCS	0		0		0		ns
tRP	40		50		60		ns
tRSH	13		15		15		ns
tRWD	80		90		105		ns
tRWL	15		15		20		ns
tWP	10		12		15		ns
tWRH	10		10		10		ns
tWRP	10		10		10		ns

EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



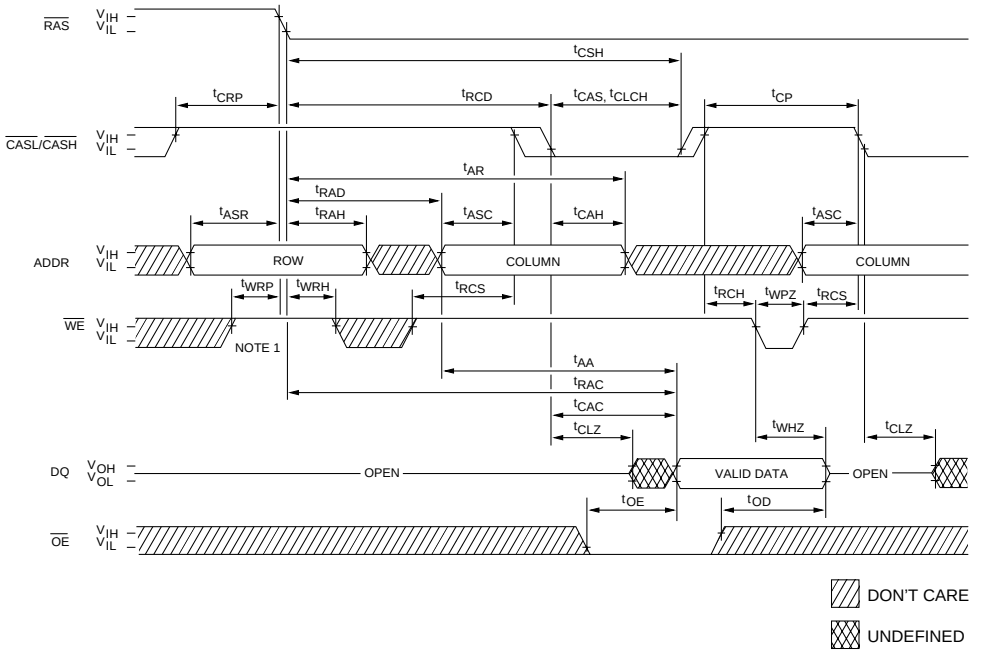
NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}AA		30		35		40	ns
^{t}ACH	15		15		20		ns
^{t}AR	45		50		60		ns
^{t}ASC	0		0		0		ns
^{t}ASR	0		0		0		ns
^{t}CAC		15		20		20	ns
^{t}CAH	10		12		15		ns
^{t}CAS	12	10,000	13	10,000	20	10,000	ns
^{t}CLCH	10		10		10		ns
^{t}COH	3		3		5		ns
^{t}CP	10		10		10		ns
^{t}CPA		35		40		40	ns
^{t}CRP	5		5		5		ns
^{t}CSH	50		55		60		ns
^{t}DH	10		12		15		ns
^{t}DS	0		0		0		ns
^{t}OE		15		20		20	ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}PC	25		30		40		ns
^{t}RAC		60		70		80	ns
^{t}RAD	12	30	12	35	15	40	ns
^{t}RAH	10		10		10		ns
^{t}RAL	30		35		40		ns
^{t}RASP	60	125,000	70	125,000	80	100,000	ns
^{t}RCD	14	45	14	50	20	60	ns
^{t}RCH	0		0		0		ns
^{t}RCS	0		0		0		ns
^{t}RP	40		50		60		ns
^{t}RSH	13		15		15		ns
^{t}WCH	10		12		15		ns
^{t}WCS	0		0		0		ns
^{t}WHZ	0	13	0	15	0	20	ns
^{t}WRH	10		10		10		ns
^{t}WRP	10		10		10		ns

READ CYCLE
(with $\overline{WE}$-controlled disable)



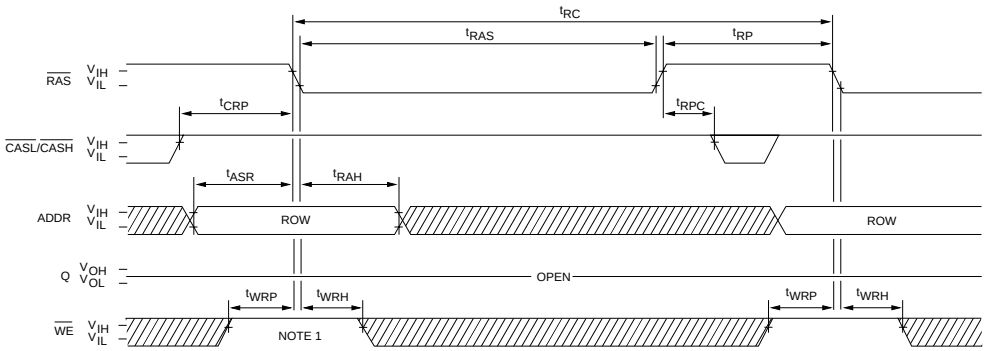
NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

TIMING PARAMETERS

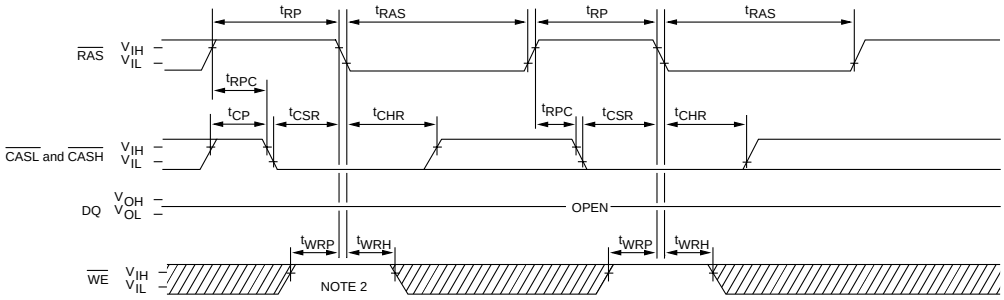
	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}AA		30		35		40	ns
^{t}AR	45		50		60		ns
^{t}ASC	0		0		0		ns
^{t}ASR	0		0		0		ns
^{t}CAC		15		20		20	ns
^{t}CAH	10		12		15		ns
^{t}CAS	12	10,000	13	10,000	20	10,000	ns
^{t}CLCH	10		10		10		ns
^{t}CLZ	0		0		0		ns
^{t}CP	10		10		10		ns
^{t}CRP	5		5		5		ns
^{t}CSH	50		55		60		ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}OD	0	15	0	15	0	15	ns
^{t}OE		15		20		20	ns
^{t}RAC		60		70		80	ns
^{t}RAD	12	30	12	35	15	40	ns
^{t}RAH	10		10		10		ns
^{t}RCD	14	45	14	50	20	60	ns
^{t}RCH	0		0		0		ns
^{t}RCS	0		0		0		ns
^{t}WHZ	0	13	0	15	0	20	ns
^{t}WPZ	10		12		15		ns
^{t}WRH	10		10		10		ns
^{t}WRP	10		10		10		ns

RAS-ONLY REFRESH CYCLE



CBR REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



NOTE:
1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.
2. ^{t}WRP and ^{t}WRH are for system design reference only. The $\overline{WE}$ signal is actually a "don't care" at $\overline{RAS}$ time during a CBR REFRESH. However, $\overline{WE}$ should be held HIGH at $\overline{RAS}$ time during a CBR REFRESH to ensure compatibility with other DRAMs that require $\overline{WE}$ HIGH at $\overline{RAS}$ time during a CBR REFRESH.

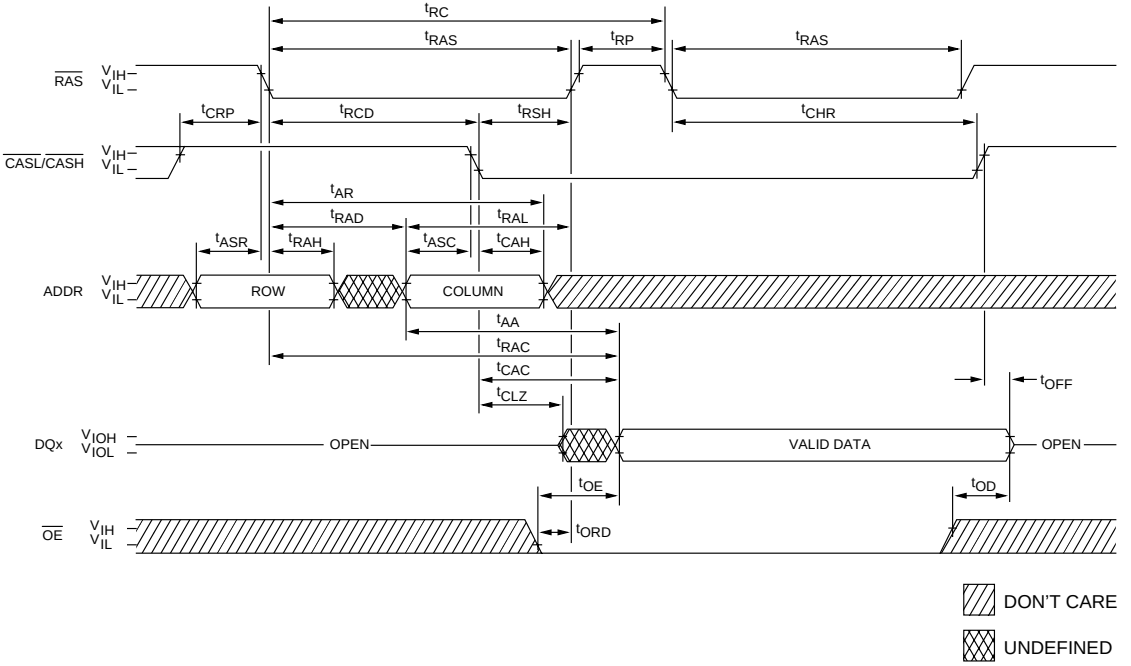
TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}ASR	0		0		0		ns
^{t}CHR	10		12		15		ns
^{t}CP	10		10		10		ns
^{t}CRP	5		5		5		ns
^{t}CSR	5		5		10		ns
^{t}RAH	10		10		10		ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}RAS	60	10,000	70	10,000	80	10,000	ns
^{t}RC	105		125		150		ns
^{t}RP	40		50		60		ns
^{t}RPC	5		5		5		ns
^{t}WRH	10		10		10		ns
^{t}WRP	10		10		10		ns

HIDDEN REFRESH CYCLE [32]

($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tAA		30		35		40	ns
tAR	45		50		60		ns
tASC	0		0		0		ns
tASR	0		0		0		ns
tCAC		15		20		20	ns
tCAH	10		12		15		ns
tCHR	10		12		15		ns
tCLZ	0		0		0		ns
tCRP	5		5		5		ns
tOD	0	15	0	15	0	20	ns
tOE		15		20		20	ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tOFF	3	15	3	15	3	15	ns
tORD	0		0		0		ns
tRAC		60		70		80	ns
tRAD	12	30	12	35	15	40	ns
tRAH	10		10		10		ns
tRAL	30		35		40		ns
tRAS	60	10,000	70	10,000	80	10,000	ns
tRC	105		125		145		ns
tRCD	14	45	14	50	20	60	ns
tRP	40		50		60		ns
tRSH	13		15		15		ns

ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (per Method 5005, Table I)
INTERIM ELECTRICAL (PRE-BURN-IN) TEST PARAMETERS (Method 5004)	2, 8A, 10
FINAL ELECTRICAL TEST PARAMETERS (Method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
GROUP A TEST REQUIREMENTS (Method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
GROUP C AND D END-POINT ELECTRICAL PARAMETERS (Method 5005)	1, 2, 3, 7, 8, 9, 10, 11

* PDA applies to subgroups 1 and 7.

** Subgroup 4 shall be measured only for initial qualification and after process or design changes, which may affect input or output capacitance.