μPD9624L/25L
CMOS PCM
CODEC-Filter Combination

Description

The μPD9624L and μPD9625L are single-chip pulse-code modulation (PCM) CODEC LSIs with transmit/receive filters. The CODEC LSIs include phase-locked loop (PLL) circuits for the transmit and receive channels that can generate a clock for its internal circuits by the frame synchronization clock. The LSIs have independent gain setting circuits that allow ease of setting the gains using digital signal input for the transmit and receive channels. These LSIs with a broad dynamic range, can be widely used for communications equipment and for digital processing of various voice frequency band signals.

The μPD9624L is μ-law compatible and the μPD9625L is A-law compatible. The μPD9624L and μPD9625L have roughly the same transmission characteristics as the μPD9604A and μPD9605A, respectively.

Features

- Single-chip CMOS monolithic LSI
- Complete single-chip CODEC LSIs, with the following internal circuits:
  - Transmit channel gain setting circuit
  - Transmit channel RC active lowpass filter (LPF) and switched-capacitor highpass filter (HPF)/LPF
  - μ-law/A-law compatible coder and decoder
  - Auto-zero circuit
  - Receive channel switched-capacitor LPF
  - Receive channel unbalanced output power amplifier and gain setting circuit
  - Precision reference voltage circuit
  - PLL circuits to generate transmit and receive internal clocks
  - Serial I/O interface circuit
- μ-law compatible (μPD9624L)
- A-law compatible (μPD9625L)
- Synchronous or asynchronous operation
- Data rate: 64 kb/s to 2.048 Mb/s
- Internal unbalanced output power amplifier, which can drive a 600 Ω resistance directly, serves as the receive output amplifier
- Low power consumption:
  - 50 mW typical (normal operation)
  - 5 mW typical (power-down/standby mode)
- Internal digital gain setting function
- Internal analog loopback test function

Ordering Information

Part Number	Companding	Package
μPD9624L	μ-law	18-pin PLCC
μPD9625L	A-law	

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Block Diagram