NEC Electronics Inc.

μPD4264400, 4265400 16,777,216 x 4-Bit Dynamic CMOS RAM

Preliminary

September 1993

Description

The μ PD4264400 and μ PD4265400 are 64M-bit dynamic RAMs organized as 16,777,216 words by 4 bits. They are designed to operate from a single +3.3-volt power supply and have an optional fast-page mode.

Advanced polycide technology minimizes silicon areas and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative voltage substrate bias—automatically and transparently.

The three-state outputs are controlled by CAS independent of RAS. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining CAS low. Data outputs return to high impedance when CAS goes high. Fast-page read and write cycles can be executed by cycling CAS.

Refreshing may be accomplished by a CAS before RAS cycle that internally generates the refresh address. Refreshing can also be accomplished by RAS-only refresh cycles or by normal read or write cycles during a 64-ms refresh period.

Two versions of the 16M x 4-bit DRAM are available. The μ PD4264400 uses 8192 combinations of A₀ - A₁₂ for

 $\overline{\text{RAS}}$ -only refreshing and 4096 address combinations of A₀ - A₁₁ to perform $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ and hidden refreshing of the memory during a 64-ms period. The $\mu\text{PD}4265400$ uses 4096 address combinations of A₀ - A₁₁ during a 64-ms period for all refresh modes.

The μ PD4264400 and μ PD4265400 are available in a 34-pin plastic SOJ and 34-pin plastic TSOP.

Features

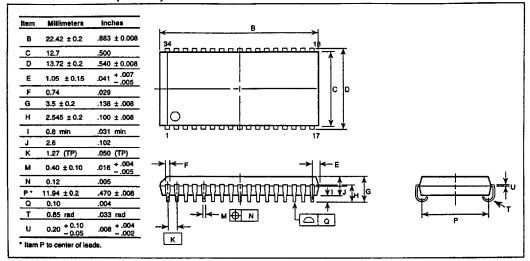
- □ 16,777,216 x 4-bit organization
- □ Single +3.3-volt power supply
- □ Fast-page option
- □ Low power dissipation: 1.80 mW (max) standby
- □ CAS before RAS refresh cycles
- Multiplexed address inputs
- On-chip substrate bias generator
- □ TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- □ Low input capacitance
- 34-pin plastic SOJ and TSOP packaging

Ordering Information

Part Number	Access Time (max)	R/W Cycle (max)	Fast-Page Cycle (max)	Active Power (max)	Package	
μPD4264400LG-A50	50 ns	90 ns	35 ns	360 mW	34-pin plastic SOJ	
-A60	60 ns	110 ns	40 ns	324 mW		
-A70	70 ns	130 ns	45 n s	288 mW		
-A80	80 ns	150 ns	50 ns	252 mW		
μPD4264400G7-A50	50 ns	90 ns	35 ns	360 mW	34-pin plastic TSOP	
-A60	60 ns	110 ns	40 ns	324 mW	•	
-A70	70 ns	130 ns	45 ns	288 mW		
-A80	80 ns	150 ns	50 ns	252 mW		
μPD4265400LG-A50	50 ns	90 ns	35 ns	468 mW	34-pin plastic SOJ	
-A60	60 ns	110 ns	40 ns	396 mW		
-A70	70 ns	130 ns	45 ns	360 mW		
-A80	80 ns	150 ns	50 ns	324 mW		
μPD4265400G7-A50	50 ns	90 ns	35 ns	468 mW	34-pin plastic TSOP	
-A60	60 ns	110 ns	40 ns	396 mW		
-A70	70 ns	130 ns	45 ns	360 mW	_	
-A80	80 ns	150 ns	50 ns	324 mW	-	

μPD4264400, 4265400

34-Pin Plastic SOJ (500-mil)



SOJ or TSOP 34 □ V_{SS} Vcc.□ 33 D VO8 *1*0₁ ☐ 32 D VO7 VO2 □ 3 31 🗗 1/06 VO3 □ 30 | 1/0₅ 29 | V_{SS} 1/O₄ 🗆 NC [28 🗖 CAS vcc □ 27 DE **WE** □ 8 RAS [26 🗖 NC 25 A12 NC [10 $A_0 \Box$ 24 A11 A1 🗖 23 A 10 22 A9 21 A8 13 A2 🗆 A3 🗆 A4 🗖 15 20 A7 19 🗖 A6 A₅ 🗖 16 V_{CC} 🗖 17 18 1 VSS

A₀ to A₁₁(A₁₂) Address inputs VO₁ to VO₈ Data inputs/outputs RAS Row address strobe CAS Column address strobe WE Write enable ŌĒ Output enable Supply voltage VCC Ground **VSS** NC No connection

34-Pin Plastic TSOP (500 mil)

m	Millimeters	Inches	34 6 6 6 6 6 6 6 7 7 8 6 6 6 7 8 7 8 9 8 9 8 9 8 9 8 9 8 9 8 9 8 9 8	Enlarged detail of lead and
A	22.66 max	.893 max	i	
В	120 max	.048 max	1	FÎGÎ I \ <mark>}</mark> ⊟
С	1.27 (TP)	.050 (TP)		<u> </u>
D	0.40 ± 0.10	.016 ± .004		† †
E	0.05 ± 0.05	.002 ± .002		E 5°±5°
F.	1.10 max	.044 max	1 1	
G	0.97	.038		
н	14.3 ± 0.2	.563 ± 0.008	 BESSESSESSESS	
1	12.7 ± 0.1	.500 ± 0.004	1 17	
J	0.8 ± 0.2	.031 ± .008	 	<u> </u>
ĸ	0.125 + 0.10 - 0.05	.005 + .004 002	^	J→
L	0.5 ± 0.1	.020 + .004 005		
M	0.21	.009		
N	0.10	.004		
N	0.10	.004		ι

NEC

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