NEC Electronics Inc.

μPD27HC65
8,192 x 8-Bit
CMOS UV EPROM

Description

The μPD27HC65 is an ultraviolet erasable and electricaly programmable read-only memory fabricated with double-polysilicon CMOS technology for high speed and low operating and standby power. The μPD27HC65 is organized as 8,192 words by 8 bits and has three-state outputs, fully TTL-compatible inputs and outputs, and a program voltage (V_{PP}) of 12.5 volts. The device is packaged in a 24-pin cerdip with quartz window.

Features

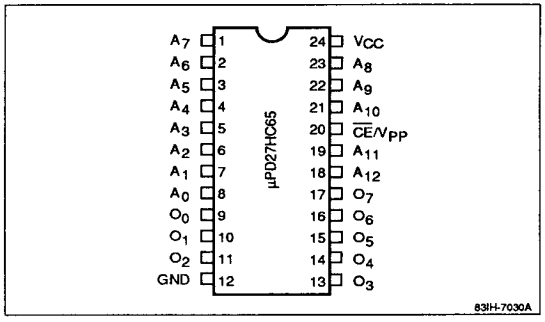
- 8,192-word x 8-bit organization
- Ultraviolet erasable and electrically programmable
- Ultra-high-speed access time
- Low power dissipation
  - 100 mA maximum (active)
  - 25 mA maximum (standby)
- TTL-compatible I/O for reading and programming
- Single +5-volt power supply
- Double polysilicon CMOS technology
- 24-pin cerdip packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD27HC65DX-25	25 ns	24-pin cerdip with quartz window
DX-35	35 ns	
DX-45	45 ns	

Pin Configuration

24-Pin Cerdip



Pin Identification

Symbol	Function
A_0 - A_{12}	Address inputs
O_0 - O_7	Data outputs
$\overline{CE}/V_{PP}$	Chip enable/program voltage
GND	Ground
V_{CC}	+5-volt power supply

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Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.6 to +7.0 V
Input voltage, V_{IN}	−0.6 to +7.0 V
Input voltage, A_9 and A_{10}	−0.6 to +13.5 V
Output voltage, V_{OUT}	−0.6 to +7.0 V
Storage temperature, T_{STG}	−65 to +125°C
Operating temperature, T_{OPR}	0 to 70°C
Program voltage, V_{PP}	−0.6 to +13.5 V

Exposure to Absolute Maximum Ratings for extended periods may affect device reallability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		5	10	pF
Output capacitance	C_{OUT}		10	15	pF
$\overline{CE}/V_{PP}$ input capacitance	C_P		10	20	pF

Truth Table

Cycle	$\overline{CE}/V_{PP}$	A_9	A_{10}	V_{CC}	Output
Read	V_{IL}	X	X	+5.0 V	D_{OUT}
Standby	V_{IH}	X	X	+5.0 V	High-Z
Byte program	+12.5 V	X	X	+6.0 V	D_{IN}
Program verify	V_{IL}	X	X	+6.0 V	D_{OUT}
Blank page set	V_{IH}	XX	V_{IHH}	+5.0 V	High-Z
Blank read (type 1)	V_{IL}	X	V_{IHH}	+5.0 V	D_{OUT}
Blank read (type 2)	V_{IL}	V_{IHH}	V_{IHH}	+5.0 V	D_{OUT}

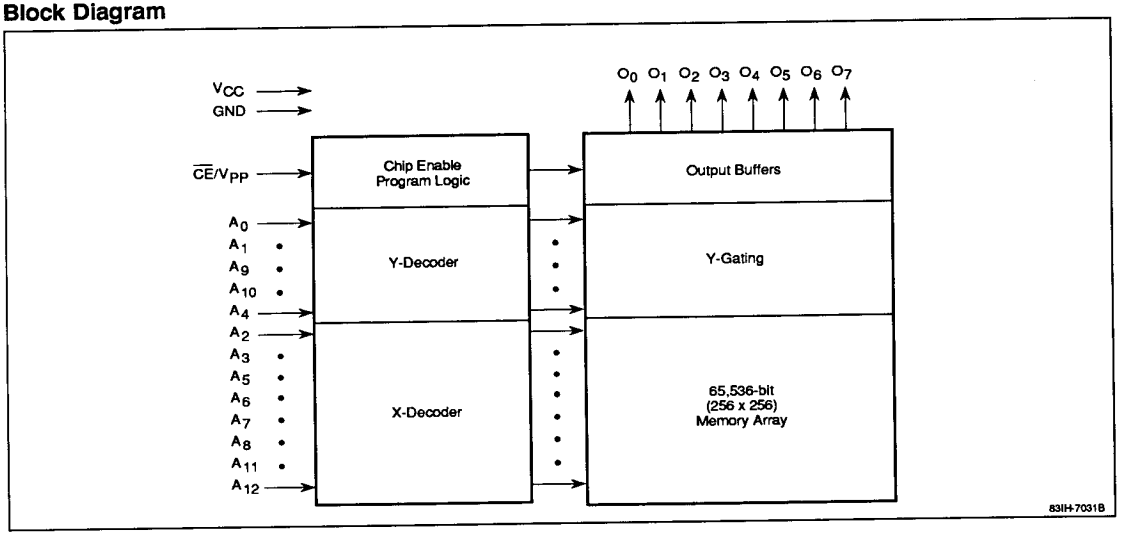
Notes:

(1) V_{IHH} = +12 V ±0.5.

(2) X can be either V_{IL} or V_{IH}.

(3) XX can be either V_{IL}, V_{IH}, or V_{IHH}.

Block Diagram



Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Read Operation or Standby					
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low (Note 1)	V_{IL}	−0.3		0.8	V
Operating temperature	T_A	0		70	°C
Programming Operation					
Supply voltage	V_{CC}	6.25	6.5	6.75	V
	$\overline{CE}/V_{PP}$	12.2	12.5	12.8	V
Input voltage, high	V_{IH}	2.4		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Operating temperature	T_A	20	25	30	V

Notes:

(1) V_{IL} = −1.5 V minimum for 10 ns maximum pulse width.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Read Operation or Standby T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%						
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4 mA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 6 mA
Output leakage current	I_{LO}	−10		10	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CE}/V_{PP}$ = V_{IH}
Input leakage current	I_{LI}	−10		10	μA	V_{IN} = 0 V to V_{CC}
V_{CC} current (active)	I_{CCA}			100	mA	$\overline{CE}/V_{PP}$ = V_{IL}; I_{OUT} = 0 mA (minimum cycle time)
V_{CC} current (standby)	I_{CCS1}			50	mA	$\overline{CE}/V_{PP}$ = V_{IH} (min); V_{IN} = V_{IH} or V_{IL}
	I_{CCS2}			25	mA	$\overline{CE}/V_{PP}$ ≥ V_{CC} − 0.2 V; V_{IN} ≥ V_{CC} − 0.2 V ≤ 0.2 V
Programming Operation T_A = 25 ±5°C; V_{CC} = +6.5 V ±0.25; $\overline{CE}/V_{PP}$ = +12.5 V ±0.3						
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4 mA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 6 mA
Input leakage current	I_{LI}	−10		10	μA	V_{IN} = 0 V to V_{CC}
V_{PP} current	I_{PP}			50	mA	
V_{CC} current	I_{CC}			100	mA	
Blank Read Operation T_A = 25 ±5°C; V_{CC} = +5.0 ±0.5 V						
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V	
	V_{IHH}	11.5	12	12.5	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4 mA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 6 mA
Input leakage current	I_{LI}	−10		10	μA	V_{IN} = 0 V to V_{CC}
V_{CC} current	I_{CC}			100	mA	

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AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	μPD27HC65-25 Min	μPD27HC65-25 Max	μPD27HC65-35 Min	μPD27HC65-35 Max	μPD27HC65-45 Min	μPD27HC65-45 Max	Unit	Test Conditions
Read Operation									
Address to output delay	t_{ACC}		25		35		45	ns	$\overline{CE}/V_{PP}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}		20		30		30	ns	
$\overline{OE}$ or $\overline{CE}$ high to output float	t_{DF}		20		30		30	ns	
Address to output hold	t_{OH}	0		0		0		ns	$\overline{CE}/V_{PP}$ = V_{IL}

AC Characteristics (cont)

T_A = 25 ±5°C; V_{CC} = +6.0 V ±0.25; $\overline{CE}/V_{PP}$ = +12.5 V ±0.3

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Programming Operation						
Address setup time	t_{AS}	2			μs	
Address hold time	t_{AH}	2			μs	
Data setup time	t_{DS}	2			μs	
Data hold time	t_{DH}	2			μs	
V_{CC} setup time	t_{VCS}	2			μs	
V_{PP} rise time	t_R	1			μs	10% to 90%
V_{PP} fall time	t_F	1			μs	90% to 10%
$\overline{CE}/V_{PP}$ setup time	t_{CES}	2			μs	
$\overline{CE}/V_{PP}$ to data delay	t_{CEP}			500	ns	
$\overline{CE}/V_{PP}$ to output float	t_{DFP}			500	ns	
Verify pulse width	t_{VP}	1			μs	
Program pulse width	t_{PW}	0.095	0.1	0.105	ms	
Overprogram pulse width	t_{OPW}	0.095		1.05	ms	
Blank Read Operation						
Page address setup time	t_{PAS}	0			μs	
Blank read setup time	t_{BRS}	1			μs	
Page programming pulse width	t_{PPW}	1			μs	
Page address hold time	t_{PAH}	1			μs	
Address setup time	t_{ASB}	0			μs	
Address to output delay	t_{ACCB}			500	ns	
Address hold time	t_{AHB}	1			μs	

Notes:

(1) Input pulse levels = 0 to 3 V; input and output timing reference levels = 1.5 V; input rise and fall times ≤ 5 ns. See figures 1 and 2 for output load.

Figure 1. Output Load

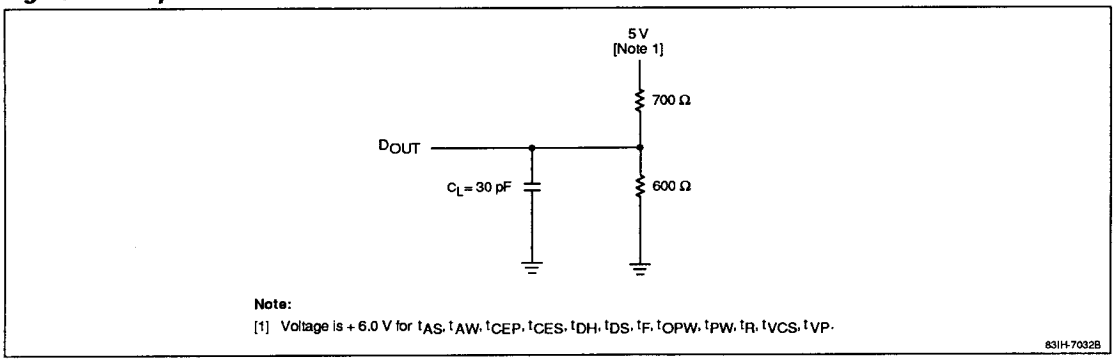
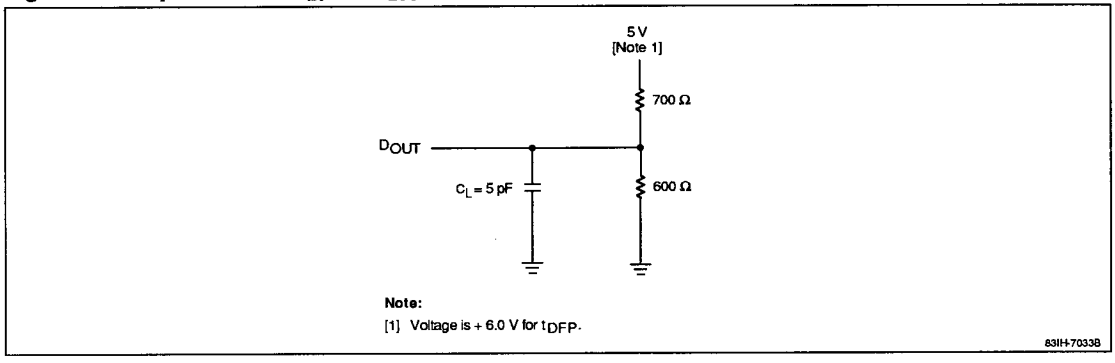


Figure 2. Output Load for t_{DF} and t_{DFP}



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Read Operation

The μPD27HC65 may be read when $\overline{CE}/V_{PP}$ is low by addressing a desired location. Data is output on O_1 through O_7 after the specified time for t_{ACC} has elapsed or after $\overline{CE}/V_{PP}$ goes low for a specified time of t_{CE}, whichever occurs later.

Blank Check Cycles

Because of the μPD27HC65's high speed, normal read cycles cannot detect an erased memory location and individual bits in a byte may be read as either high or low, causing an erased location to appear to contain valid data. The only certain method of reading an erased location is by means of blank check cycles.

Two types of cycles must be executed to assure that addresses have been completely erased. To initiate the first cycle, $\overline{CE}/V_{PP}$ must be low with A_{10} at V_{IHH} and A_9 either high or low, allowing all erased data bits to be read as high. Type 2 blank check cycles will read the erased data bits as low when both A_{10} and A_9 are at V_{IHH}. If both blank check cycles read the expected data, then the device has been erased.

The μPD27HC65 is divided into four pages of 2 Kbytes each. Because address bits A_9 and A_{10} are used for blank check selection and therefore cannot be used as address bits, the μPD27HC65 has a scheme to allow addressing of all 8 Kbytes. A page can be selected by toggling $\overline{CE}/V_{PP}$ high and then low during either a type 1 or type 2 blank check cycle to read the page address on A_0 and A_1. Subsequently, all addresses in the selected page are read from A_0 through A_8, A_{11} and A_{12} to determine whether or not they have been erased. Once a page is verified, $\overline{CE}/V_{PP}$ may again be toggled high and then low to read the next addressed page on A_0 and A_1 and then the addresses in the selected page. This process continues until all four pages have been checked.

To determine whether the μPD27HC65 has been successfully erased, both types of blank check cycles must be executed. If both pass, then the device has been erased.

PROGRAMMING

Begin programming by erasing all data; this sets all data bits to an indeterminate level, the condition in which the μPD27HC65 is originally shipped. To enter data, raise V_{CC} to +6.0 V, address the first byte, and apply valid data to the eight output pins. Apply a 0.1-ms program pulse of +12.5 V to $\overline{CE}/V_{PP}$, as shown in the programming portion of the timing waveforms. Set $\overline{CE}/V_{PP}$ low (V_{IL}) to verify the eight bits prior to making a program/no program decision. If the byte is programmed within 10 tries, apply an additional overprogram pulse of "x" ms (where "x" equals the number of tries multiplied by 0.1) and input the next address. If the μPD27HC65 is not programmed in 10 tries, reject it as a program failure.

Because the μPD27HC65 cannot distinguish an erased bit as either high or low during a normal read cycle, it is recommended that all locations be programmed to prevent reading of incorrect data by EPROM programmers or the system CPU.

Program Inhibit

Use the programming inhibit option to program multiple devices connected in parallel. All like inputs (except $\overline{CE}/V_{PP}$) may be common. Applying a +12.5 V program pulse to the $\overline{CE}/V_{PP}$ pin of an individual device will cause it to be programmed. Applying a high level (V_{IH}) to the $\overline{CE}/V_{PP}$ input of all the other devices prevents them from being programmed.

Program Verify

Address bits may be verified to determine whether or not data was correctly programmed. $\overline{CE}/V_{PP}$ of the device to be verified should be at V_{IL} and V_{CC} at +6.0 V.

Program Erasure

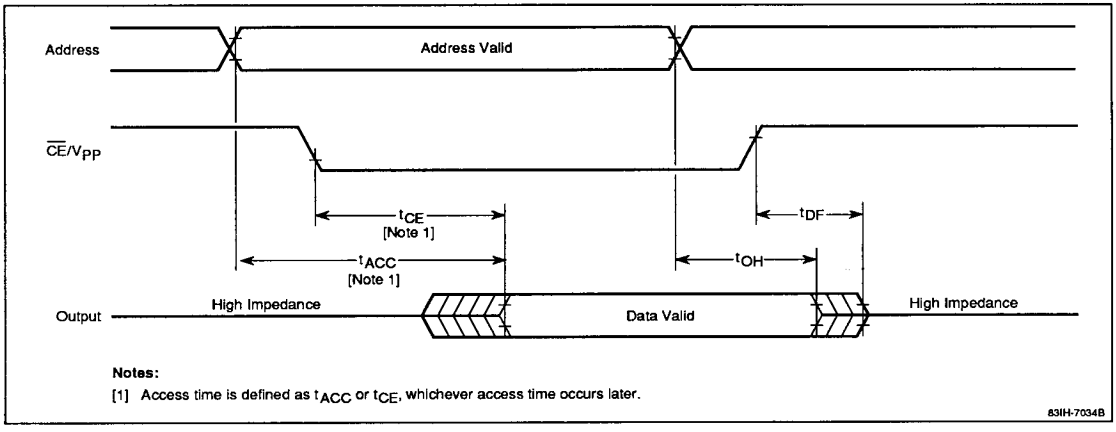
Erase data on the μPD27HC65 by exposing it to light with a wavelength shorter than 400 nm. Because exposure to direct sunlight or room-level fluorescent light could also erase the data, mask the window to prevent unintentional erasure by ultraviolet rays. Opaque labels are supplied with every device.

Data is typically erased by ultraviolet rays with a wavelength of 254 nm. A minimum integrated dose of 15 W-sec/cm^2 (ultraviolet lighting intensity multiplied by exposure time) is required to completely erase written data.

An ultraviolet lamp rated at 12,000 μW/cm^2 will complete erasure in approximately 20 minutes. Place the μPD27HC65 within 2.5 cm of the lamp tubes and remove any filter on the lamp.

Timing Waveforms

Read Cycle



Notes:

[1] Access time is defined as t_{ACC} or t_{CE}, whichever access time occurs later.

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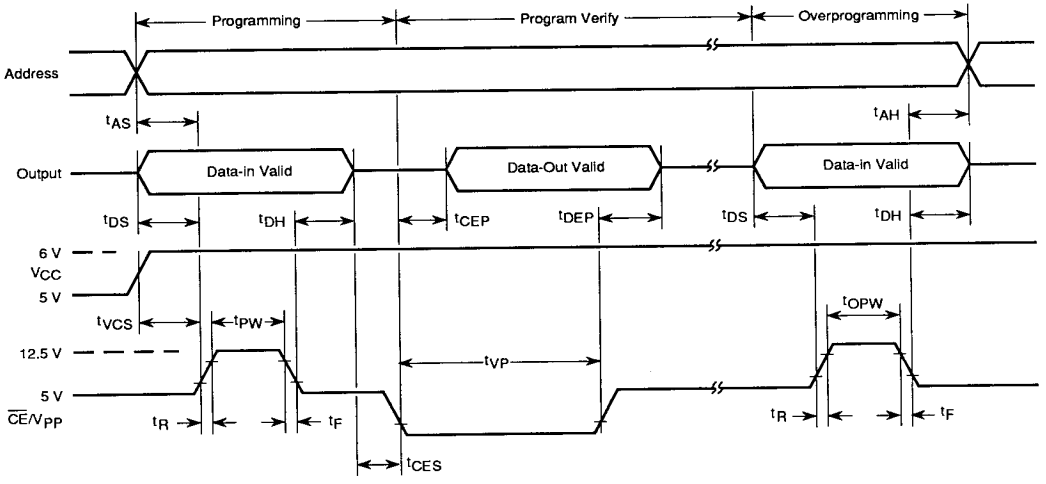
Timing Waveforms (cont)

Programming Cycle



Notes:

[1] V_{PP} must not be greater than + 13.5 V, including overshoot.

[2] Removing and reinserting the device while a voltage of 12.5 V is applied to V_{PP} may affect device reliability.

[3] The output lines are also used for data input when programming the device.

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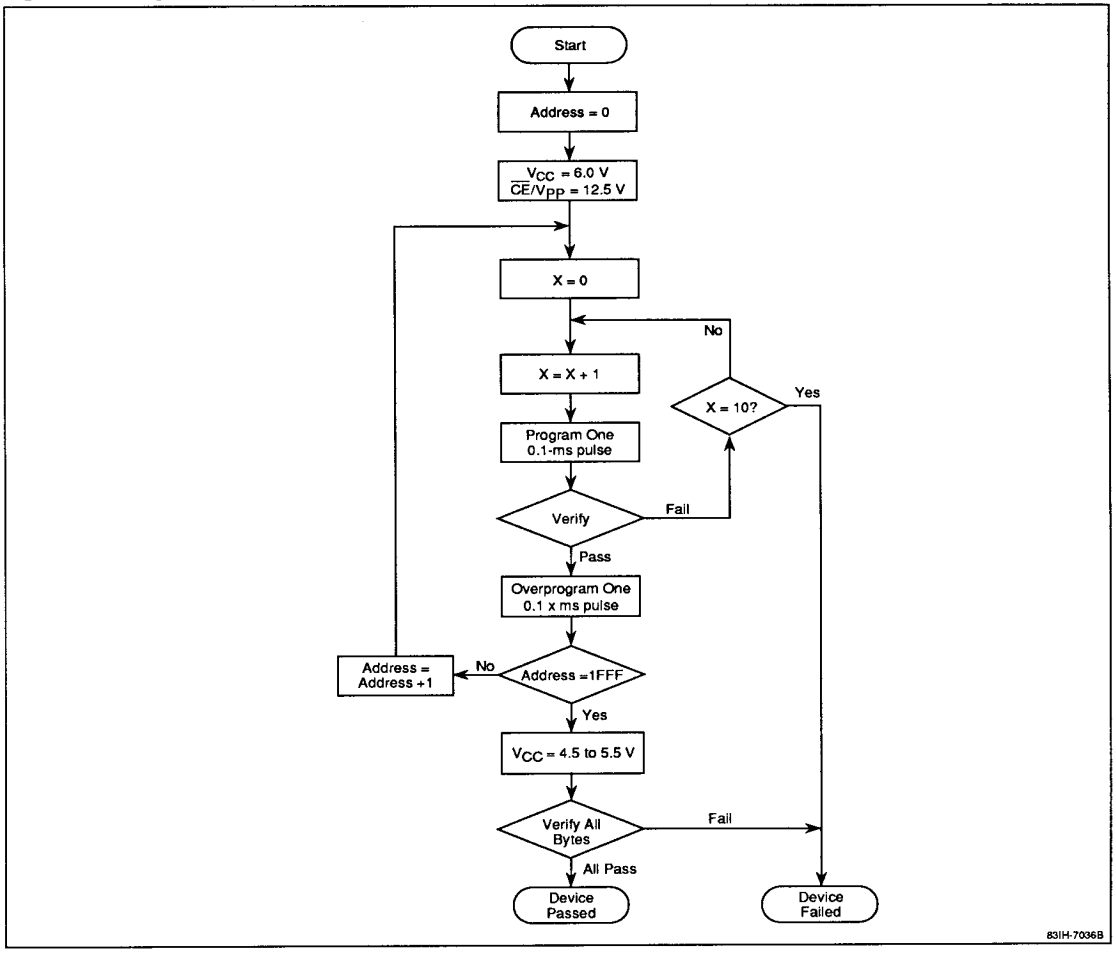
Figure 3. Programming Flowchart



Timing Waveforms (cont)

Blank Read Cycle

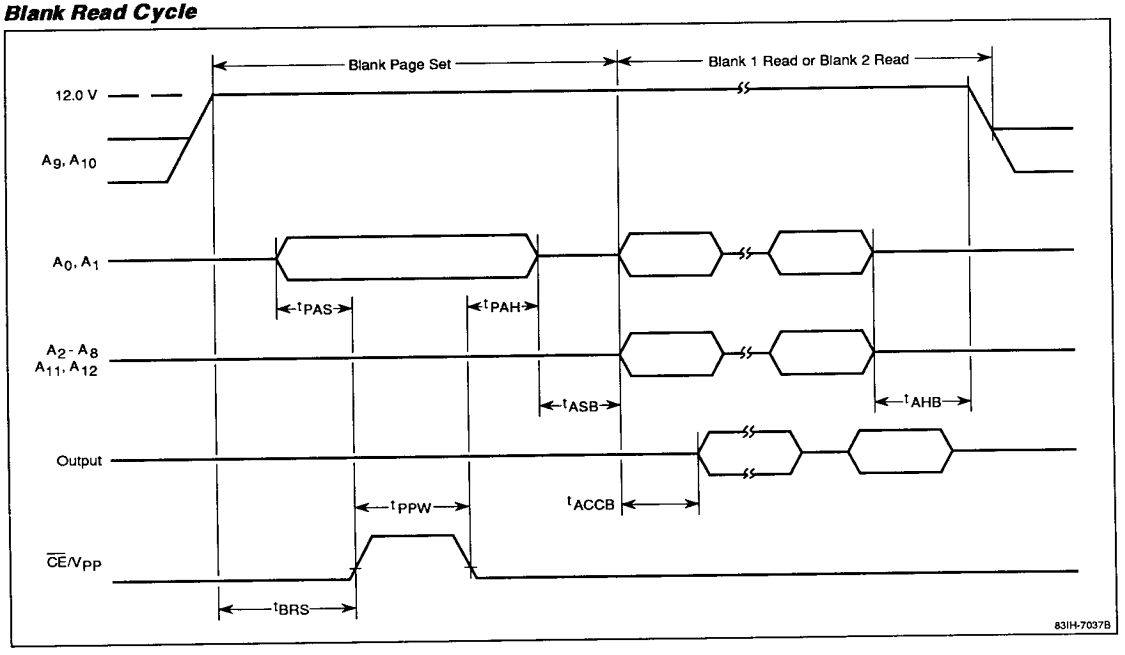
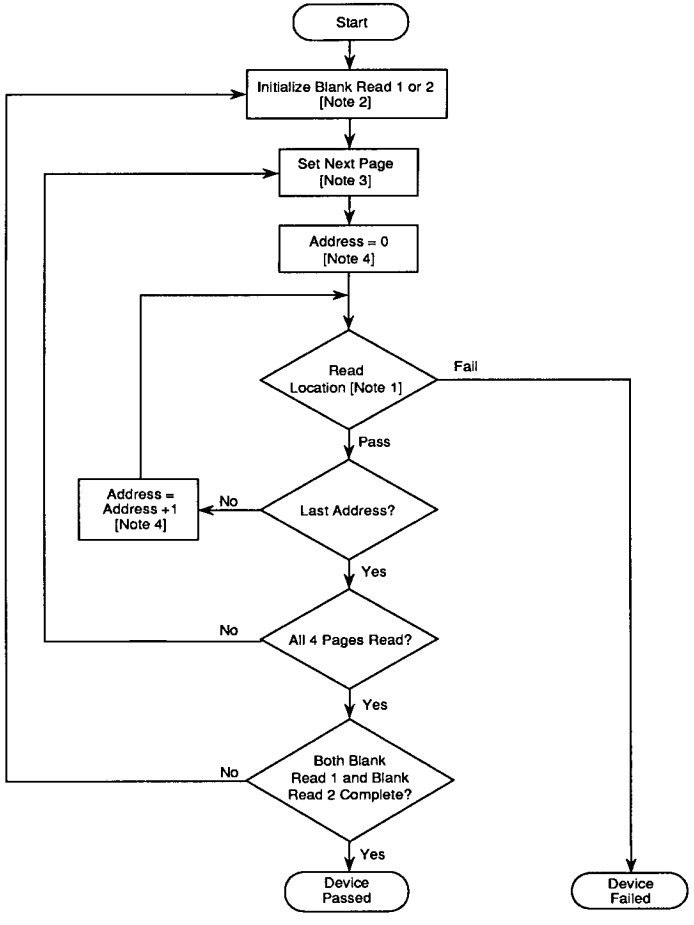


Figure 4. Blank Read Flowchart



Notes:

[1] Data must equal FF Hex for type 1 blank read cycles and 00 Hex for type 2 blank read cycles.

[2] For type 1 blank read cycles, $\overline{CE}/V_{PP} = V_{IL}$; $A_9 = V_{IL}$ or V_{IH}; $A_{10} = V_{IHH}$. For type 2 blank read cycles, $\overline{CE}/V_{PP} = V_{IL}$; $A_9 = A_{10} = V_{IHH}$.

[3] Use A_0 and A_1 for setting the page address when toggling $\overline{CE}/V_{PP}$.

[4] Use only addresses A_0 through A_8 and A_{11} and A_{12}.

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