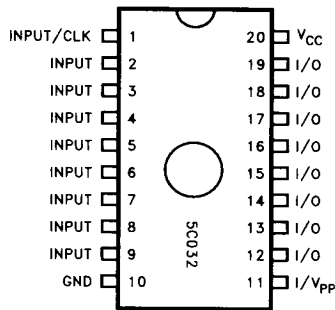# intel.

5C032
8-MACROCELL CMOS PLD

- **High-Density, Low-Power Replacement for SSI & MSI Devices and Bipolar PLDs**
- **Up to 18 Inputs (10 Dedicated & 8 I/O) and 8 Outputs**
- **Eight Macrocells with Programmable I/O Architecture**
- **t_{PD} = 30 ns (max), 43.5 MHz Pipelined, 28.5 MHz with Feedback**
- **Low Power Upgrade for All Commonly Used 20-pin PLDs**
- **CMOS EPROM Technology Based UV Erasable (CerDIP)**

- **Programmable "Security Bit" Allows Total Protection of Proprietary Designs**
- **I_{CC} (standby) 100 μA (max) I_{CC} (10 MHz) 25 mA (max)**
- **100% Generically Tested EPROM Logic Control Array**
- **20-pin 0.3" Ceramic and Plastic DIP Package**
  (See Packaging Spec., Order #240800)
  Package Type D and P
- **100% Compatible with EP320**

```
INPUT/CLK ⊏ 1        20 ⊐ Vcc
   INPUT ⊏ 2         19 ⊐ I/O
   INPUT ⊏ 3         18 ⊐ I/O
   INPUT ⊏ 4         17 ⊐ I/O
   INPUT ⊏ 5         16 ⊐ I/O
   INPUT ⊏ 6         15 ⊐ I/O
   INPUT ⊏ 7         14 ⊐ I/O
   INPUT ⊏ 8         13 ⊐ I/O
   INPUT ⊏ 9         12 ⊐ I/O
     GND ⊏ 10        11 ⊐ I/Vpp
                5C032
```
290155-1

Pin Configuration

INTRODUCTION

The Intel 5C032 is an 8-macrocell, 20-pin, general-purpose PLD (Programmable Logic Device).This device can be used to replace bipolar programmable logic arrays and LS TTL and 74HC (CMOS) SSI and MSI logic devices. The 5C032 can also be used as a direct, low-power replacement for almost all common 20-pin fuse-based programmable logic devices. With its flexible programmable I/O architecture, this device is a superset of common 20-pin PLDs.

The 5C032 PLD uses CMOS EPROM (floating gate) cells as logic control elements instead of fuses. The CMOS EPROM technology reduces power consumption of PLDs to less than 20% of a comparable bipolar device without sacrificing speed performance. In addition, the use of Intel's advanced CMOS II-E EPROM process technology enables greater logic densities to be achieved with superior speed and low-power performance over other comparable devices. Intel's 5C032 has the benefit of "zero" stand-by power not available on other programmable logic devices. EPROM technology allows these devices to be 100% factory tested by programming and erasing all the EPROM logic control elements.

The 5C032 with its superior speed and power performance and its plastic package is an ideal production vehicle for high-volume manufacturing. Most commonly used 20-pin bipolar PLDs can be easily replaced with this device allowing for tremendous power consumption savings without sacrificing speed of operation.

ARCHITECTURE DESCRIPTION

The architecture of the 5C032 is based on the "Sum of Products" PLA (Programmable Logic Array) structure with a programmable AND array feeding into a fixed OR array. This device can accommodate both combinational and sequential logic functions. A proprietary programmable I/O architecture provides individual selection of either combinational or registered output and feedback signals, all with selectable polarity.

The 5C032 contains 10 dedicated inputs as well as 8 input/output pins. These I/O pins can be individually configured to be inputs, outputs or bi-directional I/O pins. Each of these I/O pins is connected to a macrocell. The 5C032 contains 8 identical macrocells organized as shown in Figure 1.

Each macrocell (see Figure 2) consists of a PLA (programmable logic array) block and an I/O architecture block, which contains a "D" type register. The PLA block consists of eight 36-input AND gates (TRUE & COMPLEMENT of 10 dedicated inputs plus the 8 feedback inputs from the eight macrocells), feeding into an OR gate. The output of this PLA block is fed into the I/O architecture block. The different I/O and feedback options that are available in the 5C032 I/O block are shown in Figure 3.

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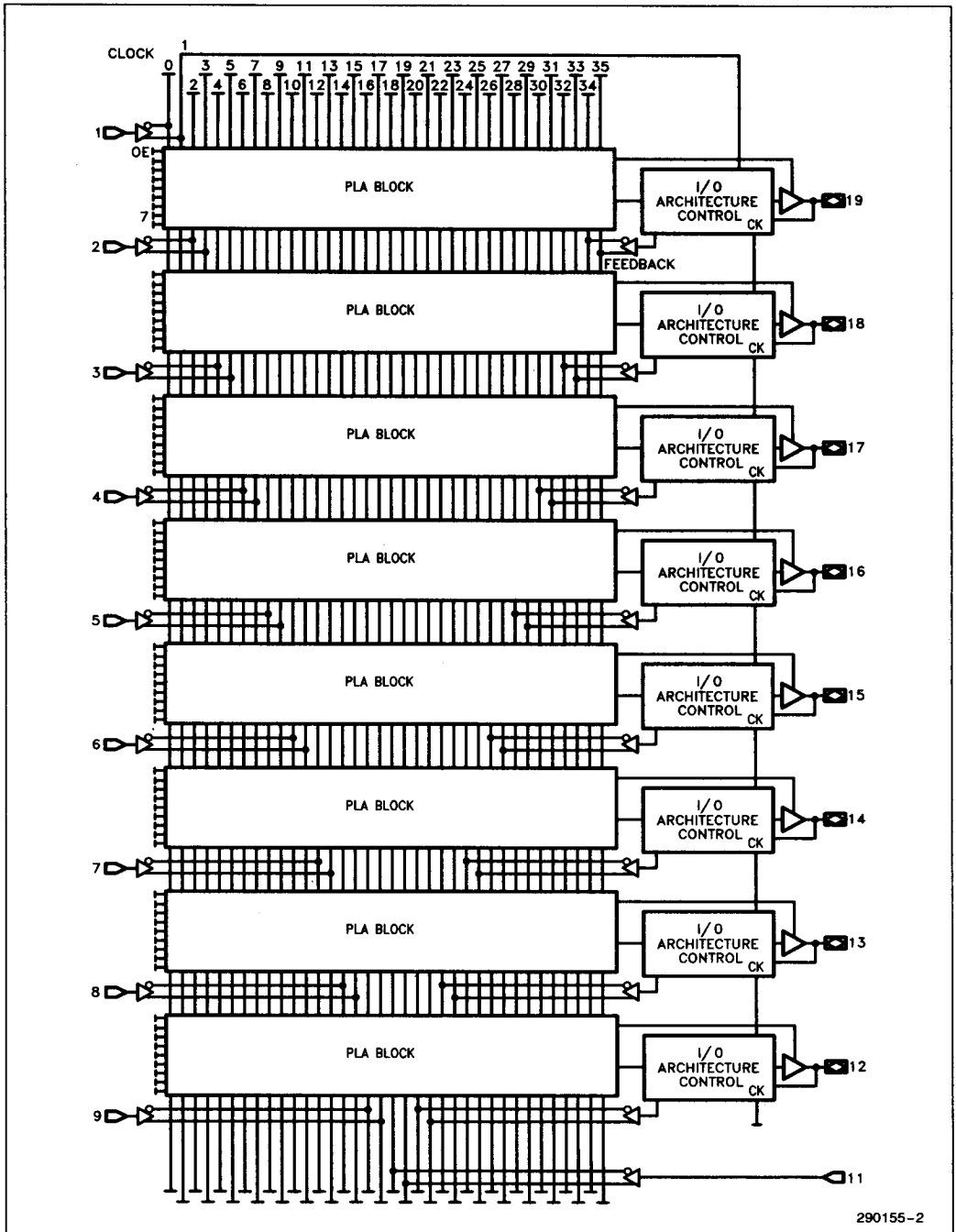
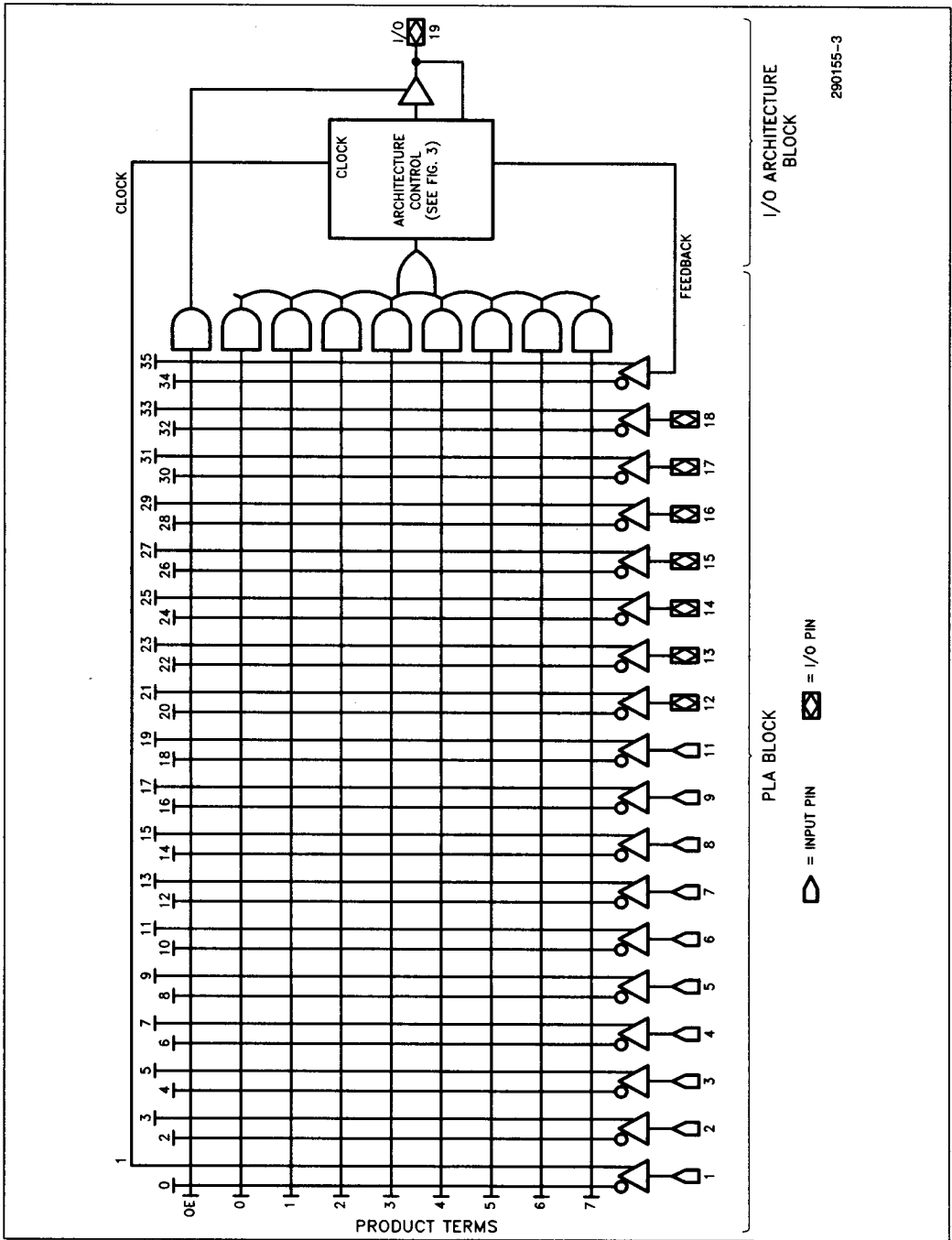

Figure 1. 5C032 Architecture
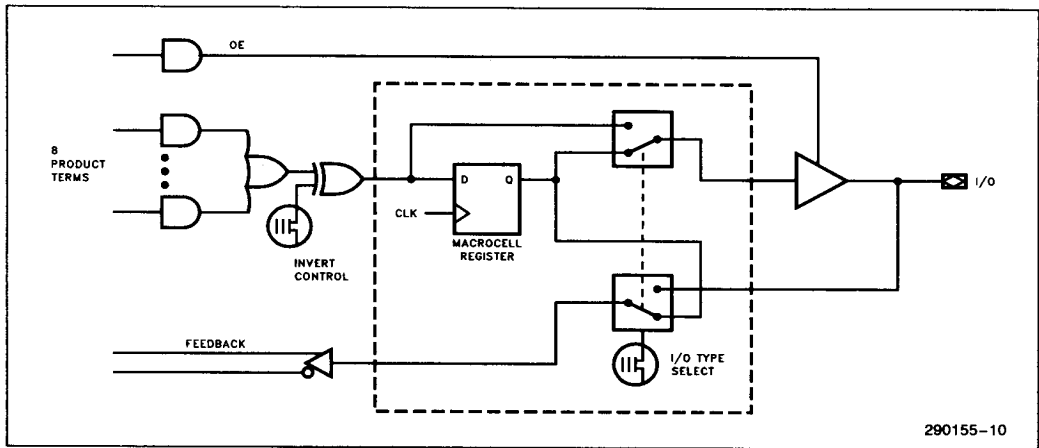
Figure 2. Logic Array Macrocell

Figure 3. 5C032 I/O Architecture Control

20 PIN CMOS COMPATIBILITY

The 5C032 is architected to be a logical superset of most 20 pin bipolar programmable array logic (PAL*) devices. The I/O and logic sections of the 5C032 device can be configured to emulate any of the devices listed below. Designers can make use of this feature by reducing the power of PAL based systems (PLDs are much lower power), replacing multiple PAL inventory items with a single PLD. Designers can also create new 20 pin PLD configurations by utilizing the individual logic and output controls of each macrocell.

List of PAL devices logically compatible with the 5C032.

16V8	16L2
10H8	16L8
12H6	16R8
14H4	16R6
16H2	16R4
16H8	16P8A
16C1	16RP8A
10LB	16RP6A
12L6	16RP4A
14L4	

*PAL is a registered trademark of Advanced Micro Devices.

Erased-State Configuration

Prior to programming or after erasing, the I/O structure is configured for combinatorial active low output with input (pin) feedback.

ERASURE CHARACTERISTICS

Erasure characteristics of the 5C032 are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000Å. It should be noted that sunlight and certain types of flourescent lamps have wavelengths in the 3000–4000Å. Data shows that constant exposure to room level flourescent lighting could erase the typical 5C032 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 5C032 is to be exposed to these types of lighting conditions for extended periods of time, conductive opaque labels should be placed over the device window to prevent unintentional erasure.

The recommended erasure procedure for the 5C032 is exposure to shortwave ultraviolet light with a wavelength of 2537Å. The integrated dose (i.e., UV intensity $\times$ exposure time) for erasure should be a minimum of fifteen (15) Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The 5C032 should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the 5C032 can be exposed to without damage is 7258 Wsec/cm^2 (1 week at 12,000 μW/cm^2). Exposure to high intensity UV light for longer periods may cause permanent damage to the device.

PROGRAMMING CHARACTERISTICS

Initially, and after erasure, all the EPROM control bits of the 5C032 are connected (in the "1" state). Each of the connected control bits are selectively disconnected by programming the EPROM cells into their "0" state. Programming voltage and waveform specifications are available by request from Intel to support programming of the device.

Intelligent Programming Algorithm

The 5C032 supports the Intelligent Programming Algorithm which rapidly programs Intel H-ELPDs (and EPROMs) using an efficient and reliable method. The Intelligent Programming Algorithm is particularly suited to the production programming environment.

This method greatly decreases the overall programming time while programming reliability is ensured as the incremental program margin of each bit is continually monitored to determine when the bit has been successfully programmed.

FUNCTIONAL TESTING

Since the logical operation of the 5C032 is controlled by EPROM elements, the device is completely testable. Each programmable EPROM bit controlling the internal logic is tested using application-independent test program patterns. After testing, the devices are erased before shipment to customers. No post-programming tests of the EPROM array are required.

The testability and reliability of EPROM-based programmable logic devices is an important feature over similar devices based on fuse technology. Fuse-based programmable logic devices require a user to perform post-programming tests to insure proper programming. These tests must be done at the device level because of the cummulative error effect. For example, a board containing ten devices each possessing a 2% device fallout translates into an 18% fallout at the board level (it should be noted that programming fallout of fuse-based programmable logic devices is typically 2% or higher).

DESIGN RECOMMENDATIONS

For proper operation, it is recommended that all input and output pins be constrained to the voltage range GND < (V_{IN} or V_{OUT}) < V_{CC}. Unused inputs should be tied to an appropriate logic level (e.g. either V_{CC} or GND) to minimize device power consumption. Reserved pins (as indicated in the iPLDS REPORT file) should be left floating (no connect) so that the pin can attain the appropriate logic level. A power supply decoupling capacitor of at least 0.2 μF must be connected directly between V_{CC} and GND pins of the device.

As with all CMOS devices, ESD handling procedures should be used with the 5C032 to prevent damage to the device during programming, assembly, and test.

DESIGN SECURITY

A single EPROM bit provides a programmable design security feature that controls the access to the data programmed into the device. If this bit is set, a proprietary design within the device cannot be copied. This EPROM security bit enables a higher degree of design security than fused-based devices since programmed data within EPROM cells is invisi-

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ble even to microscopic evaluation. The EPROM se-curity bit, along with all the other EPROM control bits, will be reset by erasing the device.

AUTOMATIC STAND-BY MODE

The 5C032 contains a programmable bit, the Turbo Bit, that optimizes operation for speed or for power savings. When the Turbo Bit is programmed (TURBO = ON), the device is optimized for maxi-mum speed. When the Turbo bit is not programmed (TURBO = OFF), the device is optimized for power savings by entering standby mode during periods of inactivity.

Figure 4 shows the device entering standby mode approximately 100 ns after the last input transition. When the next input transition is detected, the de-vice returns to active mode. Wakeup time adds an additional 15 ns to the propagation delay through the device as measured from the first input. No de-lay will occur if an output is dependent on more than one input and the last of the inputs changes after the device has returned to active mode.

After erasure, the Turbo Bit is unprogrammed (OFF); automatic standby mode is enabled. When the Tur-bo Bit is programmed (ON), the device never enters standby mode.

LATCH-UP IMMUNITY

All of the input, I/O, and clock pins of the 5C032 have been designed to resist latch-up which is inher-ent in inferior CMOS structures. The 5C032 is de-signed with Intel's proprietary CMOS II-E EPROM

process. Thus, each of the 5C032 pins will not expe-rience latch-up with currents up to ±100 mA and voltages ranging from −1V to (V_{CC} + 1V). Further-more, the programming pin is designed to resist latch-up to the 13.5V maximum device limit.

SOFTWARE SUPPORT

Full logic compilation and functional simulation for the 5C032 is supported by PLDshell Plus software.

PLDshell Plus design software is Intel's user-friendly design tool for µPLD design. PLDshell Plus allows users to incorporate their preferred text editor, pro-gramming software, and additional design tools into an easy-to-use, menued design environment that in-cludes Intel's PLDasm logic compiler and simulation software along with disassembly, conversion, and translation utilities. The PLDasm compiler and simu-lator software accepts industry-standard PDS source files that express designs as Boolean equa-tions, truth tables, or state machines. On-line help, datasheet briefs, technical notes, and error mes-sage information, along with waveform viewing/printing capability make the design task as easy as possible. PLDshell Plus software is available from Intel Literature channels or from your local Intel sales representative.

Tools that support schematic capture and timing simulation for the 5C032 are available. Please refer to the "Development Tools" section of the Program-mable Logic handbook.
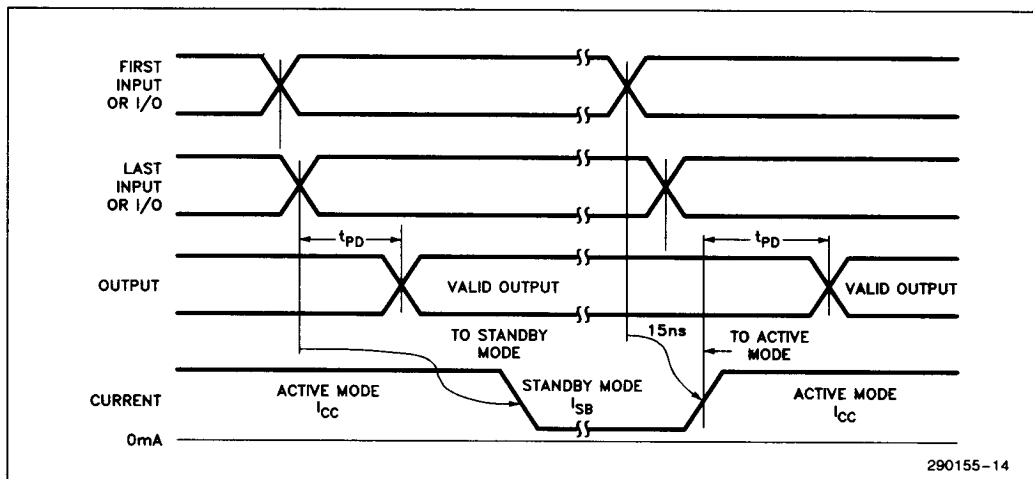

Figure 4. 5C032 Standby and Active Mode Transitions

The 5C032 is also supported by third-party compilers such as ABEL*, CUPL*, PLDesigner*, Log/IC, etc. Programming support is provided by third-party programmer companies such as Data I/O, Logical Devices, STAG, etc. Please refer to the "Third-Party Support" lists in the *Programmable Logic* handbook for complete information and vendor contacts.

ORDERING INFORMATION

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Order Code	Package	Operating Range
30	17	43.5	D5C032-30	CERDIP	Commercial
			P5C032-30	PDIP	
35	20	40	D5C032-35	CERDIP	Commercial
			P5C032-35	PDIP	
40	24	33.3	D5C032-40	CERDIP	Commercial
			P5C032-40	PDIP	
35	20	40	TP5C032-35	PDIP	Industrial

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*ABEL is a trademark of Data I/O, Corp. CUPL is a trademark of Logical Devices, Inc. PLDesigner is a trademark of MINC, Inc. Log/IC is a trademark of ISDATA, Incorporated.

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ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage(1)	−2.0	7.0	V
V_{PP}	Programming Supply Voltage(1)	−2.0	13.5	V
V_I	DC Input Voltage(1)(2)	−0.5	V_{CC}+0.5	V
t_{stg}	Storage Temperature	−65	+150	°C
t_{amb}	Ambient Temperature(4)	−10	+85	°C

NOTES:
1. Voltages with respect to ground.
2. Minimum DC input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to +7.0V for periods less than 20 ns under no load conditions.
3. Under bias, Extended temperature versions are also available.
4. Extended temperature versions also available.

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	0	+70	°C
t_R	Input Rise Time		500	ns
t_F	Input Fall Time		500	ns

D.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter/Test Conditions	Min	Typ	Max	• Unit
V_{IH}[5]	High Level Input Voltage	2.0		$V_{CC} + 0.3$	V
V_{IL}[5]	Low Level Input Voltage	−0.3		0.8	V
V_{OH}[6]	High Level Output Voltage $I_O = -4.0$ mA D.C., V_{CC} = min.	2.4			V
V_{OL}	Low Level Output Voltage $I_O = 4.0$ mA D.C., V_{CC} = min.			0.45	V
I_I	Input Leakage Current V_{CC} = max., GND < V_{IN} < V_{CC}			±10	μA
I_{OZ}	Output Leakage Current V_{CC} = max., GND < V_{OUT} < V_{CC}			±10	μA
I_{SC}[7]	Output Short Circuit Current V_{CC} = max., $V_{OUT} = 0.5V$			10	mA
I_{SB}[8]	Standby Current V_{CC} = max., $V_{IN} = V_{CC}$ or GND, Standby Mode		10	100	μA
I_{CC}[9]	Power Supply Current V_{CC} = max., $V_{IN} = V_{CC}$ or GND, No Load, Input Freq. = 10 MHz Active Mode (Turbo = Off), Device Prog. as 8-bit Ctr.		15	25	mA

NOTES:
5. Absolute values with respect to device GND; all over- and undershoots due to system or tester noise are included.
6. I_O at CMOS levels (3.84V) = −2 mA.
7. Not more than 1 output should be tested at a time. Duration of that test must not exceed 1 second.
8. With Turbo Bit = Off, device automatically enters standby mode approximately 100 ns after last input transition.
9. Maximum Active Current at operational frequency is less than 40 mA.

A.C. TESTING LOAD CIRCUIT

DEVICE OUTPUT — TO TEST SYSTEM

5V
855Ω
341Ω
C_L (INCLUDES JIG CAPACITANCE)

$C_L = 50$ pF

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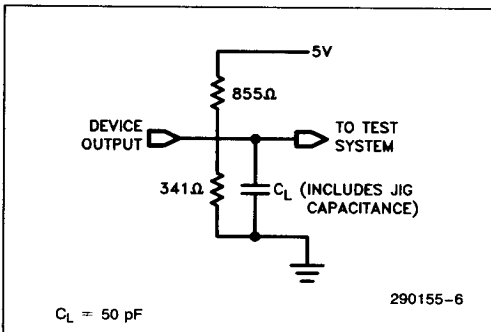
A.C. TESTING INPUT, OUTPUT WAVEFORM

INPUT 3.0 / 2.0 > TEST POINTS < 2.0 \ 0.8
0 \ 0.8 / 0.8

OUTPUT 1.5V — TEST POINTS — 1.5V

290155–7

A.C. Testing: Inputs are Driven at 3.0V for a Logic "1" and 0V for a Logic "0". Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0" on inputs. Outputs are measured at a 1.5V point. Device input rise and fall times < 6 ns.

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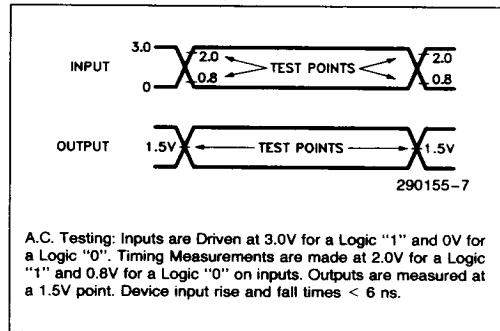
CAPACITANCE

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V, f = 1.0\ MHz$			10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V, f = 1.0\ MHz$			10	pF
C_{CLK}	Clock Pin Capacitance	$V_{IN} = 0V, f = 1.0\ MHz$			10	pF
C_{VPP}	V_{PP} Pin	Pin 11, f = 1.0 MHz			20	pF

A.C. CHARACTERISTICS $T_A = 0°C\ to\ +70°C, V_{CC} = 5V \pm5\%$, Turbo Bit On[10]

Symbol	From	To	5C032-30			5C032-35			5C032-40			Non-[8] Turbo Mode	Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PD}	I or I/O	Comb. Output			30			35			40	+15	ns
t_{PZX}[11]	I or I/O	Output Enable			30			35			40	+15	ns
t_{PXZ}[11]	I or I/O	Output Disable			30			35			40	+15	ns

NOTES:
10. Typ. values are at $T_A = 25°C, V_{CC} = 5V$, Active Mode.
11. t_{PZX} and t_{PXZ} are measured at $\pm0.5V$ from steady state voltage as driven by spec. output load. t_{PXZ} is measured with $C_L = 5\ pF$.
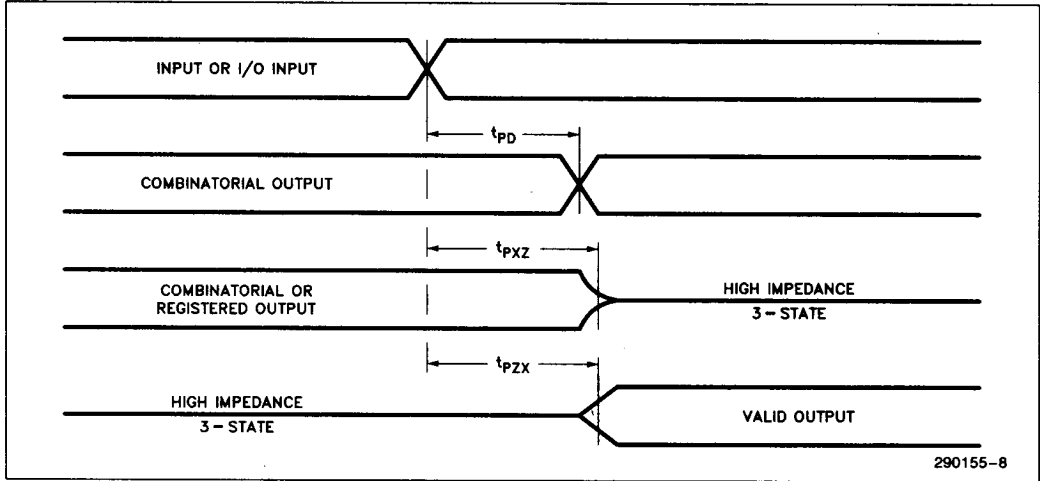
A.C. CHARACTERISTICS $T_A = 0°C\ to\ 70°C, V_{CC} = 5V \pm5\%$, Turbo Bit On [10]

SYNCHRONOUS CLOCK MODE

Symbol	Parameter	5C032-30 EP320-1			5C032-35 EP320-2			5C032-40			Non-[8] Turbo Mode	Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{MAX}	Max. Frequency (Pipelined) $1/t_{SU}$ — No Feedback			43.5			40			33.3		MHz
f_{CNT}	Max. Count Frequency $1/t_{CNT}$ — with Internal Feedback			28.5			25			21.7		MHz
t_{SU}	Input Setup Time to CLK	23			25			30			+15	ns
t_H	I or I/O Hold after CLK High	0			0			0				ns
t_{CO}	CLK High to Output Valid			17			20			24		ns
t_{CNT}	Register Output Feedback to Register Input — Internal Path	35			40			46			+15	ns
t_{CH}	CLK High Time	11			12			15				ns
t_{CL}	CLK Low Time	11			12			15				ns

SWITCHING WAVEFORMS

COMBINATORIAL MODE

INPUT OR I/O INPUT	
COMBINATORIAL OUTPUT	t_{PD}
COMBINATORIAL OR REGISTERED OUTPUT	t_{PXZ} — HIGH IMPEDANCE 3 – STATE
HIGH IMPEDANCE 3 – STATE	t_{PZX} — VALID OUTPUT

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SYNCHRONOUS CLOCK MODE

CLK1 — t_{CH} — t_{CL}

t_{SU} — t_H

INPUT MAY CHANGE — VALID INPUT — INPUT MAY CHANGE

t_{CO}

(FROM REGISTER TO OUTPUT) — VALID OUTPUT

290155-9

Current in Relation to Frequency

Conditions: $T_A = 0°C$, $V_{CC} = 5.25V$

290155-11

Current in Relation to Temperature

Conditions: $V_{CC} = 5.25V$

290155-12

Output Drive Current in Relation to Voltage

Conditions: $T_A = +25°C$, $V_{CC} = 5V$

290155-13

t_{PD} Derating vs Capacitive Loading

Conditions:
$T_A = 25°C$
$V_{CC} = 5.0V$

290155-15