

# 576-BIT BIPOLAR RAM (64×9)

# 82S09/82S19 (O.C.)

## DESCRIPTION

The organization of this device allows byte storage of data, including parity. Where parity is not monitored, the ninth bit can be used as a tag or status indicator for each word stored. Ideal for scratch-pad, push-down stacks, buffer memories, and other internal memory applications in which cost and performance requirements dictate a wide data path in favor of word depth.

The 82S09/19 features open collector outputs, chip enable input, and a very low current pnp input structure to enhance memory expansion.

During Write operation, the 82S19 output goes to a "1".

The 82S09/19 is available in the commercial and military temperature ranges. For the commercial temperature ranges (0°C to +75°C) specify N82S09/19, F or N and for the military temperature range (-55°C to +125°C) specify S82S09/19 I, R or F.

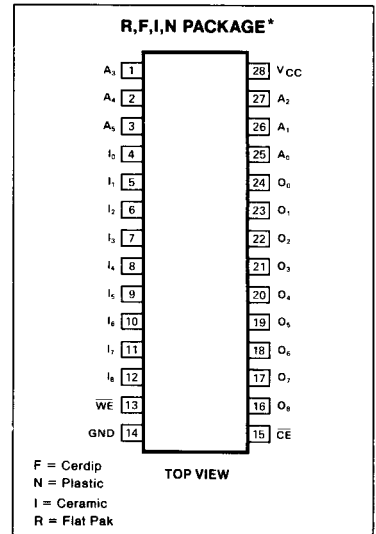
## FEATURES

- Address access time:
  - N82S09: 45ns max
  - S82S09: 80ns max
  - N82S19: 35ns max
  - S82S19: 60ns max
- Write cycle time:
  - N82S09/19: 45ns max
  - S82S09: 80ns max
  - S82S19: 70ns max
- Power dissipation: 1.3mW/bit typ
- Input loading:
  - N82S09/19: -100µA max
  - S82S09/19: -150µA max
- On-chip address decoding
- Schottky clamped
- Fully TTL compatible
- 82S09 Output is Non-Blanked During Write
- 82S19 Output is Blanked During Write

## APPLICATIONS

- Buffer memory
- Control register
- FIFO memory
- Push down stack
- Scratch pad

## PIN CONFIGURATION

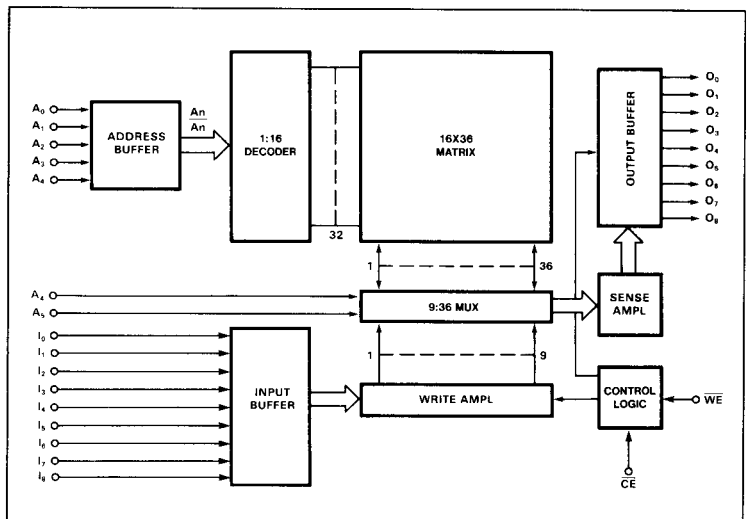


## TRUTH TABLE

MODE	CE	WE	I <sub>N</sub>	O <sub>N</sub>	
				82S09	82S19
Read	0	1	X	Complement of data stored	
Write "0"	0	0	0	1	1
Write "1"	0	0	1	0	1
Disabled	1	X	X	1	1

X = Don't care

## BLOCK DIAGRAM



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## ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V <sub>CC</sub>	Supply voltage	+7	V <sub>dc</sub>
V <sub>IN</sub>	Input voltage	+5.5	V <sub>dc</sub>
	Output voltage		V <sub>dc</sub>
V <sub>OH</sub>	High	+5.5	
T <sub>A</sub>	Temperature range		°C
	Operating	0 to +75	
	N82S09/19	-55 to +125	
	S82S09/19	-65 to +150	
T <sub>STG</sub>	Storage		

**DC ELECTRICAL CHARACTERISTICS<sup>1,7</sup>**
N82S09/19: 0°C ≤ T<sub>A</sub> ≤ +75°C, 4.75V ≤ V<sub>CC</sub> ≤ 5.25VS82S09/19: -55°C ≤ T<sub>A</sub> ≤ +125°C, 4.75V ≤ V<sub>CC</sub> ≤ 5.25V

PARAMETER <sup>1</sup>	TEST CONDITIONS	N82S09/19			S82S09/19			UNIT
		Min	Typ	Max	Min	Typ	Max	
V <sub>IL</sub> V <sub>IH</sub> V <sub>IC</sub>	Input voltage Low High Clamp <sup>2</sup>			.85	2.2		.80	V
		2.0		-1.5			-1.5	
V <sub>OL</sub>	Output voltage Low <sup>3</sup>			0.5			0.5	V
I <sub>IL</sub> I <sub>IH</sub>	Input current Low High			-100 25			-150 40	μA
I <sub>OLK</sub>	Output current Leakage <sup>4</sup>			40			60	μA
I <sub>CC</sub>	V <sub>CC</sub> supply current <sup>5</sup>			190			200	mA
C <sub>IN</sub> C <sub>OUT</sub>	Capacitance Input Output		5 8			5 8		pF

Refer to notes on next page.

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## AC ELECTRICAL CHARACTERISTICS<sup>7</sup>

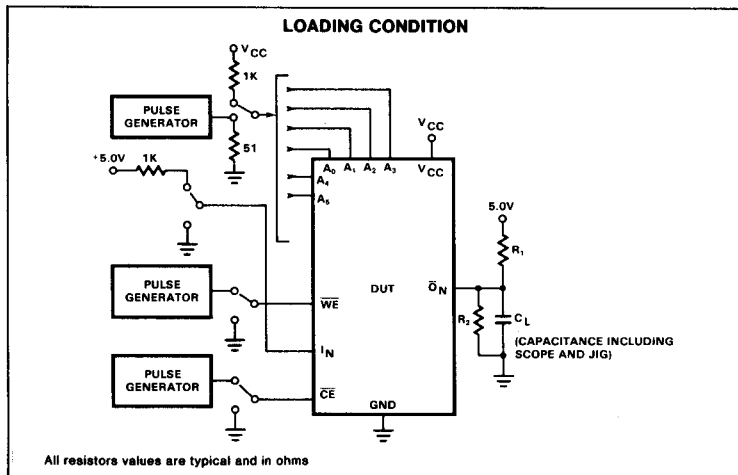
$R_1 = 600\Omega$ ,  $R_2 = 900\Omega$ ,  $C_L = 30pF$ , for 82S09  
 $R_1 = 510\Omega$ ,  $R_2 = 750\Omega$ ,  $C_L = 30pF$ , for 82S19  
 N82S19:  $0^\circ \leq T_A \leq +75^\circ C$ ,  $4.75V \leq V_{CC} \leq 5.25V$   
 S82S19:  $-55^\circ C \leq T_A \leq +125^\circ C$ ,  $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	N82S09			S82S09			N82S19			S82S19			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
T <sub>AA</sub> T <sub>CE</sub>	Access time				45			80			35			60	ns
	Address				30			50			25			40	
T <sub>CD</sub> T <sub>WD</sub> T <sub>WR</sub>	Disable time	Output			30			50			25			35	ns
	Valid time	Output			50			80			25			50	
	Write recovery time	Output	Chip enable											50	
T <sub>WSA</sub> T <sub>WHA</sub>	Setup and hold time	Write enable	Address	Setup time	10			5			10			ns	
	Hold time			5			5			10					
T <sub>WSD</sub> T <sub>WHD</sub>	Setup time	Write enable	Data in	Setup time	50			30			45			ns	
	Hold time			35			5			5					
T <sub>WSC</sub> T <sub>WHC</sub>	Setup time	Write enable	$\overline{CE}$	Setup time	10			5			10			ns	
	Hold time			5			5			10					
T <sub>WP</sub>	Pulse width				35			50			35			50	ns
	Write enable <sup>6</sup>														

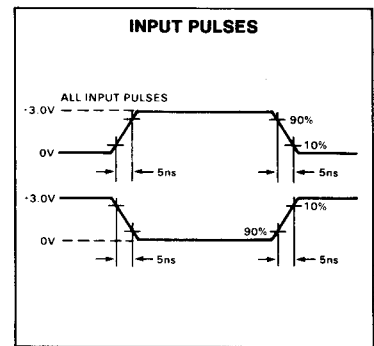
**NOTES**

- All voltage values are with respect to network ground terminal.
- Test each input one at a time.
- Measured with the logic low stored. Output sink current is supplied through a resistor to  $V_{CC}$ .
- Measured with  $V_{IH}$  applied to  $\overline{CE}$ .
- $I_{CC}$  is measured with the write enable and chip enable input grounded, all other inputs at 4.5V, and the outputs open.
- Minimum required to guarantee a Write into the slowest bit.
- The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.

## TEST LOAD CIRCUIT



## VOLTAGE WAVEFORM



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