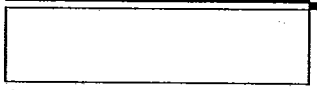
LC5863H, 5864H

T-49-19-04

3044B

CMOS LSI



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4-Bit Single Chip Microcomputer

On-Chip LCD Driver, 12K/16K-Byte ROM, 1K-Bit RAM

The LC5863H/64H are CMOS type 4-bit single chip microcomputers with internal 6K/8K-byte ROM, 1K-bit RAM and LCD driver. The internal functions of the LC5863H/64H microcomputers can operate at low voltage level.

Applications:
- Control and LCD display for cameras, CDs and tuners
- Remote control for VCRs, tuners, and the like
- Control and LCD display for small-sized measuring instruments and measuring equipment in medical field, and,
- Control and LCD display for electronic appliances with LCD display function, particularly for household products driven by dry battery

Features:
The LC5863H/64H 4-bit single chip microcomputers are highly advanced models of the LC5800 series microcomputers, and have the following features.

(1) Faster cycle time
- V_{DD} = 4.5 to 6.0V: 2 microseconds
- V_{DD} = 2.2 to 6.0V: 10 microseconds

(2) Lower current dissipation
- 4MHz-CF oscillation (5.0V): 600 microamperes (typ.) (HALT mode) 1.7 milliamperes (typ.) (basic operation mode with cycle time = 2 microseconds)
- 32kHz-X'tal oscillation (3.0V and CF stop): 4.0 microamperes (HALT mode), 20 microamperes (typ.) (basic operation mode with cycle time = 122 microseconds)

(3) More advanced timer function
- 2-channel 8-bit timer counters (usable as event counters)
- Time base clock timer (clocking)
- Watchdog timer

(4) Improvement in standby function
- Clock standby function (HALT mode): low speed mode (low current dissipation)/ high speed mode selectable in application programs
- Full-scale standby function (HOLD mode)
- HALT/HOLD mode release function by external interrupt terminal, input port (max. 9), and serial I/O

(5) More advanced I/O function
- External interrupt terminal
- Input and Input/Output terminals (max. 9) with HALT/HOLD mode release request signal inputs
- Input port terminals (max.24) with software-controllable input resistors: The input resistors (pull-up and pull-down resistors) can be selected by mask option.
- Internal prevention circuits for input port floating (max. 25)
- LCD drivers: 4 common output terminals and 35 segment output terminals
- 20 general purpose I/O port terminals
- 5 general purpose input port terminals
- 39 general purpose output port terminals (All LCD segment port terminals selected as general purpose output port terminals)
- 8-bit serial input/output port (Input terminal, output terminal and timing clock terminal)

Functional overview
- Internal ROM: 4096 x 16 bits (LC5864H), 3072 x 16 bits (LC5863H). Internal RAM: 256 x 4 bits
- Single stepping of all instructions
- Cycle time and operating voltage range
  2 microseconds -- V_{DD} = 4.5V to 6.0V
  10 microseconds -- V_{DD}= 2.2V to 6.0V
  122 microseconds -- V_{DD} = 2.0V to 6.0V
- HALT/HOLD release function and useful interrupt function
  a. 8 types of HALT release functions
  b. 7 types of HOLD release functions
  c. 7 types of interrupt functions (usable as external interrupt)
  d. 8-level subroutine nesting (including interrupt levels)
  e. Internal watchdog timer function
- Hardware design for improving processing capability
  a. Internal segment PLA circuit and internal segment decoder: The relationship between LCD driver output and segment numbers of the LCD panel is established by the internal hardware logics, without software control. Note that the LCD driver output terminals can be selected as the general purpose output port terminals.
  b. Internal 8-bit synchronous-mode serial input/output circuit
  c. Two internal 8-bit read/write timers (usable as event counters)
  d. Working area: All the RAM area can be used as the working area (RAM bank register technique).
  e. Internal RAM data pointer
  f. Internal clocking oscillator and 15-level divider (also used as the alternating frequency generator for LCD display)
- Versatile LCD panel driving output terminals (35 terminals)

Drivable LCD panel type	Number of segments drivable	Number of common terminals
1/3 bias-1/4 duty	140 segments	4 COM terminals
1/3 bias-1/3 duty	105 segments	3 COM terminals
1/2 bias-1/4 duty	140 segments	4 COM terminals
1/2 bias-1/3 duty	105 segments	3 COM terminals
1/2 bias-1/2 duty	70 segments	2 COM terminals
Static	35 segments	1 COM terminal

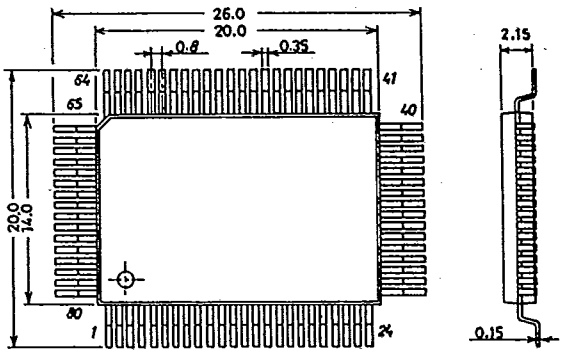
  a. The LCD driver output terminals can be also selected as general purpose output terminals.

C-MOS type output terminal	35 output terminals (max.)
Pch type output terminal	35 output terminals (max.)
Nch type output terminal	35 output terminals (max.)

- Versatility in oscillator selection: Various system types can be designed.
  a. Crystal oscillator (32kHz/65kHz/38kHz): Time base clock, system clock and LCD alternating frequency
  b. Ceramic resonator oscillator (400kHz to 4MHz): System clock and timer/serial counter clock
  c. RC oscillator (200kHz to 1MHz): System clock and timer/serial counter clock
  d. External clock: System clock and timer/serial counter clock

Delivery form: Package (QIP-80) and chip

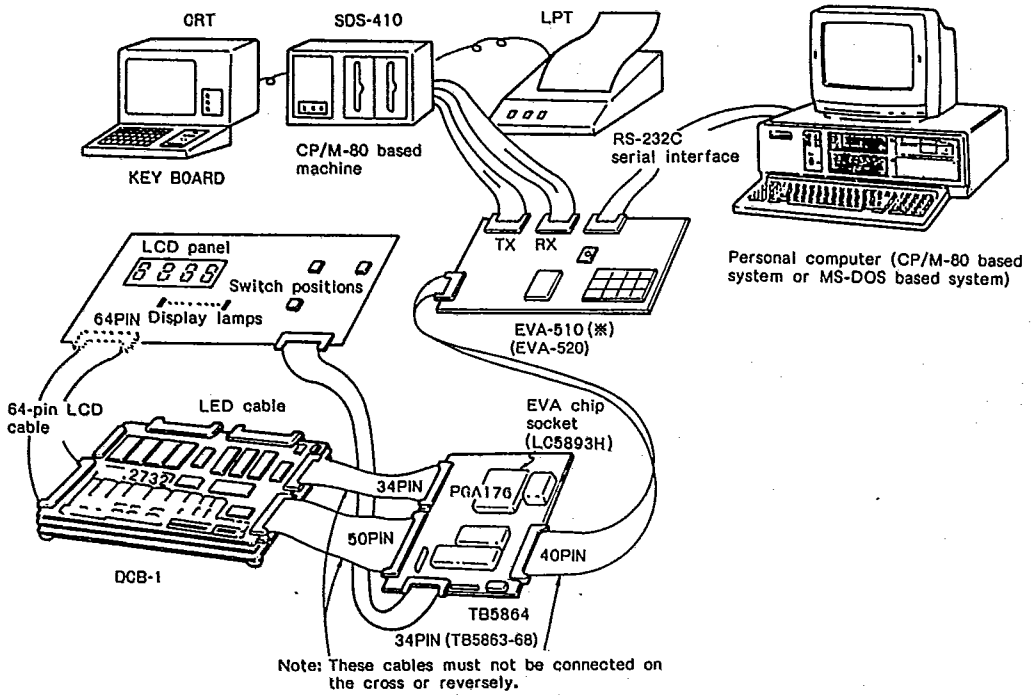
Case outline 3044B-Q80AIC
(unit:mm)



SANYO: QIP80A

Application development support tool systems
The following support tool systems are provided in order to develop applications for the LC5864H microcomputers.

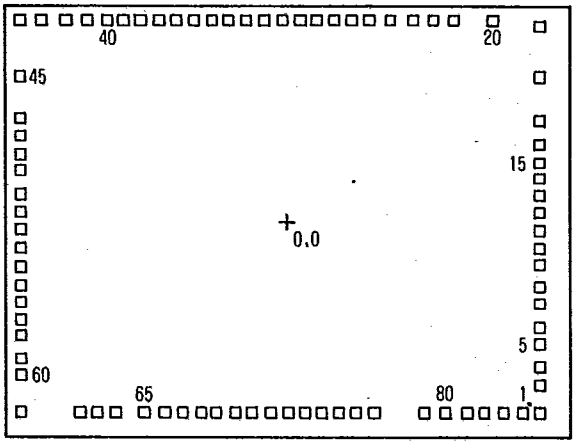
1. Software support tools
   (1) Cross assembler and mask option selection program for the SDS-410 (CP/M-80) system
   (2) Cross assembler and mask option selection program for the personal computers (IBM-PC/XT, IBM-PC/AT compatible)
   (3) Cross assembler
      (i) CP/M-80 : LC5864.COM
      (ii) MS-DOS : LC5864.EXE
   (4) Mask option selection program
      (i) CP/M-80 : SU5864.COM
      (ii) MS-DOS : SU5864.EXE
2. Hardware support tools
   (1)Evaluation chips : LC5893U --- Internal pull-up resistor
   : LC5893D --- Internal pull-down resistor
   (2) Mask option controller: DCB-1
   (3) EVA-chip board: TB5864, TB5863-68***
   (4) EVA board: EVA-510*, EVA-520**
   * EVA-510: The EVA-510 evaluation board is a new version of the EVA- 410 EVA board. On the EVA-510 EVA board is mounted a monitor ROM for the LC5800 series, LC5700 series and LC86000 series microcomputers.
   ** EVA-520: The EVA-520 evaluation board is a new version of the EVA-410 EVA board. The ROM writer function of the EVA-410 is extended up to 512 bits and a monitor ROM for the LC5800 series, LC5700 series and LC8600 series is mounted.
   *** The TB5863-68 is an EVA-chip board is intended for program development of four Type Nos. of the LC5863H,5864H,5866H, and 5868H.
   (5) EVA-510 monitor ROM: SCR5864
   The application development support tool systems are illustrated in the following figure.



Outline of development support tool systems

Note) (1) The IBM-PC/XT, IBM-PC/AT are IBM-made products.
(2) The SDS-410 is for parallel input/output.

Pin assignment and pad assignment
Chip size 5.85mmx4.50mm
Pad size 120μmx120μm
Chip height 330 μm (package form delivery)
480 μm (chip form delivery)

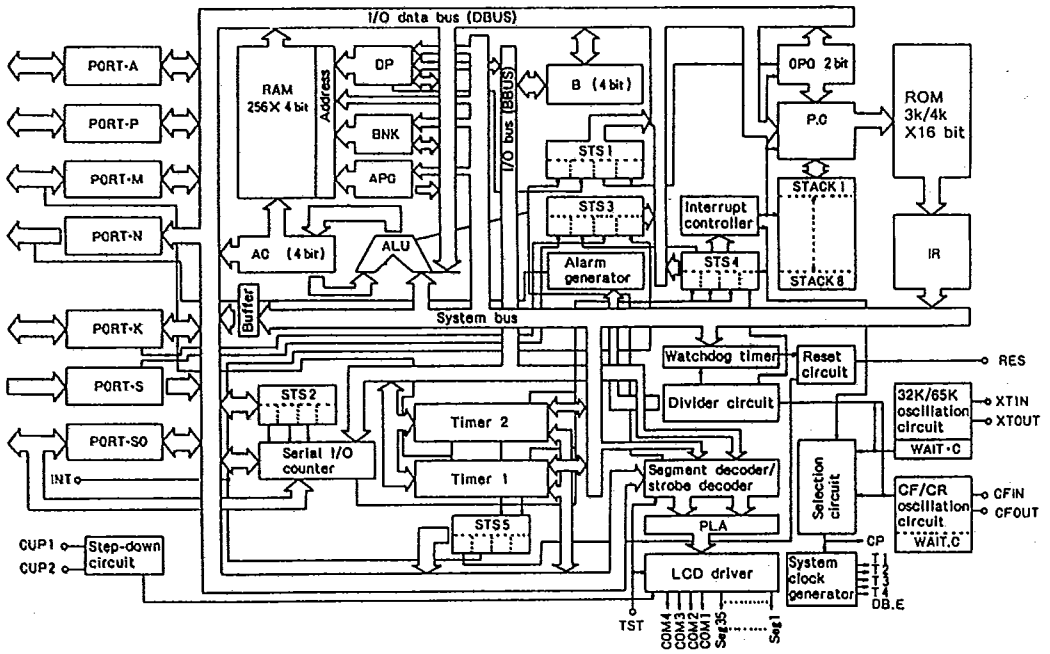


QIP-80, Pad No. and coordinate value

PIN No	PAD No	Name	Coordinate value Xμm	Yμm	PIN No	PAD No	Name	Coordinate value Xμm	Yμm	PIN No	PAD No	Name	Coordinate value Xμm	Yμm
24	1	VDD	2420	−1950	51	29	Seg8	110	2110	77	57	Seg34	−2780	− 980
—	2	Test	2620	−1950	52	30	Seg9	− 70	↑	78	58	Seg35	↑	−1160
25	3	CFIN	↑	−1685	53	31	Seg10	− 250	↓	79	59	COM4	↓	−1380
26	4	CFOUT	↓	−1490	54	32	Seg11	− 430	↓	80	60	COM3	↓	−1570
27	5	S1	↓	−1260	55	33	Seg12	− 610	↓	1	61	COM2	−2780	−1950
28	6	S2 Input port	↓	−1075	56	34	Seg13	− 790	↓	2	62	COM1	−2145	↑
29	7	S3 Input port	↓	− 840	57	35	Seg14	− 970	↓	3	63	CUP1	−1965	↓
30	8	S4 Input port	↓	− 660	58	36	Seg15	−1150	↓	4	64	CUP2	−1785	↓
31	9	K1 Input/output port	↓	− 435	59	37	Seg16	−1330	↓	5	65	RES	−1475	↓
32	10	K2 Input/output port	↓	− 255	60	38	Seg17	−1510	↓	6	66	INT Input/output port or serial input/output port	−1290	↓
33	11	K3 Input/output port	↓	− 75	61	39	Seg18	−1690	↓	7	67	SO1 Input/output port or serial input/output port	−1100	↓
34	12	K4 Input/output port	↓	105	62	40	Seg19	−1870	↓	8	68	SO2 Input/output port or serial input/output port	− 920	↓
35	13	M1 Input/output port	↓	290	—	41	Test	−2050	↓	9	69	SO3 Input/output port or serial input/output port	− 740	↓
36	14	M2 Input/output port	↓	470	—	42	Test	−2285	↓	10	70	SO4 Input/output port or serial input/output port	− 560	↓
37	15	M3 Input/output port	↓	650	63	43	Seg20	−2560	↓	11	71	A1 Input/output port	− 380	↓
38	16	M4 Input/output port	↓	830	64	44	Seg21	−2780	2110	12	72	A2 Input/output port	− 200	↓
39	17	N1 Output port	↓	1055	65	45	Seg22	↑	1525	13	73	A3 Input/output port	− 20	↓
40	18	N2 Output port	↓	1510	66	46	Seg23	↓	1110	14	74	A4 Input/output port	160	↓
41	19	N3 Output port	2620	2040	67	47	Seg24	↓	930	15	75	P1 Input/output port	345	↓
42	20	N4 Output port	2100	2110	68	48	Seg25	↓	750	16	76	P2 Input/output port	525	↓
43	21	TST	1720	↑	69	49	Seg26	↓	570	17	77	P3 Input/output port	705	↓
44	22	Seg1	1495	↓	70	50	Seg27	↓	315	18	78	P4 Input/output port	885	↓
45	23	Seg2	1275	↓	71	51	Seg28	↓	135	19	79	XTOUT	1420	↓
46	24	Seg3	1055	↓	72	52	Seg29	↓	− 45	20	80	XTIN	1620	↓
47	25	Seg4	835	↓	73	53	Seg30	↓	− 225	21	81	VDD2	1845	↓
48	26	Seg5	650	↓	74	54	Seg31	↓	− 440	22	82	VDD1	2030	↓
49	27	Seg6	470	↓	75	55	Seg32	↓	− 620	23	83	VSS	2220	−1950
50	28	Seg7	290	2110	76	56	Seg33	−2780	− 800					

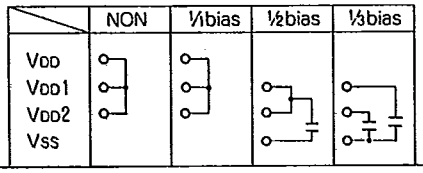
-PIN No. indicates the pin numbers on an QIP-80 production package.
-The TST pin should be connected to the VSS pin.
-Pad numbers 2, 41 and 42 must be left open.
-Pin-to-pin soldering should be used in mounting an QIP-80 package onto printed circuit board (PCB). That is, entire package dipping should be avoided. Keep it in mind.

The system block diagram of the LC5863H/64H microcomputers is shown below.



RAM	: Data memory	IR	: Instruction register
ROM	: Program memory	STS1	: Status register 1
DP	: Data pointer register	STS2	: Status register 2
BNK	: Bank register	STS3	: Status register 3
APG	: RAM page flag	STS4	: Status register 4
AC	: Accumulator	STS5	: Status register 5
ALU	: Arithmetic and logical operation unit	PLA	: Programmable logic array for segment data/strobe data
B	: B register	WAIT.C	: Wait time counter
OPG	: ROM page flag		
PC	: Program counter		

Pin description

Pin name	I/O	QIP-80 Pin number	Functional description	Option	Reset status
VDD VSS	— —	24 23	Power supply		
VDD1 VDD2	— —	22 21	LCD driving power  		
CUP1 CUP2	— —	3 4	Switching terminals for supplying LCD driving voltage to the VDD1 and VDD2 terminals. - These two terminals are to be connected with a nonpolarized electrolytic capacitor when 1/2 bias or 1/3 bias specifications are adopted. - These two terminals should be left open when any specifications other than 1/2 bias and 1/3 bias.		
CFIN CFOUT	Input Output	25 26	Used for generating system clock frequency - Used for connection with a ceramic resonator - Used for connection with an RC circuit - Used for receiving and supplying external clock signals to internal functional block (CFOUT to be left open). The operation can be stopped with the HOLD or SLOW instruction.	①CF specification ②RC specification ③External clock specification ④Not used	
XTIN XTOUT	Input Output	20 19	Used for supplying base clocks (clock mode and LCD alternating frequency) and system clock signals to internal block - Used for connection with 32KHz crystal oscillator - Used for connection with 65KHz crystal oscillator. The operation can be stopped with the HOLD instruction.	①32K specification ②65K specification ③38K specification ④Not used	
S1 S2 S3 S4	Input	27 28 29 30	Input port - Input terminal for receiving and inputting data to the RAM from external units. - Provided with internal chattering rectification circuit of 7.8 milliseconds or 1.95 milliseconds. - Provided with internal pull-up/pull-down resistor. Note: The values, 7.8 milliseconds and 1.95 milliseconds, apply to the specification with ø0 = 32.768 kHz.	①"L"/"H" level hold Tr selection ②Pull-up/pull- down resistor selection	- Pull-up/pull-down resistor ON Note: Forced into floating state after reset.
K1 K2 K3 K4	Input/ output	31 32 33 34	Input/output port - Input terminal for receiving and inputting data to the RAM from an external unit. - Output terminal for reading and outputting data to an external unit from the RAM. - When the input mode has been selected, data from an external unit is adjusted by chattering rectification circuit (7.8 milliseconds or 1.95 milliseconds). One of the values, 7.8 or 1.95 milliseconds can be selected by the SSW instruction. With this instruction, the same value for the S port is also selected at the same time. Refer to the SSW instruction. - Provided with internal pull-up/pull-down resistor. Note: The values, 7.8 milliseconds and 1.95 milliseconds, apply to the specification with ø0 = 32.768 kHz.	①"L"/"H" level hold Tr selection ②Pull-up/pull-down resistor selection	- Pull-up/pull-down resistor ON Note: Forced into floating state after reset. - Input mode - Output latch data level = "H"
M1 M2 M3 M4	Input/ output	35 36 37 38	Input/output port - Input terminal for receiving and inputting data to the RAM from an external unit. - Output terminal for reading and outputting data to an external unit from the RAM. - M3 is used as input terminal for external clock at mode 3 of TM1. - M4 is used as input terminal for external clock at mode 3 of TM2. * External clock cycle is minimum cycle time x 2. - Provided with internal pull-up/pull- down resistor.	Same as the K port (K1 to K4)	Same as the K port (K1 to K4)
A1 A2 A3 A4	Input/ output	11 12 13 14	Input/output port Functions: Same as the M port (M1 to M4)	Same as the K port (K1 to K4)	Same as the K port (K1 to K4)
P1 P2 P3 P4	Input/ output	15 16 17 18	Input/output port Functions: Same as the M port (M1 to M4)	Same as the K port (K1 to K4)	Same as the K port (K1 to K4)

Pin name	I/O	QIP-80 pin number	Functional description	Option	Reset status
SO1 SO2 SO3 SO4	Input/ output	7 8 9 10	Input/output port Functions: Same as the M port (M1 to M4) Terminals SO1 to SO3 can be also used as the serial interface function. - The serial mode can be selected in your application programs. - Terminal functions: SO1 for serial data input, SO2 for serial data output, SO3 for serial clock. - Serial clocks can be selected in your application program: External/internal and rise edge output/fall edge output.	①"L"/"H" level hold Tr selectable ②Internal pull-up/pull-down resistor selectable ③Internal serial clock divider ratio selectable i) 1/1 ii) 1/2 iii) 1/4	Same as the K port (K1 to K4).
N1 N2 N3 N4	Output	39 40 41 42	Output port - Output terminal for outputting data to an external unit from the RAM. - Terminal N4 for outputting alarm signals (Condition: output latch data level = "L") - The alarm signal frequency can be selected from 4kHz, 2kHz and 1kHz in your application program (condition: ϕ0 = 32.768kHz).	①Output formats for terminals N1 to N4. i) CMOS output format, ii) N-ch open drain format	N1 to N4 output level: "H".
INT	Input	6	Input port - Input terminal for external interrupt request signals. - Input terminal for receiving and inputting data from an external unit to the RAM. - Interrupt signals can be detected either at the rise edge or fall edge. - Provided with internal pull-up/pull-down resistor.	①"L"/"H" level hold Tr selectable ②Internal pull-up/pull-down resistor selectable ③Detection signal edge (rise or fall) selectable	
RES	Input	5	Input terminal for receiving reset signals to reset the LSI internal functions. - Input level can be either "H" or "L". - Provided with internal pull-up/pull-down resistor. Note: The reset signal should stay at the same level for more than 200 microseconds.	①Internal resistor selection: Pull-up, pull-down and open. ②Reset level selectable: "L" or "H" level	
TST	Input	43	Test input terminal - FLP-80 package: Must be connected to the VSS pin. - Chip: Must be left open or connected to the VSS pin.		
SEG1 SEG2 to SEG35	Output	44 45 to 78	1) LCD panel drivers or normal output terminals - LCD panel drivers. i) STATIC format. ii) 1/2 bias-1/2 duty format. iii) 1/2 bias-1/3 duty format. iv) 1/2 bias-1/4 duty format. v) 1/3 bias-1/3 duty format. vi) 1/3 bias-1/4 duty format. Formats i) to vi) can be selected by mask option. - Normal output terminals. i) CMOS output format. ii) P-ch open drain output format. iii) N-ch open drain output format. Output formats i) to iii) can be selected by mask option. 2) LCD driver/normal output function selection requires no command from your application program. It is controlled by the PLA circuit. 3) Latch output level controllable at standby state caused by oscillation stop and reset signal 4) Any combination of LCD driver function and normal output function can be selected.	①LCD driver output/ normal output selectable ②LCD driving format selection: i) STATIC driving format. ii) 1/2 bias-1/2 duty driving format. iii) 1/2 bias-1/3 duty driving format. iv) 1/2 bias-1/4 duty driving format. v) 1/3 bias-1/3 duty driving format. vi) 1/3 bias-1/4 duty driving format ③Normal output function selectable. CMOS output format - P-ch open drain output format - N-ch open drain output format ④Latch output level selection at standby mode	①LCD driver mode - All segments ON - All segments OFF. * These two output logic modes at the reset can be selected by mask option. ②Normal output mode - H level - L level * These two output logic modes can be selected by mask option. Note: If a certain combination of LCD driver mode/normal output mode is adopted, the following two logic statuses at the reset can be selected by mask option. - All segments ON/"H" level - All segments OFF/"L" level ③The STATIC LCD driving format is employed as long as the reset signal is active.

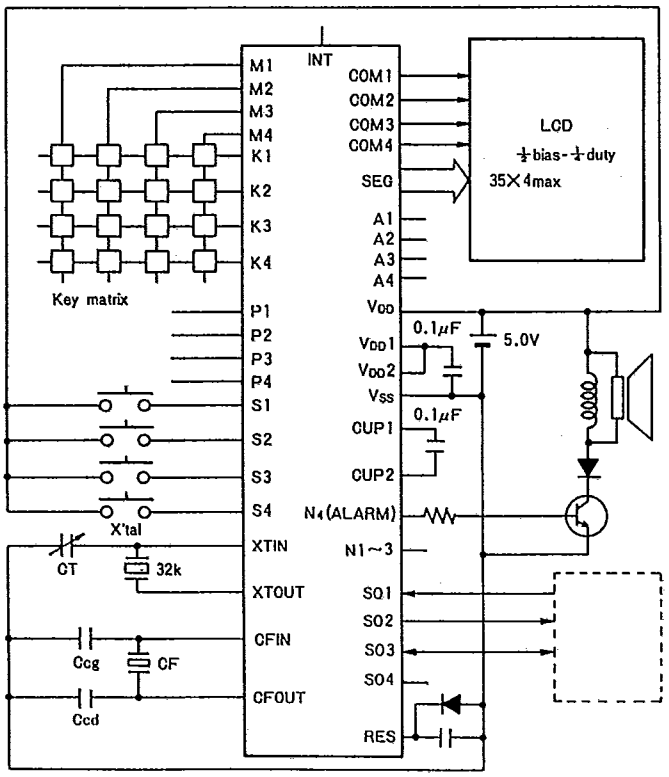
Pin name	I/O	QIP-80 pin number	Functional description	Option	Reset state
COM1 COM2 COM3 COM4	Output	2 1 80 79	Output terminals for applying power to common electrodes (COMMON terminals) of the LCD panel. The following terminal combinations can be selected for the four types of lighting formats (condition: $\phi 0$ = 32.768kHz).		The STATIC lighting format is employed as long as the reset signal is active. *If the CF, RC or EXT oscillation option is selected, it may happen that alternating frequency signal supply stops. Such an occurrence depends on oscillation optional selections.

	STATIC	½duty	⅓duty	¼duty
COM1	○	○	○	○
COM2	×	○	○	○
COM3	×	×	○	○
COM4	×	×	×	○
Alternating frequency	32Hz	32Hz	42.7Hz	32Hz

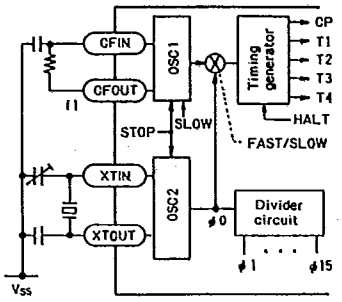
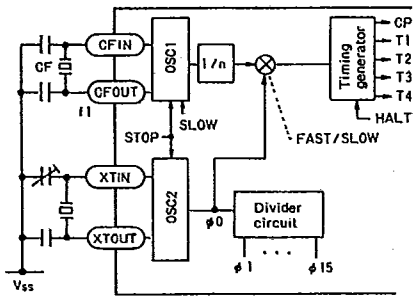
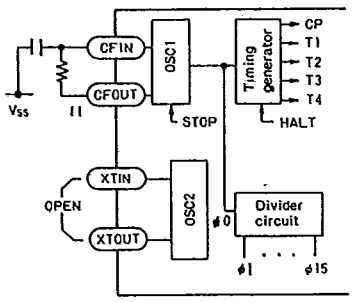
Note: The COMMON terminals indicated by X cannot be used by the corresponding lighting formats.

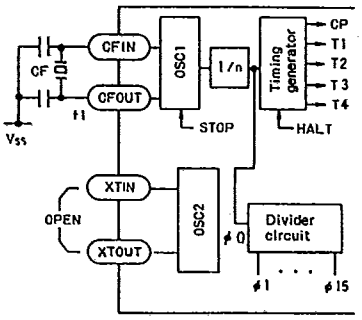
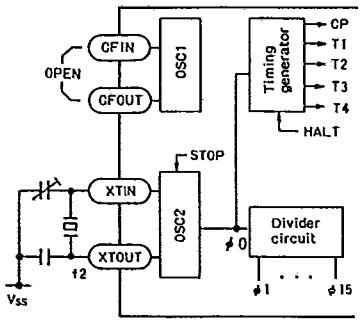
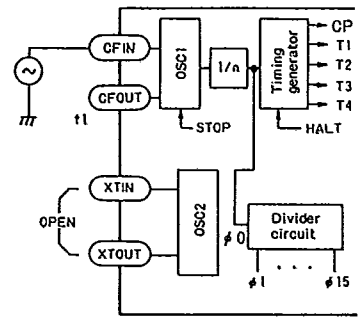
Sample application circuit

LCD : ½bias-¼duty

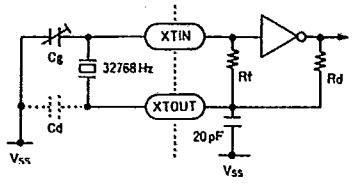
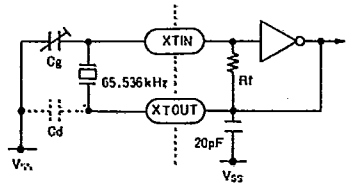


Oscillation circuit options

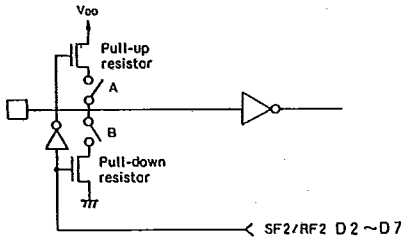
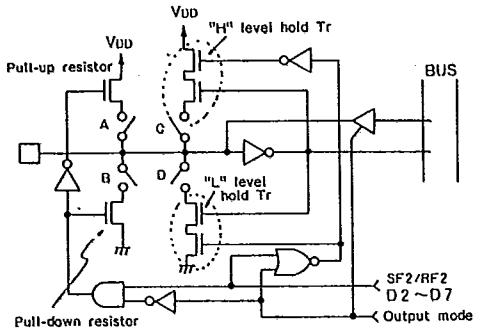
Option	Circuit format	Remarks
RC & X'tal		- Cycle time: f1 cycle x 4 - Output from the divider circuit (φ1 to φ15) is used as the timer base clocks, LCD driver waveform generation signals, and S/K port clock for chattering rectification. - The OSC1 oscillation circuit is forced into stop state with the SLOW instruction.
CF & X'tal • 400kHz (CF) to • 4 MHz (CF)		- Cycle time: f1 cycle x 4n (n: 2) - Output from the divider circuit (φ1 to φ15) is used as the timer base clocks, LCD driver waveform generation signals, and S/K port clock for chattering rectification. - The OSC1 oscillation circuit is forced into stop state with the SLOW instruction.
RC		- Cycle time: f1 cycle x 4 - Output from the divider circuit (φ1 to φ15) is used as the LCD driver waveform generation signals, and S/K port clock for chattering rectification.

Option	Circuit format	Remarks
CF • 400kHz to • 4 MHz		- Cycle time: f1 cycle x 4n (n: 2) - Output from the divider circuit (ϕ1 to ϕ15) is used as the LCD driver waveform generation signals, and S/K port clock for chattering rectification.
X'tal		- Cycle time: f2 cycle x 4 - Output from the divider circuit (ϕ1 to ϕ15) is used as the time base clocks, LCD driver waveform generation signals, and S/K port clock for chattering rectification.
External clock source		- Cycle time: f1 cycle x 4n (n: 2) - Output from the divider circuit (ϕ1 to ϕ15) is used as the LCD driver waveform generation signals, and S/K port clock for eliminating chatterings

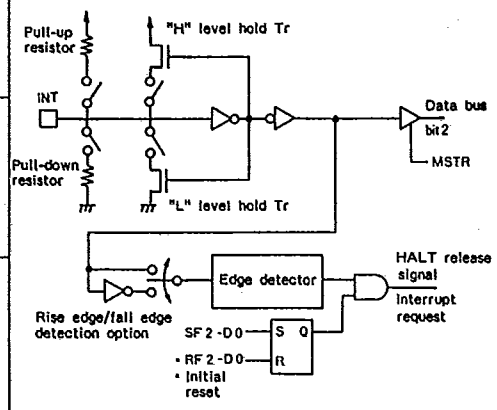
Crystal oscillation options

Option	Circuit format	Remarks
32 kHz		32 kHz oscillation option with the internal Rd (200 kΩ typ.).
65 kHz or 38 kHz		

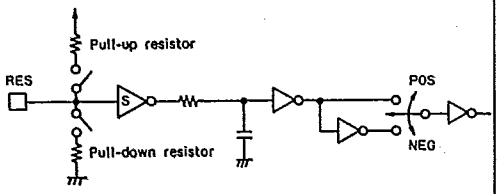
Input port options

Option	Circuit format	Remarks
Internal pull-up/pull-down resistor selection		The optional internal resistors for the following ports can be switched at the same time by the SF2 or RF2 instruction. - S1 to 4, K1 to 4, M1 to 4, P1 to 4, SO1 to 4, A1 to 4 Reset status. Resistance is weak as long as the reset signal is active. After the reset signal becomes inactive, the resistance becomes strong. Option. One of the two options, A and B, must be selected.
"L" or "H" level hold Tr selection	 • Combination examples Combination type / 1 / 2 / 3 / 4 Pull-up resistor (A): ON ON Pull-down resistor (B): ON ON "H" level hold Tr (C): ON "L" level hold Tr (D): ON	When use of the hold Tr is selected: - This option can be selected for reducing the current dissipation by pull-ups or pull-downs. For example, this option should be selected when a push switch and a slide switch are to be used for the S1 and S2 pins, respectively. - When input open specification is employed, make resistance weak first and then read in input level. After this, make the resistance strong. In this case, the "H" or "L" level hold Tr becomes energized to keep the input level if the input level is within floating range. When nonuse of the hold Tr is selected: - Use the input terminal Tr with pull-up or pull-down resistor ON. - Do not use the "H" level or "L" level hold Tr when terminal is connected with external control signal line. That is, no Tr should be used when the input data level is not within floating range.

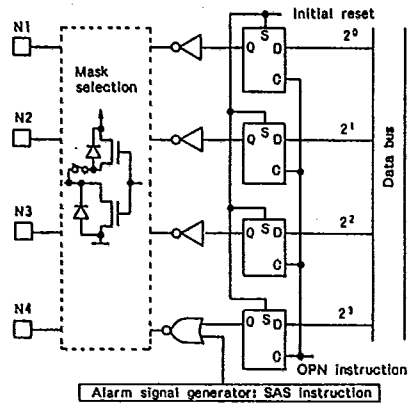
INT terminal

Option	Circuit format	Remarks
Internal resistor selection: pull-up, pull-down and resistor open.		Internal resistor selection - Pull-up resistor adoption - Pull-down resistor adoption - Resistors left open
"H" level/"L" level hold Tr selection		Input signal level hold Tr selection - "H" level hold Tr adoption - "L" level hold Tr adoption - No level hold Tr adoption
Detection rise edge/fall edge option		Detection signal edge selection - Rise edge detection - Fall edge detection

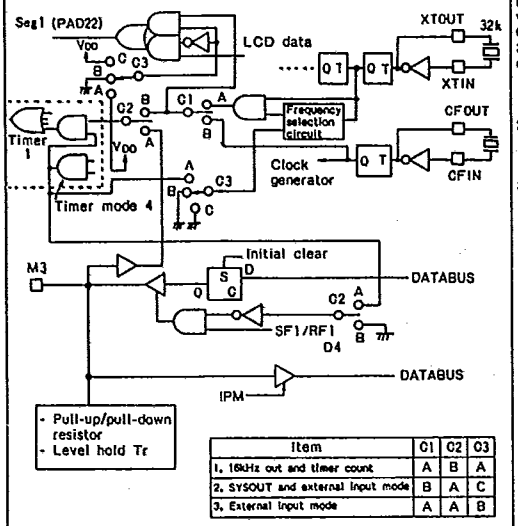
RES terminal

Option	Circuit format	Remarks
Internal resistor selection: Pull-up, pull-down and resistor open. Terminal level selection		Internal resistor selection and terminal polarity selection - Pull-up resistor and "L" level reset signal - Pull-down resistor and "H" level reset signal - Open resistor and "L" level reset signal - Open resistor and "H" level reset signal

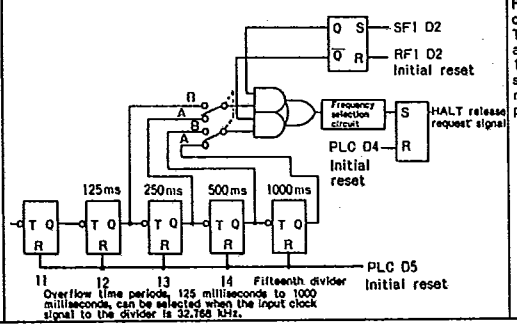
Output terminals N1 to N4

Option	Circuit format	Remarks
N-ch open/CMOS output format selection		- N-ch open drain/CMOS output format selection - Output format can be selected for each terminal by mask option.

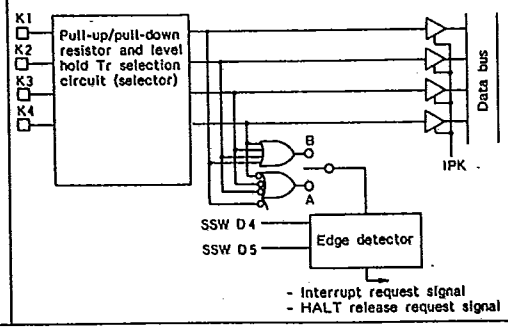
Timer 1 mode

Option	Circuit format	Remarks
1. 16kHz OUT 2. SYS OUT 3. Timer 1 EXTIN	 Item / C1 / C2 / C3 1. 16kHz out and timer count: A B A 2. SYSOUT and external input mode: B A C 3. External input mode: A A B	Mode 3 (external input mode) of timer 1 is provided with the following three options. One of the three options can be selected for mode 3 (external input mode) of timer 1. If no optional data is selected, option 3 will be assumed. 1. Output from the first divider is input to the timer and then counted. This output is also sent to SEG 1 (PAD22). 2. Clock pulses are sent to timer via the M3 terminal and then counted. In this mode, the CF oscillation signal frequency is divided by 2 and sent to SEG 1 (PAD22). 3. This is a normal mode allowing clock pulses to be input to the timer through the M3 terminal and then counted.

Overflow time selection for the 15-level divider

Option	Circuit format	Remarks
1. 1000ms/250ms 2. 500ms/125ms		Fifteen-level divider circuit is provided for counting basic clock input (32.768 kHz signal). This divider has the following mask options allowing the user to select overflow time periods: 1000 or 500 milliseconds, and 250 or 125 milliseconds. 1000 or 250 milliseconds, or 500 or 125 milliseconds can be selected in your application program.

Mask options for input port K

Option	Circuit format	Remarks
Pull-up/pull-down resistor selection		Pull-up/pull-down resistor selection is automatically accompanied by the input detection selector gate switching. That is, either mask option A or B in the figure is selected at the same time when pull-up or pull-down resistor is selected. A (pull-up resistor specification): The edge detector receives a signal from the input detection gate when all the inputs (K1 to K4) were H and any one of them changes to L. The edge detector does not work when any one of the inputs was already L and a certain terminal input level changes to H or L. B (pull-down resistor specification): Logic levels of item A are reversed.

A list of mask options

1) Port internal resistor selection (Ports: S, K, P, M, A and SO)
   - Pull-up resistor specification: LC5893U EVA chip
   - Pull-down resistor specification: LC5893D EVA chip
2) "H" level or "L" level hold Tr selection for port S
   - Level hold Tr selection
   - Level hold Tr non-selection
3) "H" level or "L" level hold Tr selection for port K
   - Level hold Tr selection
   - Level hold Tr non-selection
4) "H" level or "L" level hold Tr selection for port M
   - Level hold Tr selection
   - Level hold Tr non-selection
5) "H" level or "L" level hold Tr selection for port P
   - Level hold Tr selection
   - Level hold Tr non-selection
6) "H" level or "L" level hold Tr selection for port A
   - Level hold Tr selection
   - Level hold Tr non-selection
7) "H" level or "L" level hold Tr selection for port SO
   - Level hold Tr selection
   - Level hold Tr non-selection
8) Internal resistor selection for the INT terminal and signal edge selection
   - Pull-up resistor (NEGATIVE)
   - Pull-down resistor (POSITIVE)
   - Open (NEGATIVE)
   - Open (POSITIVE)
9) Level hold Tr selection for terminal INT
   - "L" or "H" level hold Tr selection
   - "L" or "H" level hold Tr non-selection
10) RES terminal
   - Pull-up resistor ("L" level reset)
   - Pull-down resistor ("H" level reset)
   - Open ("L" level reset)
   - Open ("H" level reset)
11) N1 terminal
   - N-ch open-drain output format
   - CMOS output format
12) N2 terminal
   - N-ch open-drain output format
   - CMOS output format
13) N3 terminal
   - N-ch open-drain output format
   - CMOS output format
14) N4 terminal
   - N-ch open-drain output format
   - CMOS output format
15) OSC specification
   - CF only
   - RC only
   - X'tal only
   - EXT only
   - CF + X'tal
   - RC + X'tal
   - EXT + X'tal

16) CF/EXT
- 400 kHz or 800 kHz
- 1 MHz to 4 MHz

17) X'tal
- 32 kHz
- 65 kHz
- 38 kHz

18) LCD port
- "L" level <- STOP and RES
- "H" level <- RES. "L" level <- STOP
- HOLD mode <- STOP. "L" level <- RES
- HOLD mode <- STOP. "H" level <- RES

19) 15-level counter overflow time period
- $\phi_0/2048$ or $\phi_0/8192$
- $\phi_0/4096$ or $\phi_0/16384$

20) Serial I/O internal clock cycle
- Cycle time x 1 x 2
- Cycle time x 2 x 2
- Cycle time x 4 x 2

21) LCD driver
- STATIC
- 1/2 bias-1/2 duty lighting format
- 1/2 bias-1/3 duty lighting format
- 1/2 bias-1/4 duty lighting format
- 1/3 bias-1/3 duty lighting format
- 1/3 bias-1/4 duty lighting format

22) LCD alternating frequency
- SLOW
- TYP
- FAST

23) Timer 1 mode 3 selection
- $\phi 1$ OUT
- Cycle time x 1/4 and EXTIN
- EXTIN
- NONUSE

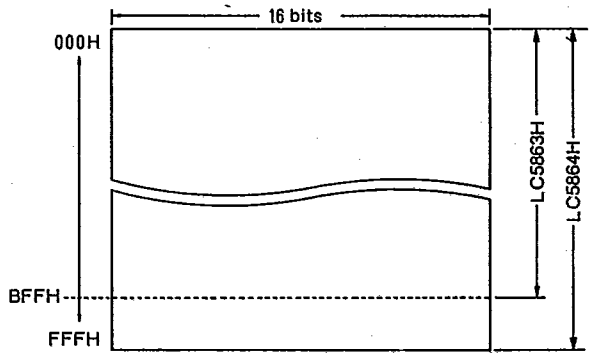
24) Internal reset circuit
- Selection
- Disabled

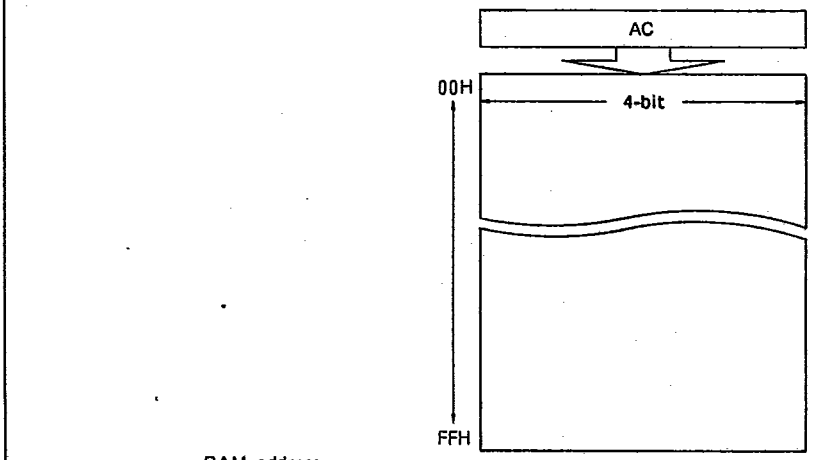
25) LCD port status at the reset
- All segments ON and CMOS terminal level "H"
- All segments OFF and CMOS terminal level "L"

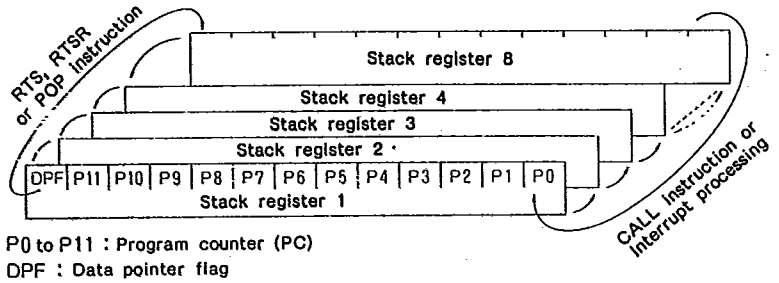
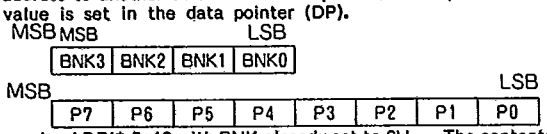
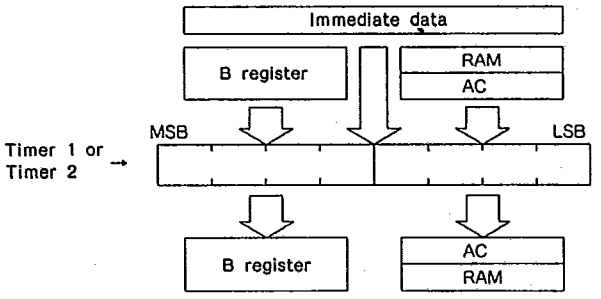
Description of internal register functions

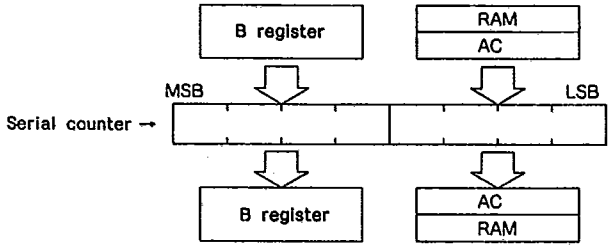
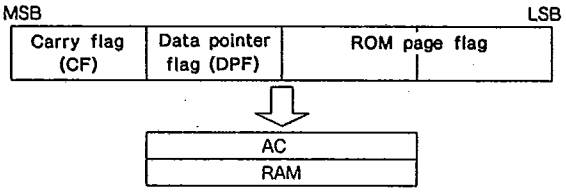
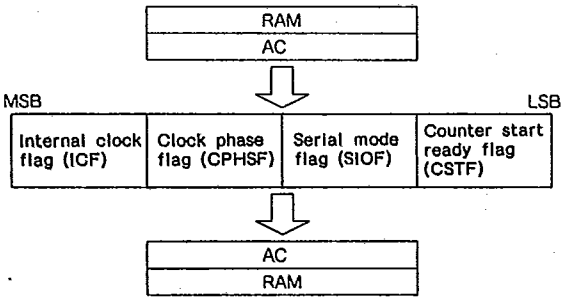
<table>
<tr><th>Symbol</th><th>R/W</th><th>Functional description</th><th>Initial reset value</th></tr>
<tr><td>PC</td><td>—</td><td>Program counter (PC)
The program counter (PC) is a 12-bit counter and used to point to the address in the program memory (ROM), which stores the next instruction to be executed.
Normally, the PC content is incremented by 1 from 000H to FFFH. When such special operations as branching operation, subroutine processing, interrupt processing and initial reset operation are carried out, the data corresponding to them are set in the program counter (PC).

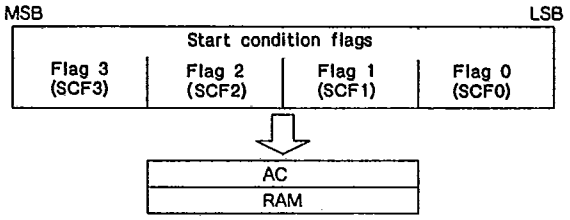
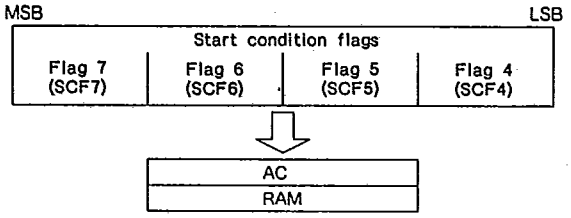
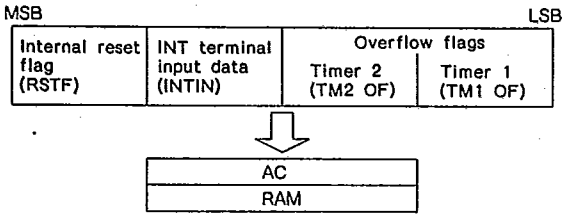
The data corresponding to the special operations are as follows:
<table>
<tr><th>Operation \ PC</th><th>PC11</th><th>PC10</th><th>PC9</th><th>PC8</th><th>PC7</th><th>PC6</th><th>PC5</th><th>PC4</th><th>PC3</th><th>PC2</th><th>PC1</th><th>PC0</th></tr>
<tr><td>Initial reset</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td rowspan="4">Interrupt</td><td>External interrupt from the INT terminal</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>External interrupt from the S/R terminal</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Internal interrupt from timer 1 or timer 2</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Internal interrupt from serial counter. External interrupt from the SO4 terminal.</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Unconditional jump (JMP instruction)</td><td>Page</td><td>P10</td><td>P9</td><td>P8</td><td>P7</td><td>P6</td><td>P5</td><td>P4</td><td>P3</td><td>P2</td><td>P1</td><td>P0</td></tr>
<tr><td>Conditional jump (BAB0, BAB1 BAB2, BAB3 BAZ, BANZ BCH, BCNH)</td><td>Page</td><td>P10</td><td>P9</td><td>P8</td><td>P7</td><td>P6</td><td>P5</td><td>P4</td><td>P3</td><td>P2</td><td>P1</td><td>P0</td></tr>
<tr><td>Call instruction (CALL)</td><td>Page</td><td>P10</td><td>P9</td><td>P8</td><td>P7</td><td>P6</td><td>P5</td><td>P4</td><td>P3</td><td>P2</td><td>P1</td><td>P0</td></tr>
<tr><td>Return instruction (RTS RTSR)</td><td colspan="12">Call address + 1</td></tr>
</table>
Page: ROM page flag contents. One page consists of 2048 addresses. --- The ROM page flag contents can be set by the MROPF or SROPF instruction.
P_0 to P_{10}: Immediate data given by each instruction</td><td></td></tr>
<tr><td>ROM</td><td>R/O</td><td>Program memory (ROM)
The program memory (ROM) is a read only memory with a capacity of 4K words (8K bytes; 4096 x 16 bits). It stores user programs to be executed.(LC5863H: 3072 x 16 bits)

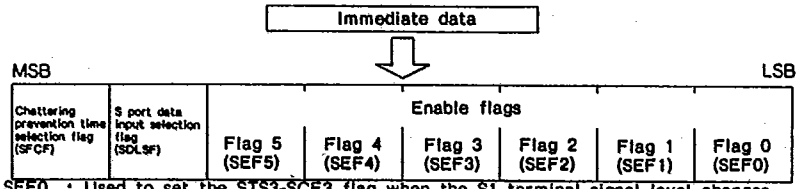
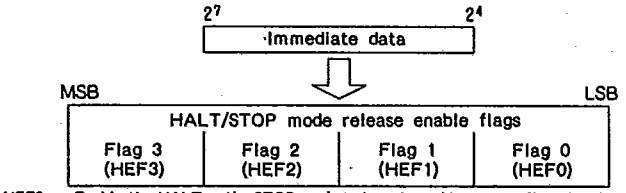
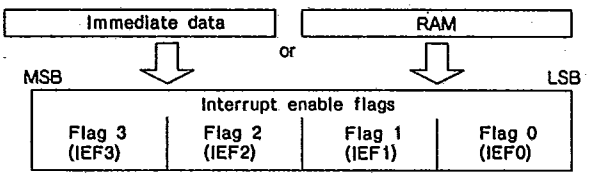
 
</td><td></td></tr>
<tr><td>RAM</td><td>R/W</td><td>Data memory (RAM)
The data memory (RAM) is a static RAM with a capacity of 1K bits (256 x 4 bits).
The addresses in the data memory (RAM) can be accessed in the following 4 addressing modes:
- Direct addressing mode --- Immediate data used to make an access to any address in the RAM area between 00H and FFH.
- Indirect addressing mode --- 8-bit data pointer (DPL and DPH) used to make an access to any address in the RAM area between 00H and FFH.
- Indirect addressing mode --- 4-bit RAM bank register x 10H + immediate data (0H to 0FH)
- Indirect addressing mode --- 4-bit RAM bank register x 10H +8H + immediate data (0H to 7H)
Note that data input to a desired RAM address is carried out via the accumulator (AC) automatically.</td><td>Undefined</td></tr>
</table>

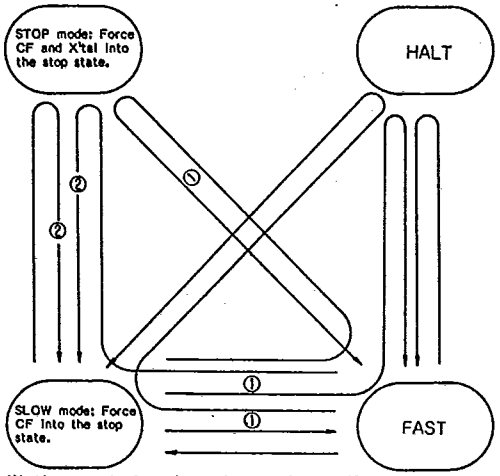
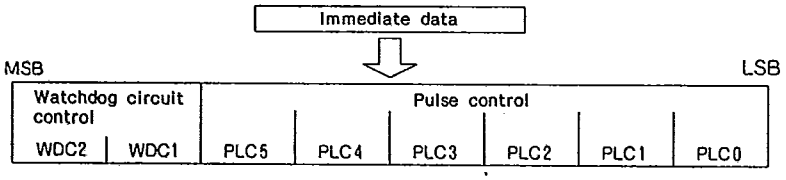
Symbol	R/W	Functional description	Initial reset value
RAM	R/W	 RAM address A) P7 P6 P5 P4 P3 P2 P1 P0 : B) DPH DPL : Condition: The data pointer flag must be set in advance. C) RAM bank register P3 P2 P1 P0 : Condition: When the instructions like the ADDI instruction are to be used. D) RAM bank register 1 W2 W1 W0 : Condition: When the instructions such as the MRW W,P and MWR P,W are to be used. Note: Direct addressing mode by immediate data is given priority over indirect addressing mode by the data pointer if RAM bank register (BNK) content is equal to the DPH value given by an instruction. This is detailed in the following two examples. Example: The contents of the S port will be written into address 10H in the data memory (RAM) if the IPS 10H instruction is executed in the following conditions: Condition 1: Data pointer flag (DPF) -> Already set. Condition 2: DPH = 5H and DPL = 3H. RAM bank register (BNK) = 1H Example: The contents of the S port will be written into address 53H in the data memory (RAM) if the IPS 10H instruction is executed in the following conditions: Condition 1: Data pointer flag (DPF) -> Already set. Condition 2: DPH = 5H and DPL = 3H. RAM bank register (BNK) = 4H In the second example, the BNK contents and DPH contents are not the same.	Undefined
AC	R/W	Accumulator (AC) MSB LSB AC3 AC2 AC1 AC0	Undefined
B	R/W	B register MSB LSB B3 B2 B1 B0 The B register is used with a RAM address to write or read data to/from timer 1, timer 2, data pointer (DP) and LCD port.	Undefined
DP	R/W	Data pointer (DP) MSB LSB DP7 DP6 DP5 DP4 DP3 DP2 DP1 DP0 DPH DPL The data pointer (DP) can be used to allow the user to make an access to the RAM address area with the data pointer flag (DPF) already set.	Undefined

Symbol	R/W	Functional description	Initial reset value
STACK	R/W	Stack pointer (STACK) The stack pointer (STACK) consists of 8 x 13-bit registers. It allows the user to use 8-level nesting. The stack pointer (STACK) is incremented when the CALL instruction is executed and when interrupt processing is carried out. It is decremented when the RST, RTSR or POP instruction is executed.  P0 to P11 : Program counter (PC) DPF : Data pointer flag	01H
BNK	R/W	Bank register (BNK) The bank register (BNK) is a 4-bit register. It is used to divide the RAM area (00H to FFH) into 16 bank areas. The bank register (BNK) is used when data is moved from one address to another in the RAM area, immediate operation is carried out and a desired value is set in the data pointer (DP).  Example: ADDI* 5, 10 with BNK already set to 6H --- The contents at address 65H in the RAM and 10H are added together in binary and the binary sum is then stored into the accumulator (AC) and address 65H.	00H
APG	R/W	RAM page flag The RAM page flag consists of two bits. This flag is used to allow the user to adopt the RAM with a capacity of up to 4K bits (1024 x 4 bits). Note: Please set the RAM page flag to 0H on the LC5864H.	00H
TIM TIM1 TIM2	R/W	Timer counter The timer counter is an 8-bit down counter. Four-bit data can be exchanged between the lower four bits of the timer counter and an address in the data memory (RAM). Four-bit data can be exchanged between the upper four bits of the timer counter and the B register. 	Undefined

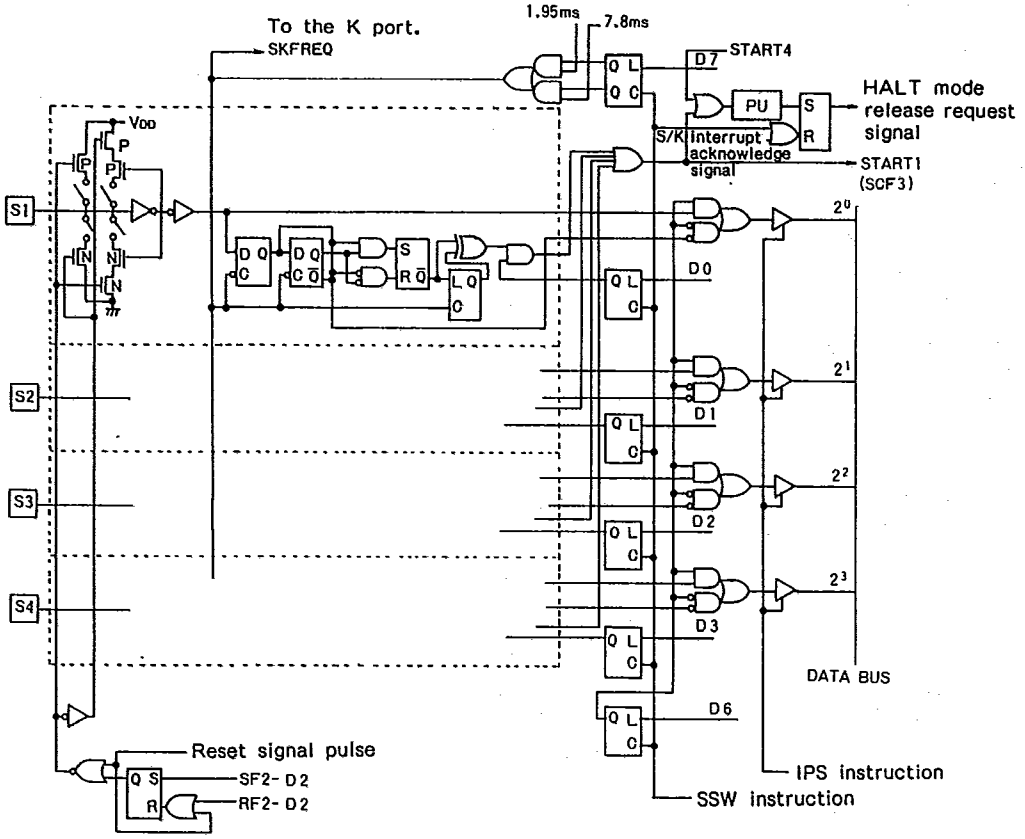
Symbol	R/W	Functional description	Initial reset value
SIO	R/W	Serial counter The serial counter is an 8-bit shift register. Four-bit data is exchanged between the lower 4 bits of the serial counter and an address in the data memory (RAM). Four-bit data is exchanged between the upper 4 bits of the serial counter and the B register. 	Undefined
OPG	R/W	ROM page flag The ROM page flag consists of two bits. This flag is used to allow the user to adopt the ROM with a capacity of up to 16K bytes (8192 x 16 bits). Each page area is 4K bytes in size (2048 x 16 bits). Note: The size of the ROM mounted on the LC5864H microcomputer is 8K bytes (4K x 16 bits). Therefore, the bit 1 of the ROM page flag must be set to "0".	00H
STS1	R/O	Status register 1 (STS1) Status register 1 (STS1) consists of 4 bits. Each bit has the following meaning: 	00H
STS2	R/W	Status register 2 (STS2) Status register 2 (STS2) is a 4-bit register used to control the serial counter and monitor the operational status.  ICF : Set to "H" when internal clock mode is selected. CPHSF : Set to "H" when data is output on the rising edge of a selected clock and data is input on the falling edge. SIOF : Set to "H" when the serial I/O mode is selected. CSTF : Set this flat to "H" to start the SIO counter operation. (please refer to the SSCF or MRSC instruction.) "L" level flag status: SIO counter now in operation (Please refer to the MSCF instruction.)	00H

Symbol	R/W	Functional description	Initial reset value
STS3	R/O	Status register 3 (STS3) Status register 3 (STS3) is a 3-bit register used to confirm the arrival of the HALT and STOP operation mode release request signals.  SCF0 : Set if the INT terminal signal level changes. SCF1 : Set if the K port signal level changes. SCF2 : Set if any one of the STS4 flags is set. SCF3 : Set if the S port signal level changes. Note: The SCF0 flag can be set only when the SF2-1 instruction has been already used to enable the INT terminal HALT release request signal. Flags SCF1 and SCF3 can be set only when the SSW instruction has been already used to enable the mode release signals from the S and K ports.	00H
STS4	R/O	Status register 4 (STS4) Status register 4 (STS4) is a 4-bit register used to confirm the arrival of the HALT and STOP operation mode release request signals.  SCF4 : Set by an overflow signal from the divider STS5 : Set by an underflow signal from timer 1 SCF6 : Set by an underflow signal from timer 2 SCF7 : Set by an overflow signal from the serial counter or when the SO4 terminal signal level changes.	00H
STS5	R/O	Status register 5 (STS5) Status register 5 (STS5) is a 4-bit register. Each bit has the following meaning.  TM1 OF/TM2 OF: Interrupt overflow flag INTIN : INT terminal input data RSTF : Internal reset flag set at the power on. The internal reset flag (RSTF) can be set by a steep signal change at the power-on reset.	00H

Symbol	R/W	Functional description	Initial reset value
CTL1	W/O	Control register 1 (CTL1) Control register 1 (CTL1) is an 8-bit register used to control the S and K ports.  SEF0 : Used to set the STS3-SCF3 flag when the S1 terminal signal level changes. SEF1 : Used to set the STS3-SCF3 flag when the S2 terminal signal level changes. SEF2 : Used to set the STS3-SCF3 flag when the S3 terminal signal level changes. SEF3 : Used to set the STS3-SCF3 flag when the S4 terminal signal level changes. SEF4 : Used to set the STS3-SCF1 flag when any one of the K port terminals changes its pole-property to "H" or "L". SEF5 : Used to set the STS3-SCF1 flag when all of the K port terminals enter the "L" or "H" level state. SDLSF : Used to enable the S port input data (S1 to S4 input signals) to be directly input to the accumulator (AC) and the data memory area (RAM). If set to "0", the logic signals from the second D-FF circuits are directly input to the accumulator (AC) and the data memory area (RAM). SFCF : Used to switch the chattering prevention time from 7 millisecons to 2 milliseconds.	00H
CTL2	W/O	Control register 2 (CTL2) Control register 2 (CTL2) is a 4-bit register used to enable the HALT and STOP operation mode release request signals. Each bit of control register 2 has the following meaning.  HEF0 : Enable the HALT or the STOP mode to be released by an overflow signal from the divider. HEF1 : Enable the HALT or the STOP mode to be released by an underflow signal from timer 1. HEF2 : Enable the HALT or the STOP mode to be released by an underflow signal from timer 2. HEF3 : Enable the HALT or the STOP mode to be released by an overflow signal from the serial counter or by a signal level change at the SO4 terminal.	00H
CTL3	W/O	Control register 3 (CTL3) Control register 3 (CTL3) is a 4-bit register used to enable interrupt signal. Each bit of control register 3 has the following meaning:  IEF0 : Enable signal rise edge or signal fall edge at the INT terminal to cause interrupt request. IEF1 : Enable signal level change at the S or K port to cause interrupt request. IEF2 : Enable an underflow signal from timer 1/timer 2 to cause interrupt request. IEF3 : Enable an overflow signal from the serial counter or a signal level change at the SO4 terminal to cause interrupt request.	00H

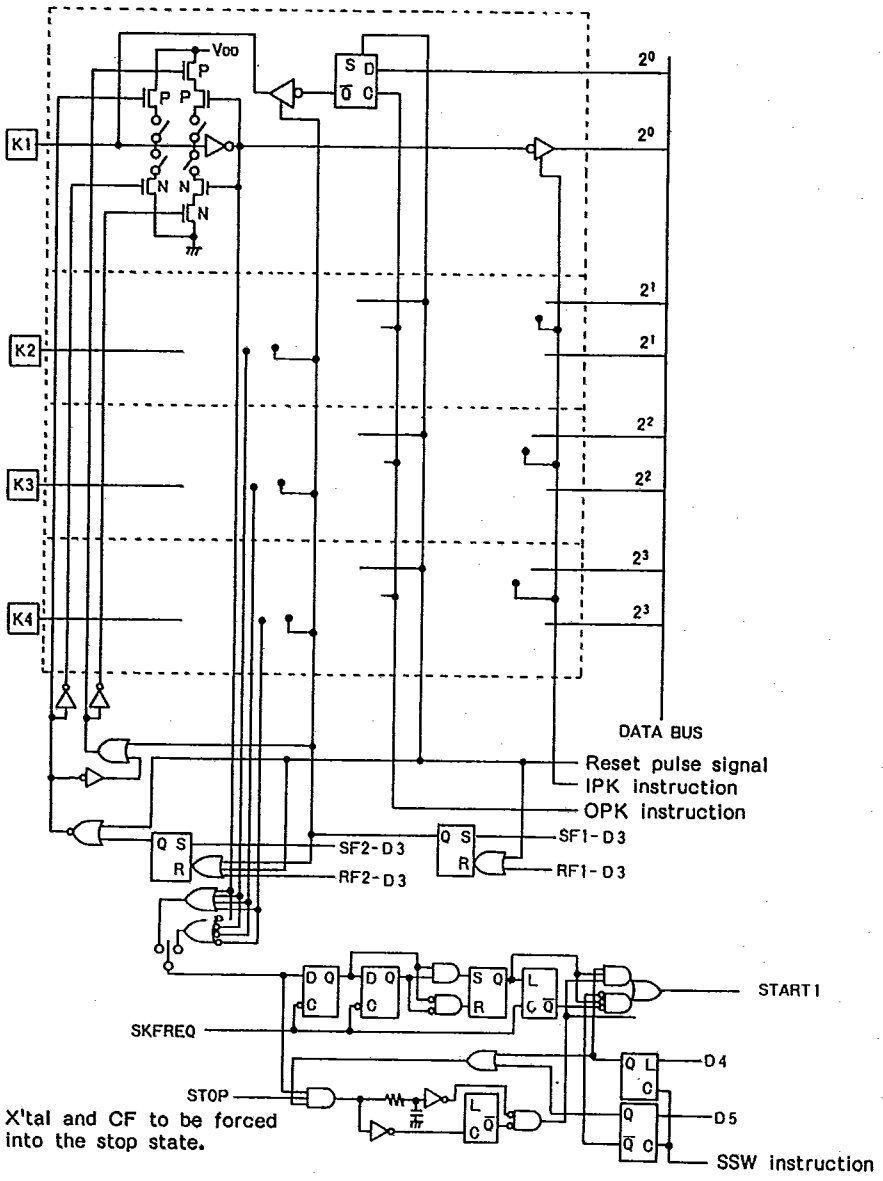
Symbol	R/W	Functional description	Initial reset value
SC	W/O	System clock control  1. When CF oscillation mode is selected, the CF oscillation stabilization period should be kept in mind in changing the current operation mode from the STOP/SLOW to the FAST. 2. When the X'tal oscillation mode is selected, the oscillation stabilization time period should be considered.	
PLC	W/O	Pulse control The pulse control is used to initialize the status register and divider. In addition, it is used to start up the watchdog circuit.  PLC0 : Reset the SCF0 flag bit. PLC1 : Reset the SCF5 flag bit. PLC2 : Reset the SCF6 flag bit. PLC3 : Reset the SCF7 flag bit. PLC4 : Reset the SCF4 flag bit. PLC5 : Reset the last 5 FFs (11 to 15) of the divider circuit. WDC1 : Send clock pulses to the WDC1. WDC2 : Send clock pulses to the WDC2. Note that the system will be initialized a certain period later if clock pulses are not sent to the WDC1 and WDC2 sequentially.	

Input structure of the "S" port

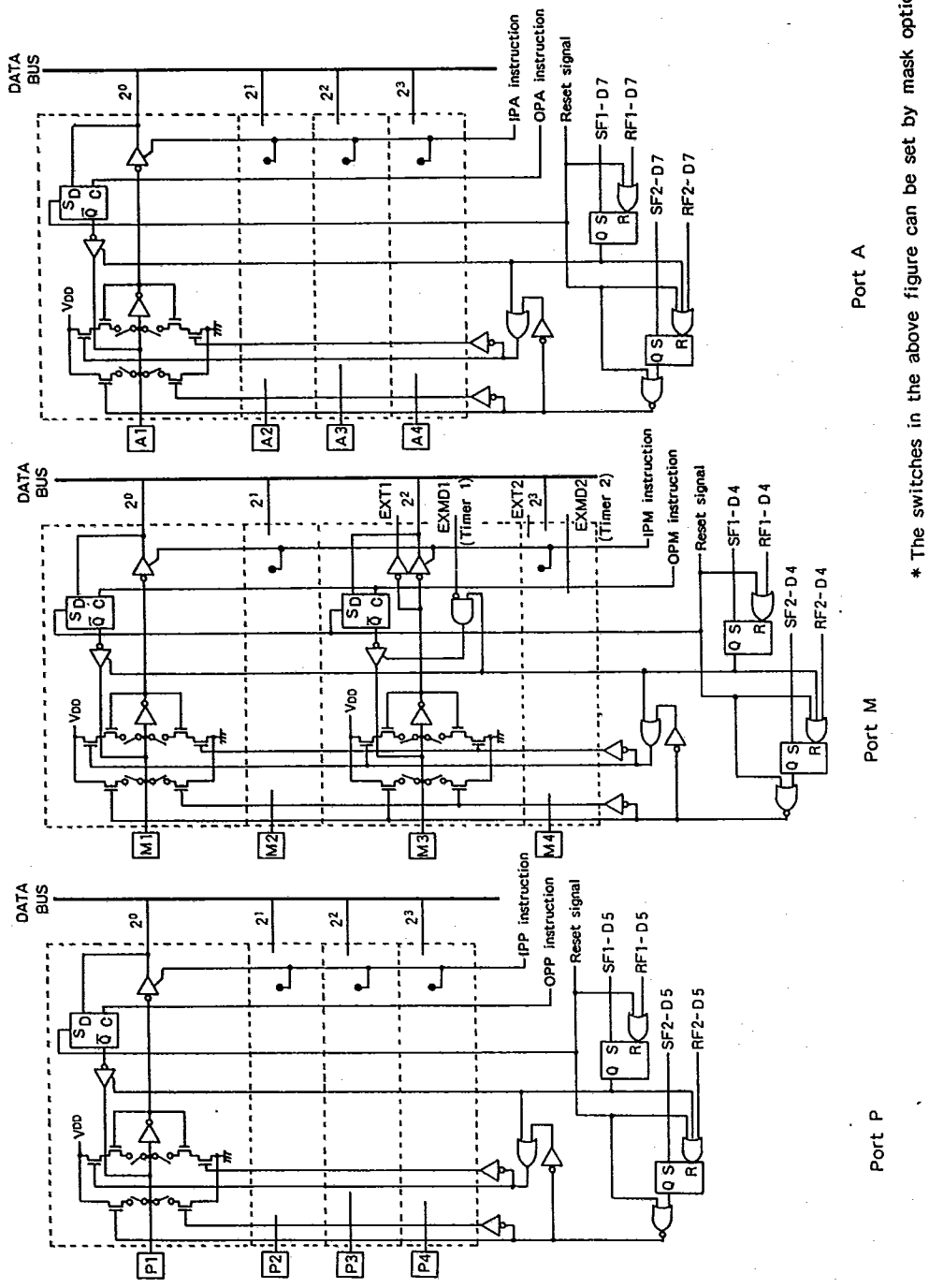


* The switches in the above figure can be set by mask option.

Input/output structure of the "K" port



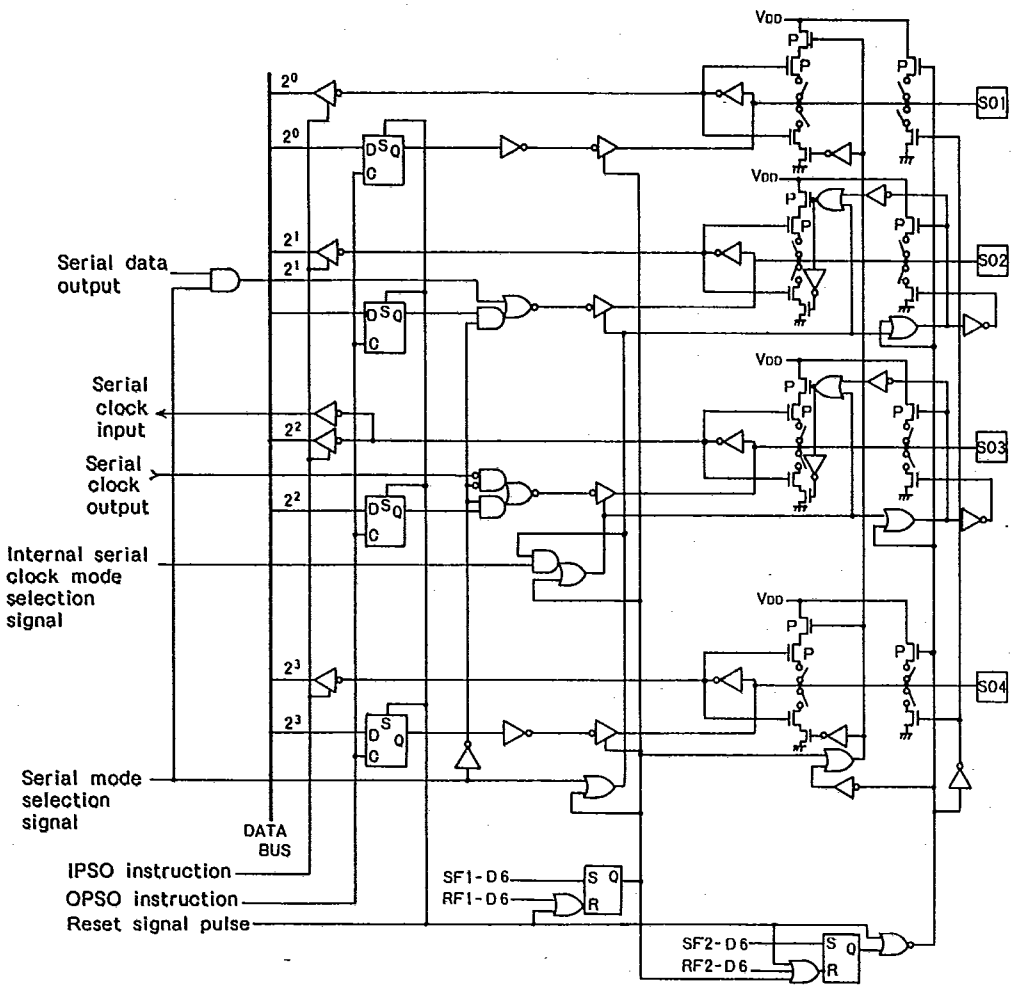
* The switches in the above figure can be set by mask option.



Input/output structure of the "P", "M" and "A" ports

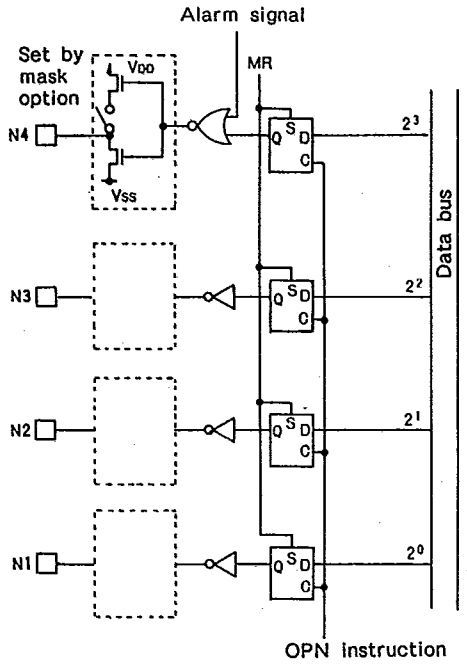
* The switches in the above figure can be set by mask option.

Input/output structure of the SO port



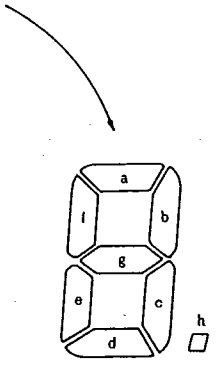
*The switches in the above figure can be set by mask option.

Output structure of the N port



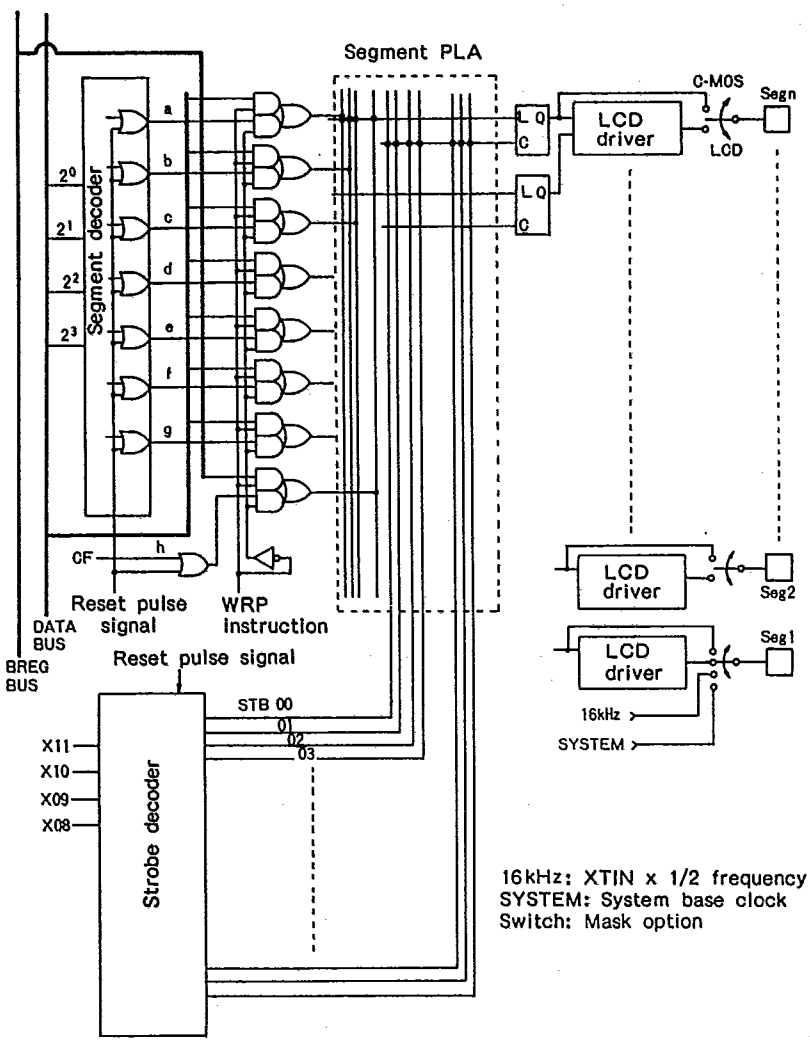
Segment decoder instructions

Instruction	Data	Related block	a	b	c	d	e	f	g	h
WRT	0	RAM	1	1	1	1	1	1	0	CF
	1		0	1	1	0	0	0	0	
	2		1	1	0	1	1	0	1	
	3		1	1	1	1	0	0	1	
	4		0	1	1	0	0	1	1	
	5		1	0	1	1	0	1	1	
	6		1	0	1	1	1	1	1	
	7		1	1	1	0	0	0	0	
	8		1	1	1	1	1	1	1	
	9		1	1	1	1	0	1	1	
	10		1	0	0	1	1	1	1	
	11		1	0	0	1	1	1	1	
	12		0	0	0	0	0	0	1	
	13		0	0	0	0	0	0	1	
	14		0	0	0	0	0	0	0	
WRT	15	RAM	0	0	0	0	0	0	0	CF
WRP	00~FF	RAM,Breg	RAM 2^0	RAM 2^1	RAM 2^2	RAM 2^3	Breg 2^0	Breg 2^1	Breg 2^2	Breg 2^3



CF --- Carry flag

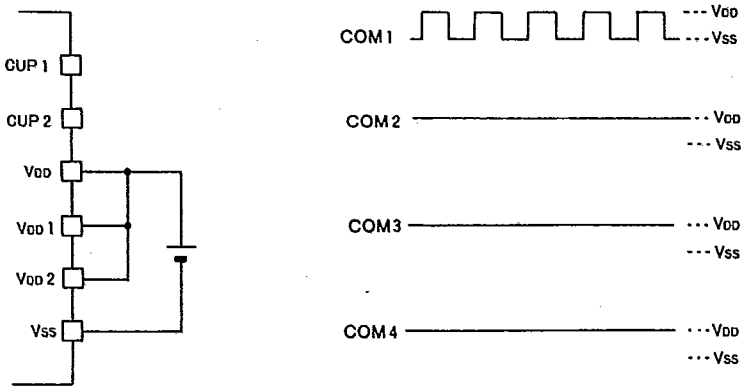
LCD panel driving block structure and software



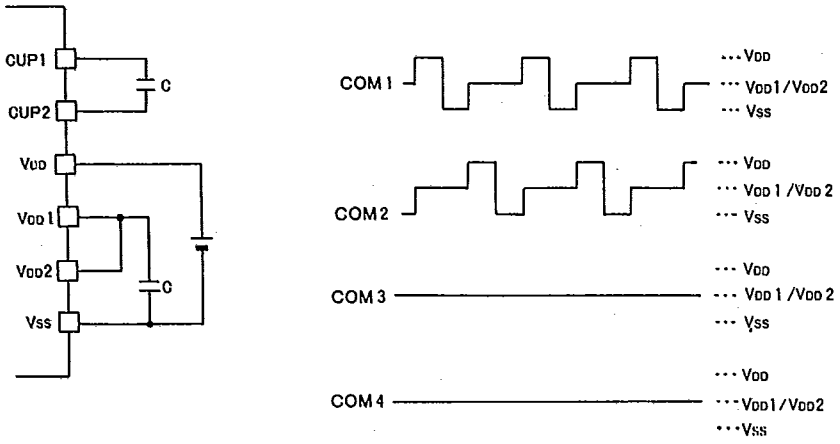
16kHz: XTIN x 1/2 frequency signal
SYSTEM: System base clock
Switch: Mask option

Bias waveforms

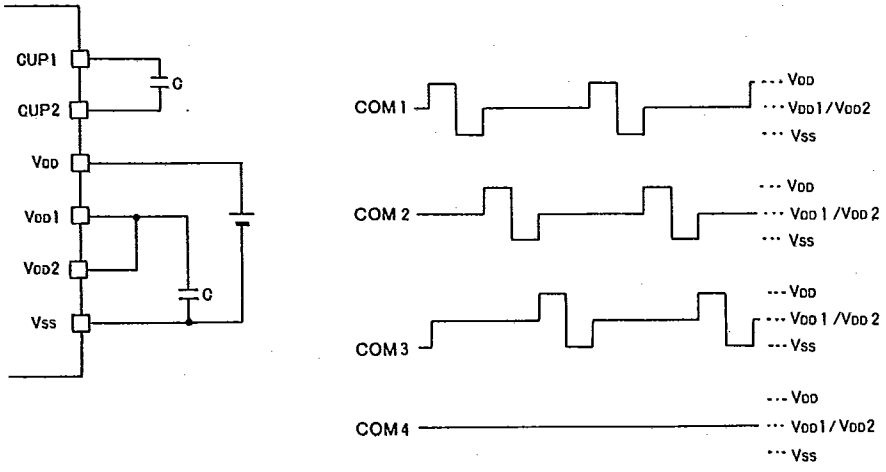
ⓐ Static



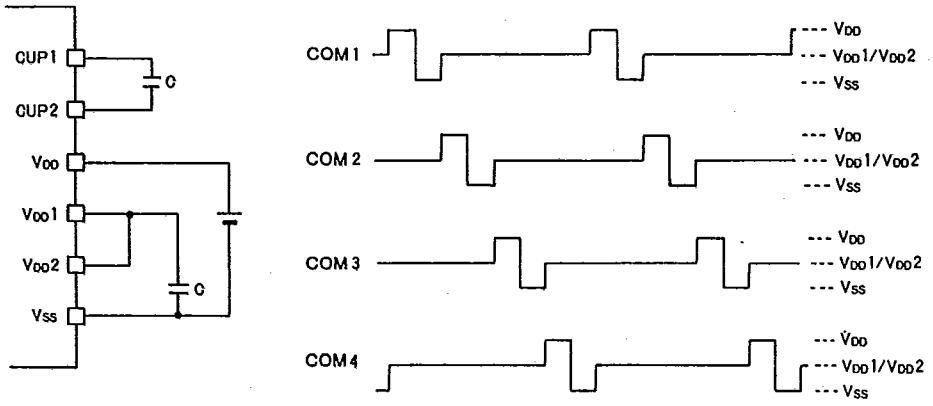
ⓑ ½Bias-½Duty



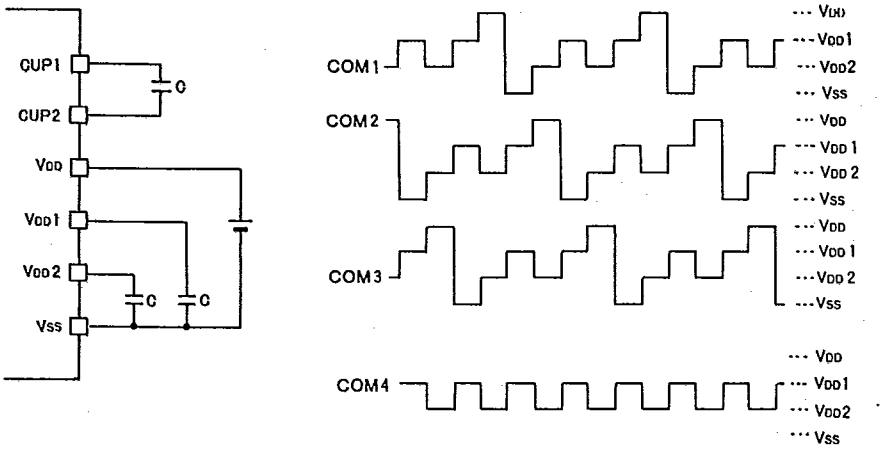
ⓒ ½Bias-⅓Duty



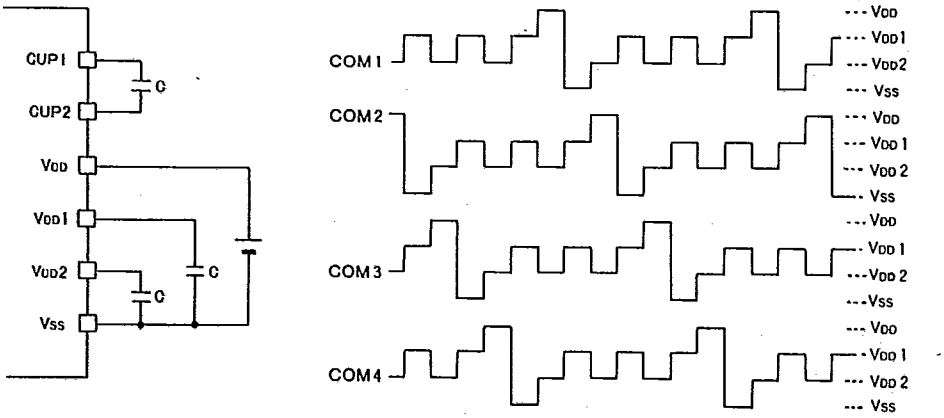
ⓓ½Bias-¼Duty



ⓔ⅓Bias-⅓Duty



ⓕ⅓Bias-¼Duty



Absolute maximum ratings/V_{SS}=0V, Ta=25℃

Item	Symbol	Conditions/terminals	min	typ	max	unit
Maximum supply voltage	V_{DD}		−0.3		+7.0	V
	$V_{DD}1$		−0.3		V_{DD}	V
	$V_{DD}2$		−0.3		V_{DD}	V
Maximum input voltage	$V_I(1)$	Depend on the fixed circuit formats shown in Figures 1-1 and 1-2 XTIN,CFIN	Determined by the circuits.			
	$V_I(2)$	S1−4, K1−4, P1−4, M1−4, SO1−4, A1−4, RES INT, TST Condition: ports K, P, M, SO and A are used in the input mode.	−0.3		V_{DD} +0.3	V
Maximum output voltage	$V_O(1)$	Depend on the fixed circuit formats shown in Figure 1-1 and 1-2. XTOUT,CFOUT	Determined by the circuits.			
	$V_O(2)$	K1−4, P1−4, M1−4, SO1−4 A1−4, N1−4, CUP1, CUP2, Segment, COM1−3 Condition: ports K, P, M, SO and A are used in the output mode.	−0.3		V_{DD} +0.3	V
	$V_O(3)$	Open drain output specification N1−4 (Nch)	−0.3		+16	V
Output pin current	$I_O(1)$	Output current per pin N1−4	0		+15	mA
	$I_O(2)$	Output current per pin N1−4	−10		0	mA
	$I_O(3)$	Output current per pin K1−4, P1−4, M1−4,	0		5	mA
	$I_O(4)$	Output current per pin SO1−4, A1−4	−5		0	mA
	$\Sigma I_O(1)$	Pin total output current K1−4, P1−4, M1−4, SO1−4, A1−4, N1−4,			70	mA
	$\Sigma I_O(2)$	Pin total output current Segment	−70			mA
Allowable power dissipation	Pd(max)	FLP-80 flat package			500	mA
Operating ambient temperature	Topg		−30		+70	℃
Storage ambient temperature	Tstg		−55		+125	℃

Recommended operating range/V_{SS}=0V, Ta=-30 to +70℃

Item	Symbol	Conditions/terminals	min	typ	max	unit
Supply voltage	V_{DD}	No LCD lighting function : $V_{DD}1=V_{DD}2=V_{DD}$	2.0		6.0	V
		STATIC lighting format : $V_{DD}1=V_{DD}2=V_{DD}$	2.0		6.0	V
		1/2 bias lighting format : $V_{DD}1=V_{DD}2\fallingdotseq\frac{1}{2}V_{DD}$	2.8		6.0	V
		1/3 bias lighting format : $V_{DD}1\fallingdotseq 2*\frac{1}{3}V_{DD}$ $V_{DD}2\fallingdotseq\frac{1}{3}V_{DD}$	4.0		6.0	V
Hold voltage	V_{HD}	RAM and register contents hold voltage	2.0		V_{DD}	V
High level input voltage	$V_{IH}1$	S1−4, K1−4, P1−4, M1−4, (Note 1) SO1−4, A1−4 INT	0.7V_{DD}		V_{DD}	V
Low level input voltage	$V_{IL}1$	Condition: Ports K, P, M, SO and A are used in the input mode.	0		0.3V_{DD}	V
High level input voltage	$V_{IH}2$	RES pin	0.75V_{DD}		V_{DD}	V
Low level input voltage	$V_{IL}2$		0		0.25V_{DD}	V
High level input voltage	$V_{IH}3$	CFIN pin	0.75V_{DD}		V_{DD}	V
Low level input voltage	$V_{IL}3$		0		0.25V_{DD}	V
Operating frequency 1	fopg1	V_{DD}=2.0V~6.0V 32kHz XTIN/XTOUT	32		33	kHz
Operating frequency 2	fopg2	V_{DD}=2.2V~6.0V 38kHz crystal oscillation	37		39	kHz
Operating frequency 3	fopg3	V_{DD}=2.2V~6.0V 65kHz mode	60		70	kHz
Operating frequency 4	fopg4	V_{DD}=2.2V~6.0V	190		810	kHz
Operating frequency 5	fopg5	V_{DD}=2.8V~6.0V CFIN/CFOUT	190		1200	kHz
Operating frequency 6	fopg6	V_{DD}=3.0V~6.0V CF oscillation mode	190		2300	kHz
Operating frequency 7	fopg7	V_{DD}=4.5V~6.0V	190		4200	kHz
Operating frequency 8	fopg8	V_{DD}=4.0V~6.0V CFIN/CFOUT $RC^{\text{oscillation}}_{\text{mode}}$	100		1500	kHz
Operating frequency 9	fopg9	V_{DD}=2.0V~6.0V CFIN/CFOUT $EXT^{\text{oscillation}}_{\text{mode}}$	190		800	kHz
Operating frequency 10	fopg10	V_{DD}=3.0V~6.0V SO1/SO3 pin	DC		200	kHz
		At the serial mode. Rise time/fall time ≦ cycle time x 1/10				

Note 1: Both the CF resonator and Xtal oscillation circuits enter the stop state and thereby the entire circuit operation stops.

Electrical characteristics/V_{DD}=2.5 to 3.2V, V_{SS}=0V, Ta=-30 to +70°C

Item	Symbol	Conditions/terminals		min	typ	max	unit
Input resistance	R_{IN}1A	$V_{IN}=0.2V_{DD}$	"L" level hold Tr. Note 1. See Figure 2.	60	300	1200	kΩ
	R_{IN}1B	$V_{IN}=V_{DD}$	Pull-down resistor. Note 1. See Figure 2.	30	150	500	kΩ
	R_{IN}1C	$V_{IN}=0.8V_{DD}$	"H" level hold Tr. Note 1. See Figure 2.	60	300	1200	kΩ
	R_{IN}1D	$V_{IN}=V_{SS}$	Pull-up resistor. Note 1. See Figure 2.	30	150	500	kΩ
	R_{IN}2A	$V_{IN}=0.2V_{DD}$	INT "L" level hold Tr.	60	300	1200	kΩ
	R_{IN}2B	$V_{IN}=V_{DD}$	INT pull-down resistor	300	1500	5000	kΩ
	R_{IN}2C	$V_{IN}=0.8V_{DD}$	INT "H" level hold Tr.	60	300	1200	kΩ
	R_{IN}2D	$V_{IN}=V_{SS}$	INT pull-up resistor	300	1500	5000	kΩ
	R_{IN}3	$V_{IN}=V_{DD}$	RES pull-down resistor	10	30	50	kΩ
	R_{IN}4	$V_{IN}=V_{SS}$	RES pull-up resistor	10	30	50	kΩ
	R_{IN}5	$V_{IN}=V_{DD}$	TST pin pull-down resistor	60	250	1000	kΩ
	R_{IN}1A	$V_{IN}=0.2V_{DD}$	"L" level hold Tr. Note 1. See Figure 2.	80	300	1200	kΩ
	R_{IN}1B	$V_{IN}=V_{DD}$	Pull-down resistor. Note 1. See Figure 2.	40	150	500	kΩ
	R_{IN}1C	$V_{IN}=0.8V_{DD}$	"H" level hold Tr. Note 1. See Figure 2.	80	300	1200	kΩ
	R_{IN}1D	$V_{IN}=V_{SS}$	Pull-up resistor. Note 1. See Figure 2.	40	150	500	kΩ
	R_{IN}2A	$V_{IN}=0.2V_{DD}$	INT "L" level hold Tr.	80	300	1200	kΩ
	R_{IN}2B	$V_{IN}=V_{DD}$	INT pull-down resistor	400	1500	5000	kΩ
	R_{IN}2C	$V_{IN}=0.8V_{DD}$	INT "H" level hold Tr.	80	300	1200	kΩ
	R_{IN}2D	$V_{IN}=V_{SS}$	INT pull-up resistor	400	1500	5000	kΩ
	R_{IN}3	$V_{IN}=V_{DD}$	RES pull-down resistor	10	30	50	kΩ
	R_{IN}4	$V_{IN}=V_{SS}$	RES pull-up resistor	10	30	50	kΩ
	R_{IN}5	$V_{IN}=V_{DD}$	TST pin pull-down resistor	80	250	1000	kΩ
High level output voltage	V_{OH}(1)	$I_{OH}=-500\mu A$	N1−4	$V_{DD}-0.5$			V
Low level output voltage	V_{OL}(1)	$I_{OL}=1.0mA$				0.5	V
High level output voltage	V_{OH}(2)	$I_{OH}=-400\mu A$	K1−4, P1−4, M1−4, SO1−4, A1−4 (Condition: Ports K, P, M, SO and A are used in the output mode.)	$V_{DD}-0.5$			V
Low level output voltage	V_{OL}(2)	$I_{OD}=400\mu A$				0.5	V
Leakage current with output OFF	$\|I_{OFF}\|$	$V_{OH}=13.5V$	N1−4 (Open specification) Figure 10.			1.0	μA
Segment port output impedance							
●CMOS output port mode							
High level output voltage	V_{OH}(3)	$I_{OH}=-100\mu A$	Segment PAD №22~40, 43~58 FLP-80 pin №44~78	$V_{DD}-0.5$			V
Low level output voltage	V_{OL}(3)	$I_{OL}=100\mu A$				0.5	V
●P-ch open drain output port type (See Figure 11)							
High level output voltage	V_{OH}(3)	$I_{OH}=-100\mu A$	Segment PAD №22~40, 43~58 FLP-80 pin №44~78	$V_{DD}-0.5$			V
Leakage current with output OFF	$\|I_{OFF}\|$	$V_{OL}=V_{SS}$				1.0	μA
●N-ch open drain output port type (See Figure 11)							
High level output voltage	V_{OL}(3)	$I_{OL}=100\mu A$	Segment PAD №22~40, 43~58 FLP-80 pin №44~78			0.5	V
Leakage current with output OFF	$\|I_{OFF}\|$	$V_{OH}=V_{DD}$				1.0	μA
●Static lighting format							
High level output voltage	V_{OH}(4)	$I_{OH}=-20\mu A$	Segment PAD №22~40, 43~58 FLP-80 pin №44~78	$V_{DD}-0.2$			V
Low level output voltage	V_{OL}(4)	$I_{OL}=20\mu A$				0.2	V
High level output voltage	V_{OH}(5)	$I_{OH}=-100\mu A$	COM1	$V_{DD}-0.2$			V
Low level output voltage	V_{OL}(5)	$I_{OL}=100\mu A$				0.2	V

Note 1: 24 pins - S1 to S4, K1 to K4, P1 to P4, M1 to M4, SO1 to SO4 and A1 to A4.

Electrical characteristics/V_{DD}=3.0 to 4.5V, V_{SS}=0V, Ta=-30 to +70℃

Item	Symbol	Conditions/terminals		min	typ	max	unit
Input resistance	$R_{IN}1A$	$V_{IN}=0.2V_{DD}$	"L" level hold Tr. Note 1. See Figure 2.	35	200	800	kΩ
	$R_{IN}1B$	$V_{IN}=V_{DD}$	Pull-down resistor. Note 1. See Figure 2.	15	80	300	kΩ
	$R_{IN}1C$	$V_{IN}=0.8V_{DD}$	"H" level hold Tr. Note 1. See Figure 2.	35	200	800	kΩ
	$R_{IN}1D$	$V_{IN}=V_{SS}$	Pull-up resistor. Note 1. See Figure 2.	15	80	300	kΩ
	$R_{IN}2A$	$V_{IN}=0.2V_{DD}$	INT "L" level hold Tr.	35	200	800	kΩ
	$R_{IN}2B$	$V_{IN}=V_{DD}$	INT pull-down resistor	150	800	3000	kΩ
	$R_{IN}2C$	$V_{IN}=0.8V_{DD}$	INT "H" level hold Tr.	35	200	800	kΩ
	$R_{IN}2D$	$V_{IN}=V_{SS}$	INT pull-up resistor	150	800	3000	kΩ
	$R_{IN}3$	$V_{IN}=V_{DD}$	RES pull-down resistor	10	30	50	kΩ
	$R_{IN}4$	$V_{IN}=V_{SS}$	RES pull-up resistor	10	30	50	kΩ
	$R_{IN}5$	$V_{IN}=V_{DD}$	TST pin pull-down resistor	25	130	500	kΩ
	$R_{IN}1A$	$V_{IN}=0.2V_{DD}$	"L" level hold Tr. Note 1. See Figure 2.	40	200	800	kΩ
	$R_{IN}1B$	$V_{IN}=V_{DD}$	Pull-down resistor. See Figure 2.	20	80	300	kΩ
	$R_{IN}1C$	$V_{IN}=0.8V_{DD}$	"H" level hold Tr. Note 1. See Figure 2.	40	200	800	kΩ
	$R_{IN}1D$	$V_{IN}=V_{SS}$	Pull-up resistor. Note 1. See Figure 2.	20	80	300	kΩ
	$R_{IN}2A$	$V_{IN}=0.2V_{DD}$	INT "L" level hold Tr.	40	200	800	kΩ
	$R_{IN}2B$	$V_{IN}=V_{DD}$	INT pull-down resistor	200	800	3000	kΩ
	$R_{IN}2C$	$V_{IN}=0.8V_{DD}$	INT "H" level hold Tr.	40	300	1200	kΩ
	$R_{IN}2D$	$V_{IN}=V_{SS}$	INT pull-up resistor	200	800	3000	kΩ
	$R_{IN}3$	$V_{IN}=V_{DD}$	RES pull-down resistor	10	30	50	kΩ
	$R_{IN}4$	$V_{IN}=V_{SS}$	RES pull-up resistor	10	30	50	kΩ
	$R_{IN}5$	$V_{IN}=V_{DD}$	TST pin pull-down resistor	30	130	500	kΩ
			V_{DD}= 3.0～4.0V				
High level output voltage	$V_{OH}(1)$	$I_{OH}=-1.0mA$	N1－4	V_{DD} −0.5			V
Low level output voltage	$V_{OL}(1)$	$I_{OL}=2.0mA$				0.5	V
High level output voltage	$V_{OH}(2)$	$I_{OH}=-500\mu A$	K1－4, P1－4, M1－4, SO1－4, A1－4 (Condition: Ports K, P, M, SO and A are used in the output mode.)	V_{DD} −0.5			V
Low level output voltage	$V_{OL}(2)$	$I_{OL}=500\mu A$				0.5	V
Leakage current with output OFF	$\|I_{OFF}\|$	$V_{OH}=13.5V$	N1－4 (Open specification) Figure 10.			1.0	μA
Segment port output impedance							
●CMOS output port mode							
High level output voltage	$V_{OH}(3)$	$I_{OH}=-300\mu A$	Segment PAD No22～40, 43～58 FLP-80 pin No44～78	V_{DD} −0.5			V
Low level output voltage	$V_{OL}(3)$	$I_{OL}=300\mu A$				0.5	V
● P-ch open drain output port type (See Figure 11)							
High level output voltage	$V_{OH}(3)$	$I_{OH}=-300\mu A$	Segment PAD No22～40, 43～58 FLP-80 pin No44～78	V_{DD} −0.5			V
Leakage current with output OFF	$\|I_{OFF}\|$	$V_{OL}=V_{SS}$				1.0	μA
● N-ch open drain output port type (See Figure 11)							
Low level output voltage	$V_{OL}(3)$	$I_{OL}=300\mu A$	Segment PAD No22～40, 43～58 FLP-80 pin No44～78			0.5	V
Leakage current with output OFF	$\|I_{OFF}\|$	$V_{OH}=V_{DD}$				1.0	μA

Note 1: 24 pins - S1 to S4, K1 to K4, P1 to P4, M1 to M4, SO1 to SO4 and A1 to A4.

Electrical characteristics/V_{DD}=3.0 to 4.5V, V_{SS}=0V, Ta=-30 to +70℃

Item	Symbol	Conditions/terminals	min	typ	max	unit
● Static lighting format						
High level output voltage	$V_{OH}(4)$	I_{OH}=−20μA, Segment PAD №22~40, 43~58, FLP-80 pin №44~78	V_{DD}−0.2			V
Low level output voltage	$V_{OL}(4)$	I_{OL}= 20μA, Segment PAD №22~40, 43~58, FLP-80 pin №44~78			0.2	V
High level output voltage	$V_{OH}(5)$	I_{OH}=−100μA, COM1	V_{DD}−0.2			V
Low level output voltage	$V_{OL}(5)$	I_{OL}= 100μA, COM1			0.2	V
● 1/2 bias lighting format						
High level output voltage	$V_{OH}(4)$	I_{OH}=−20μA, Segment PAD №22~40, 43~58, FLP-80 pin №44~78	V_{DD}−0.2			V
Low level output voltage	$V_{OL}(4)$	I_{OL}= 20μA, Segment PAD №22~40, 43~58, FLP-80 pin №44~78			0.2	V
High level output voltage	$V_{OH}(5)$	I_{OH}=−100μA	V_{DD}−0.2			V
Medium level output voltage	V_{OM}	I_{OH}=−100μA, COM1 − 4	$V_{DD}/2$−0.2		$V_{DD}/2$+0.2	V
		I_{OL}= 100μA, COM1 − 4				V
Low level output voltage	$V_{OL}(5)$	I_{OL}= 100μA, COM1 − 4			0.2	V
● 1/3 bias lighting format --- This bias mode cannot be adopted if the V_{DD} range = 3.0V to 4.0V						
Leakage current at supply voltage	$I_{LEK}(1)$	V_{DD}=3.0V Ta=25℃ See Figure 3.		0.2	1.0	μA
Leakage current at supply voltage	$I_{LEK}(2)$	V_{DD}=3.0 V Ta=50℃ See Figure 3.		1.0	5.0	μA
Input leakage current	I_{OFF}	V_{DD}=3.0V, S1-4, K1-4, P1-4, M1-4, SO1 − 4, A1 − 4, INT, RES			1.0	μA
		V_{IN}=V_{DD}				μA
		V_{IN}=V_{SS} (Conditions: Ports K, P, M, SO and A are used in the input mode. INT and RES: Open.)	−1.0			μA
Output voltage 1	$V_{DD}1-(1)$	V_{DD}=3.0V, C1=C2=0.1μF $V_{DD}1$=Vo ½Bias, fopg=32.768kHz See Figure 4.	1.3	1.5	1.7	V
Supply current 1	$I_{DD}1$-1	V_{DD}=3.0V Ta=25℃ Xtal oscillation mode 32kHz crystal oscillation mode Cg=20pF, Cl=25kΩ At the HALT operation mode. See Figure 6. LCD=½Bias		4.0	8.0	μA
	$I_{DD}1$-2	V_{DD}=3.0V Ta=50℃		6.0	20	μA
Supply current 2	$I_{DD}2$-1	V_{DD}=3.0V Ta=25℃ Xtal oscillation mode Xtal : 38kHz or 65kHz XCg=10pF, Cl=25kΩ At the HALT operation mode. See Figure 6. LCD=1/3Bias		6.0	10	μA
	$I_{DD}2$-2	V_{DD}=3.0V Ta=50℃		10	30	μA
Supply current 3	$I_{DD}3$-1	V_{DD}=3.0V Ta=25℃ CF oscillation mode CF : 400kHz Ccg=Ccd=330pF At the HALT operation mode. See Figure 7.		150	300	μA
	$I_{DD}3$-2	V_{DD}=3.0V Ta=50℃		200	500	μA
Oscillation start voltage	$\|V_{STT}\|$	Tstt≦5 sec. Xtal oscillation mode 32KHz crystal oscillation mode Cg=20pF Cl≦25kΩ See Figure 6.			2.2	V
Oscillation hold voltage	$\|V_{HOLD}\|$		2.0		6.0	V
Oscillation start time	$\|Tstt\|$	V_{DD}=2.2V			5	s
Oscillation stability	Δf	V_{DD}=2.95~3.05V			3	ppm
Oscillation start voltage	$\|Vstt\|$	Tstt≦5 sec. Xtal oscillation mode 38kHz or 65kHz Xtal XCg=10pF Cl≦25kΩ See Figure 6.			2.4	V
Oscillation hold voltage	$\|V_{HOLD}\|$		2.2		6.0	V
Oscillation start time	$\|Tstt\|$	V_{DD}=2.4V			5	s
Oscillation start voltage	$\|Vstt\|$	Tstt≦30ms CF oscillation mode 400kHz CF Ccg=Ccd=330pF See Figure 7.			2.4	V
Oscillation hold voltage	$\|V_{HOLD}\|$		2.2		6.0	V
Oscillation start time	$\|Tstt\|$	V_{DD}=2.4V			30	ms
Oscillation start voltage	$\|Vstt\|$	Tstt≦30ms CF oscillation mode 800kHz CF Ccg=Ccd=220pF or 100pF See Figure 7.			2.4	V
Oscillation hold voltage	$\|V_{HOLD}\|$		2.2		6.0	V
Oscillation start time	$\|Tstt\|$	V_{DD}=2.4V			30	ms
Oscillation correction capacitance	Cd	V_{DD}=3.0V XTOUT pin (internal capacitor)	16	20	24	pF

Electrical characteristics/V_{SS}=4.5 to 6.0V, V_{SS}=0V, Ta=-30 to +70°C

Item	Symbol	Conditions/terminals	min	typ	max	unit
Input resistance	$R_{IN}1A$	$V_{IN}=0.2V_{DD}$ "L" level hold Tr. Note 1. See Figure 2.	30	120	500	kΩ
	$R_{IN}1B$	$V_{IN}=V_{DD}$ Pull-down resistor. Note 1. See Figure 2.	10	50	200	kΩ
	$R_{IN}1C$	$V_{IN}=0.8V_{DD}$ "H" level hold Tr. Note 1. See Figure 2.	30	120	500	kΩ
	$R_{IN}1D$	$V_{IN}=V_{SS}$ Pull-up resistor. Note 1. See Figure 2.	10	50	200	kΩ
	$R_{IN}2A$	$V_{IN}=0.2V_{DD}$ INT "L" level hold Tr.	30	120	500	kΩ
	$R_{IN}2B$	$V_{IN}=V_{DD}$ INT pull-down resistor	100	500	2000	kΩ
	$R_{IN}2C$	$V_{IN}=0.8V_{DD}$ INT "H" level hold Tr.	30	120	500	kΩ
	$R_{IN}2D$	$V_{IN}=V_{SS}$ INT pull-up resistor	100	500	2000	kΩ
	$R_{IN}3$	$V_{IN}=V_{DD}$ RES pull-down resistor	10	30	50	kΩ
	$R_{IN}4$	$V_{IN}=V_{SS}$ RES pull-up resistor	10	30	50	kΩ
	$R_{IN}5$	$V_{IN}=V_{DD}$ TST pin pull-down resistor	20	70	300	kΩ
High level output voltage	$V_{OH}(1)$	$I_{OH}=-5.0mA$ N1−4	$V_{DD}-0.5$			V
Low level output voltage	$V_{OL}(1)$	$I_{OL}=10.0mA$ N1−4			0.5	V
High level output voltage	$V_{OH}(2)$	$I_{OH}=-1.0mA$ K1−4, P1−4, M1−4, SO1−4, A1−4	$V_{DD}-0.5$	$V_{DD}-0.2$		V
Low level output voltage	$V_{OL}(2)$	$I_{OL}=2.0mA$ Condition: Ports K, P, M, SO and A are used in the output mode.		0.2	0.5	V
Leakage current with output OFF	$\|I_{OFF}\|$	$V_{OH}=13.5V$ N1−4 Open specification Figure 10			1.0	μA
Segment port output impedance						
● CMOS output port mode						
High level output voltage	$V_{OH}(3)$	$I_{OH}=-500\mu A$ Segment PAD No22~40, 43~58	$V_{DD}-0.5$	$V_{DD}-0.2$		V
Low level output voltage	$V_{OL}(3)$	$I_{OL}=500\mu A$ FLP-80 pin No44~78			0.5	V
● P-ch open drain output port type (See Figure 11)						
High level output voltage	$V_{OH}(4)$	$I_{OH}=-500\mu A$ Segment PAD No22~40, 43~58	$V_{DD}-0.5$	$V_{DD}-0.2$		V
Leakage current with output OFF	$\|I_{OFF}\|$	$V_{OL}=V_{SS}2$ FLP-80 pin No44~78			1.0	μA
● N-ch open drain output port type (See Figure 11)						
Low level output voltage	$V_{OL}(4)$	$I_{OL}=500\mu A$ Segment PAD No22~40, 43~58		0.2	0.5	V
Leakage current at supply voltage	$\|I_{OFF}\|$	$V_{OH}=V_{DD}$ FLP-80 pin No44~78			1.0	μA

Electrical characteristics/V_{SS}=4.5 to 6.0V, V_{SS}=0V, Ta=-30 to +70℃

Item	Symbol	Conditions/terminals	min	typ	max	unit
●Static lighting format						
High level output voltage	$V_{OH}(4)$	I_{OH}=−40μA, Segment PAD No22~40, 43~58	V_{DD} −0.2			V
Low level output voltage	$V_{OL}(4)$	I_{OL}= 40μA, FLP-80 pin No44~78			0.2	V
High level output voltage	$V_{OH}(6)$	I_{OH}=−400μA, COM1	V_{DD} −0.2			V
Low level output voltage	$V_{OL}(6)$	I_{OL}= 400μA			0.2	V
●1/2 bias lighting format						
High level output voltage	$V_{OH}(4)$	I_{OH}=−40μA, Segment PAD No22~40, 43~58	V_{DD} −0.2			V
Low level output voltage	$V_{OL}(4)$	I_{OL}= 40μA, FLP-80 pin No44~78			0.2	V
High level output voltage	$V_{OH}(6)$	I_{OH}=−400μA	V_{DD} −0.2			V
Medium level output voltage	$V_{OM}2$-1	I_{OH}=−400μA, I_{OL}= 400μA, COM1−4	$V_{DD}/2$ −0.2		$V_{DD}/2$ +0.2	V
Low level output voltage	$V_{OL}(6)$	I_{OL}= 400μA			0.2	V
●1/3 bias lighting format						
High level output voltage	$V_{OH}(4)$	I_{OH}=−40μA	V_{DD} −0.2			V
Medium level output voltage	$V_{OM}1$-1	I_{OH}=−40μA, Segment PAD No22~40, 43~58	$2V_{DD}/3$ −0.2		$2V_{DD}/3$ +0.2	V
	$V_{OM}1$-2	I_{OL}= 40μA, FLP-80 pin No44~78	$V_{DD}/3$ −0.2		$V_{DD}/3$ +0.2	V
Low level output voltage	$V_{OL}(4)$	I_{OL}= 40μA			0.2	V
High level output voltage	$V_{OH}(6)$	I_{OH}=−400μA	V_{DD} −0.2			V
Medium level output voltage	$V_{OM}2$-1	I_{OH}=−400μA, COM1−4	$2V_{DD}/3$ −0.2		$2V_{DD}/3$ +0.2	V
	$V_{OM}2$-2	I_{OL}= 400μA	$V_{DD}/3$ −0.2		$V_{DD}/3$ +0.2	V
Low level output voltage	$V_{OL}(6)$	I_{OL}= 400μA			0.2	V

Electrical characteristics/V_{SS}=4.5 to 6.0V, V_{SS}=0V, Ta=-30 to +70℃

Item	Symbol	Conditions/terminals	min	typ	max	unit
Leakage current at supply voltage	$I_{LEK}(1)$	V_{DD}=6.0V Ta=25℃ See Figure 3.		0.2	1.0	μA
Leakage current at supply voltage	$I_{LEK}(2)$	V_{DD}=6.0V Ta=50℃ See Figure 3.		1.0	5.0	μA
Input leakage current	I_{OFF}	V_{DD}=6.0V, V_{IN}=V_{DD}: S1–4, K1–4, P1–4, M1–4, SO1–4, A1–4, INT, RES			1.0	μA
		V_{IN}=V_{SS} (Condition: Ports K, P, M, SO and A are used in the input mode. INT and RES: Open.)	−1.0			μA
Output voltage 2	$V_{DD}1$-(2)	V_{DD}=5.0V, C1=C2=0.1μF See Figure 4, $V_{DD}1$=Vo, ½Bias, fopg=32.768kHz	2.4	2.5	2.6	V
Output voltage 3	$V_{DD}1$-(3)	V_{DD}=5.0V, C1=C2=0.1μF See Figure 5, $V_{DD}1$=Vo	1.4	1.67	1.8	V
	$V_{DD}2$-(3)	½Bias, fopg=32.768kHz $V_{DD}2$=Vo	3.1	3.33	3.5	V
Supply current 1	$I_{DD}1$-1	V_{DD}=5.0V Ta=25℃ Xtal oscillation mode 32kHz crystal oscillation mode		15	30	μA
	$I_{DD}1$-2	V_{DD}=5.0V Ta=50℃ XCg=20pF, Cl=25kΩ At the HALT operation mode. See Figure 6. LCD=⅓Bias		20	50	μA
Supply current 2	$I_{DD}2$-1	V_{DD}=5.0V Ta=25℃ Xtal oscillation mode Xtal : 38kHz or 65kHz		15	30	μA
	$I_{DD}2$-2	V_{DD}=5.0V Ta=50℃ XCg=10pF, Cl=25kΩ At the HALT operation mode. See Figure 6. LCD=1/3 Bias		20	50	μA
Supply current 3	$I_{DD}3$-1	V_{DD}=5.0V Ta=25℃ CF oscillation mode CF : 400kHz		400	600	μA
	$I_{DD}3$-2	V_{DD}=5.0V Ta=50℃ Ccg=Ccd=330pF At the HALT operation mode. See Figure 7.		450	600	μA
Supply current 4	$I_{DD}4$-1	V_{DD}=5.0V Ta=25℃ CF oscillation mode CF : 1000kHz		450	650	μA
	$I_{DD}4$-2	V_{DD}=5.0V Ta=50℃ Ccg=Ccd=100pF At the HALT operation mode. See Figure 8.		500	700	μA
Supply current 5	$I_{DD}5$-1	V_{DD}=5.0V Ta=25℃ CF oscillation mode CF : 2000kHz		500	700	μA
	$I_{DD}5$-2	V_{DD}=5.0V Ta=50℃ Ccg=Ccd=33pF At the HALT operation mode. See Figure 8.		550	750	μA
Supply current 6	$I_{DD}6$-1	V_{DD}=5.0V Ta=25℃ CF oscillation mode CF : 4000kHz		700	900	μA
	$I_{DD}6$-2	V_{DD}=5.0V Ta=50℃ Ccg=Ccd=33pF At the HALT operation mode. See Figure 8.		800	1000	μA
Oscillation adjustment capacitance	Cd	V_{DD}=5.0V XTOUT pin (internal capacitor)	16	20	24	pF

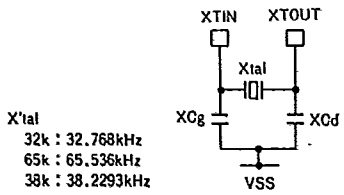


Figure 1-1. Fixed oscillation circuit (XT terminal)

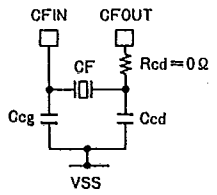


Figure 1-2. Fixed oscillation circuit (CF terminal)

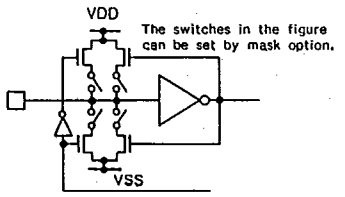


Figure 2. Input structure of ports S, K, P, M, SO and A

Recommended ceramic resonators

Manufacturer	Murata			Kyocera		
Frequency \ Item	Product number	Ccg(pF)	Ccd(pF)	Product number	Ccg(pF)	Ccd(pF)
400kHz	CSB400P	330	330	KBR-400B	330	330
800kHz	CSB800J	220	220	KBR-800H	100	100
1 MHz	CSB1000J	220	220	KBR-1000H	100	100
2 MHz	CSA2.00MG(CST2.00MG)	33	33	KBR-2.0MS	33	33
4 MHz	CSA4.00MG(CST4.00MG)	33	33	KBR-4.0MS	33	33

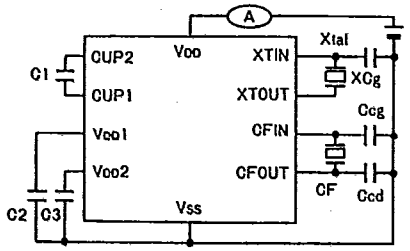


Figure 3. Measuring circuit for leakage current at power source

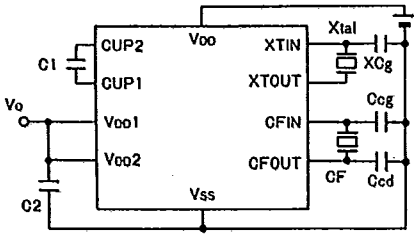
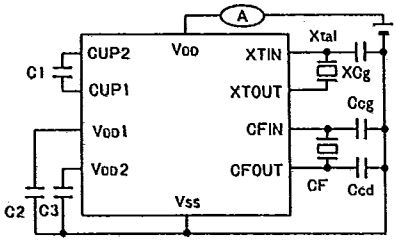
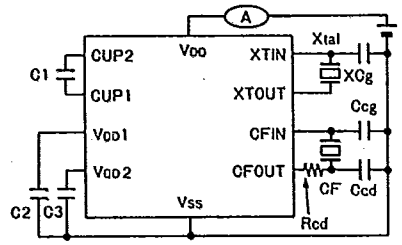


Figure 4. Output voltage measuring circuit



Note: CF in the stop state.
Xtal: 32kHz, 38kHz or 65kHz.
C1, C2 and C3: 0.1 microfarad

Figure 6. Supply current measuring circuit



Note: X'tal in the stop state

Figure 8. Supply current measuring circuit

STOP state

Port S	: With input resistor ON
I/O port	: Output mode and output data level "H"
RES and INT pin	: With internal resistor and externally open.
LCD port	: Not including externally added device current.
Xtal	: 32kHz to 65kHz.
CF	: 200kHz to 4MHz.
Xtal	: 32kHz
C1, C2 and C3	: 0.1 microfarad
LCD port	: Open
CF	: 200kHz to 4MHz

Figures 4 and 5

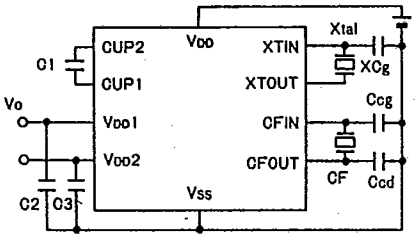
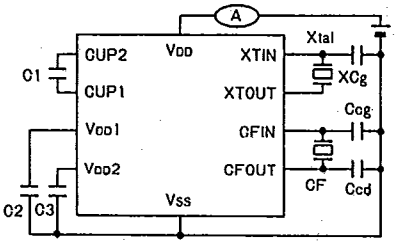
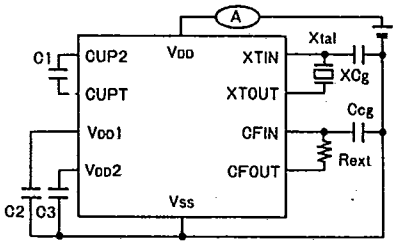


Figure 5. Output voltage measuring circuit



Note: X'tal in the stop state.

Figure 7. Supply current measuring circuit



Note: X'tal in the stop state.

Figure 9. Supply current measuring circuit

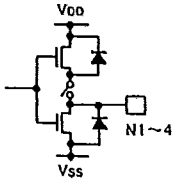


Figure 10. Output structure of port N (N1 to N4)

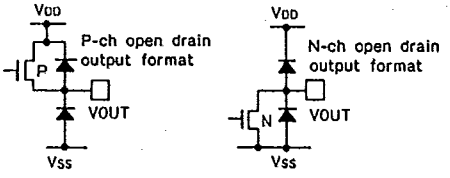


Figure 11. Structure of segment open drain output format

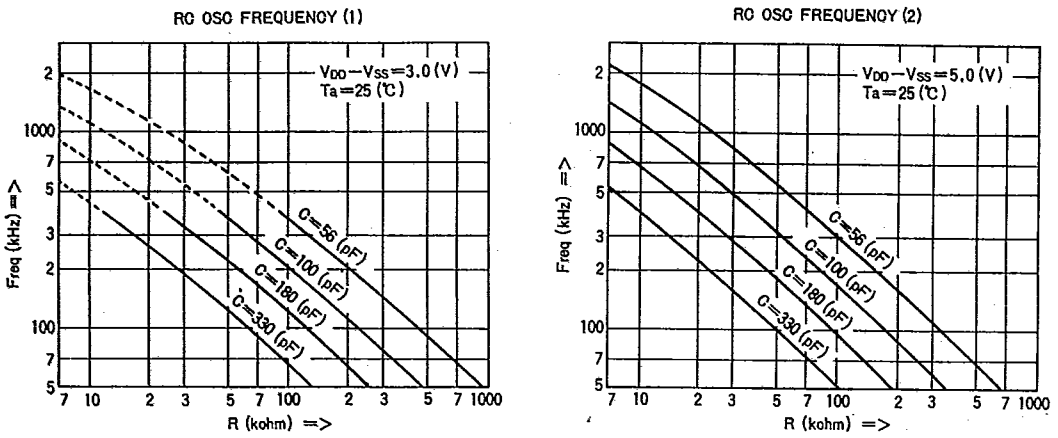
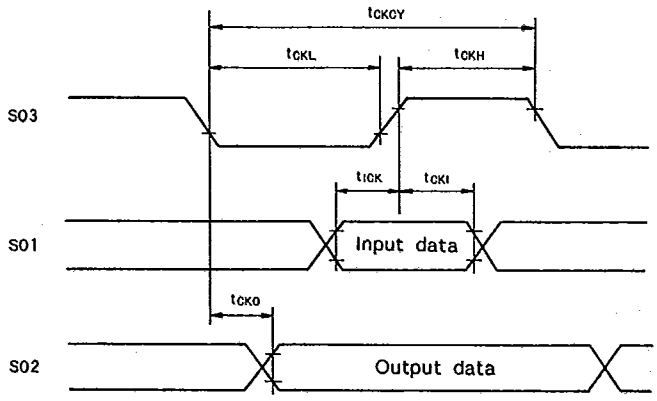
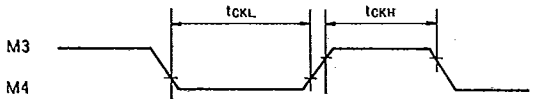


Figure 12. Sample RC oscillation frequency characteristics



tCKCY·····5μs MIN tCKL=tCKH·····2.4μs MIN
tICK·····1μs MIN tCKI ·····1μs MIN
tCKO·····1μs MAX
VDD=3.0~6.0V

Figure 13. Serial input/output timing (at external clock mode)



tCKL, tCKH·····More than cycle time

Figure 14. Timer 1, timer 2 external clock input timing
(at external clock mode, M3, M4 terminals)

Instruction set for the LC5863H/64H microcomputers

Conventions

AC	: Accumulator	HQF	: HALT request flag
ACn	: Accumulator bit number	HEFn	: HALT mode release request signal enable flag
CF	: Carry flag		
DP	: Data pointer	HRFn	: HALT mode release request signal flag n
DPF	: Data pointer flag		
PC	: Program counter	TM	: Timer
[P( )]	: Port ( ) contents	L	: LCD latch
Rx	: Address Rx in the data memory (RAM)	Breg	: B register
		STS	: Status register
Rxn	: Bit number of address Rx in the data memory (RAM)	MS	: Timer mode select
		( )	: Content
IEFn	: Interrupt enable flag n of control register 3 (CTL3)	←	: Data transfer direction or result storage destination
WRFn	: Working register flag n	A	: Logical product (AND)
SCFn	: Start condition flag n	V	: Logical sum (OR)
PDF	: Pull-down flag	∀	: Exclusive logic sum (X-or)

Instruction set for the LC5863H/64H microcomputers

Instruction type	Mnemonic	Op code	Operations	Operations description	Affected flags
Accumulator manipulation instruction	SR0 X	0 1 1 0 0 0 0 0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$0 \rightarrow (Rx)_3 \rightarrow (Rx)_2 \rightarrow (Rx)_1 \rightarrow (Rx)_0$ AC←(Rx)	Shift right the contents at address Rx. Zero (0) is inserted into the most significant bit (MSB). Then transfer to the accumulator (AC) the new contents at address Rx.	
	SR1 X	0 1 1 0 0 0 0 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$1 \rightarrow (Rx)_3 \rightarrow (Rx)_2 \rightarrow (Rx)_1 \rightarrow (Rx)_0$ AC←(Rx)	Shift right the contents at address Rx. One (1) is inserted into the most significant bit (MSB). Then transfer to the accumulator (AC) the new contents at address Rx.	
	SL0 X	0 1 1 0 0 0 1 0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$(Rx)_3 \leftarrow (Rx)_2 \leftarrow (Rx)_1 \leftarrow (Rx)_0 \leftarrow 0$ AC←(Rx)	Shift left the contents at address Rx. Zero (0) is inserted into the least significant bit (LSB). Then transfer to the accumulator (AC) the new contents at address Rx.	
	SL1 X	0 1 1 0 0 0 1 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$(Rx)_3 \leftarrow (Rx)_2 \leftarrow (Rx)_1 \leftarrow (Rx)_0 \leftarrow 1$ AC←(Rx)	Shift left the contents at address Rx. One (1) is inserted into the least significant bit (LSB). Then transfer to the accumulator (AC) the new contents at address Rx.	
	RRC X	0 1 1 0 1 0 0 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$\lceil (Rx)_3 \rightarrow (Rx)_2 \rightarrow (Rx)_1 \rightarrow (Rx)_0 \rightarrow CF \rightarrow \rceil$ AC←(Rx)	Rotate right the contents at address Rx with CF. Then transfer to the accumulator (AC) the new contents at address Rx.	CF
	RLC X	0 1 1 0 1 0 1 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$\lceil (Rx)_3 \leftarrow (Rx)_2 \leftarrow (Rx)_1 \leftarrow (Rx)_0 \leftarrow CF \leftarrow \rceil$ AC←(Rx)	Rotate left the contents at address Rx with CF. Then transfer to the accumulator (AC) the new contents at address Rx.	CF
	MPF X	0 1 1 0 1 1 1 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	(Rx), AC←OPG1, OPG2, DPF, CF	Transfer the contents of ROM page flags 1 and 2, CF and DPF to the accumulator (AC) and address Rx in the RAM.	
	MRPF X	0 0 1 0 1 1 1 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC←OPG1, OPG2, CF←(Rx)	Transfer the contents at address Rx in the RAM to ROM page flags 1 and 2, and CF. Note that the contents the DPF remain unchenged.	CF
	SCF	1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 1	CF←1	Set the carry flag (CF).	CF
	RCF	1 1 1 1 0 0 1 0 0 0 0 0 0 0 0 1	CF←0	Reset the carry flag (CF)	CF
Memory manipulation instruction	SRAPF D	1 1 1 0 1 1 1 0 0 0 0 0 0 0 D_1 D_0	RAM Page←D D=0~3	Select RAM pages. Note that each RAM page area consists of 1K bits (256 x 4 bits).	APG
	LRAPF X	0 1 1 0 1 1 0 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$(Rx)_0$, $(Rx)_1$←RAM Page $(Rx)_2$, $(Rx)_3$←RAM Page (SAVE)	Transfer the contents of the RAM page flag and RAM save page to the accumulator (AC) and address Rx in the RAM.	
	SBNK D	1 1 1 0 1 0 1 0 0 0 0 0 D_3 D_2 D_1 D_0	Bank←D D=0~15	Set immediate data (D) in the bank register (BNK).	BNK
	MRBK X	0 1 1 0 0 1 0 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Bank←(Rx)	Transfer to the bank register (BNK) the contents at address Rx in the RAM.	BNK
	MBNK X	0 1 1 0 1 1 1 0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC←Bank (Rx)←Bank	Transfer to the accumulator (AC) and address Rx in the RAM the contents of the bank register (BNK).	
	SDP D	1 1 1 0 1 1 1 1 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	DP←D D=0~255	Set immediate data (D) in the data pointer (DP).	DPH DPL
	MRDH X	0 1 1 0 0 1 1 0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	DPH←(Rx)	Transfer to the 4 upper bits (DP_H) of the data pointer (DP) the contents at address Rx in the RAM.	DPH
	MRDL X	0 1 1 0 0 1 1 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	DPL←(Rx)	Transfer to the 4 lower bits (DP_L) of the data pointer (DP) the contents at address Rx in the RAM.	DPL
	MDPR X	0 1 1 1 1 1 0 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	(Rx)←AC, AC←DPL Breg←DPH	Transfer to the accumulator (AC) and address Rx in the RAM the contents of the 4 lower bits (DP_L) of the data pointer (DP) and transfer to the B register the contents of the 4 upper bits (DP_H).	
Arithmetic operation instruction	ADC X	0 1 0 0 0 0 0 0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC←(Rx)+(AC)+CF	Add the contents of address Rx, AC and CF together in binary and then store the binary sum into the accumulator (AC).	CF
	ADC* X	0 1 0 0 0 0 0 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC←(Rx)+(AC)+CF (Rx)←AC	Add the contents of address Rx, AC and CF together in binary and then store the binary sum into the accumulator (AC) and address Rx in the RAM.	CF
	SBC X	0 1 0 0 0 0 1 0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$AC \leftarrow (Rx)+\overline{(AC)}+CF$	Subtract the AC contents from those of address Rx and CF in binary and then store the binary difference into the accumulator (AC).	CF
	SBC* X	0 1 0 0 0 0 1 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$AC \leftarrow (Rx)+\overline{(AC)}+CF$ (Rx)←AC	Subtract the AC contents from those of address Rx and CF in binary and then store the binary difference into the accumulator (AC) and address Rx in the RAM.	CF
	ADD X	0 1 0 0 0 1 0 0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC←(Rx)+(AC)	Add the contents of address Rx and accumulator (AC) together in binary and then store the binary sum into the AC.	CF
	ADD* X	0 1 0 0 0 1 0 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC←(Rx)+(AC) (Rx)←AC	Add the contents of address Rx and accumulator (AC) in binary and then store the binary sum into the AC and address Rx in the RAM.	CF
	SUB X	0 1 0 0 0 1 1 0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$AC \leftarrow (Rx)+\overline{(AC)}+1$	Subtract the AC contents from those of address Rx in the RAM in binary and then store the binary difference into the accumulator (AC).	CF
	SUB* X	0 1 0 0 0 1 1 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$AC \leftarrow (Rx)+\overline{(AC)}+1$ (Rx)←AC	Subtract the AC contents from those of address Rx in the RAM in binary and then store the binary difference into the accumulator (AC) and address Rx.	CF

Instruction type	Mnemonic	Op code	Operations	Operations description	Affected flags
Arithmetic operation instruction	ADN X	0 1 0 0 1 0 0 0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC←(Rx)+(AC)	Add the contents of the accumulator (AC) and those of address Rx in the RAM together in binary and then store the binary sum into the AC.	
	ADN* X	0 1 0 0 1 0 0 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC←(Rx)+(AC) (Rx)←AC	Add the contents of the accumulator (AC) and those of address Rx in the RAM in binary and then store the binary sum into the AC and address Rx in the RAM.	
	ADCI X,Y	0 1 0 1 0 0 0 0 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC←(Rx)+Y+CF	Add the contents of address Rx in the RAM, immediate data Y and the CF contents together in binary and then store the binary sum into the accumulator (AC).	CF
	ADCI* X, Y	0 1 0 1 0 0 0 1 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC←(Rx)+Y+CF (Rx)←AC	Add the contents of address Rx in the RAM, immediate data Y and the CF contents together in binary and then store the binary sum into the accumulator (AC) and address Rx.	CF
	SBCI X, Y	0 1 0 1 0 0 1 0 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC←(Rx)+$\overline{Y}$+CF	Subtract immediate data Y from the contents of address Rx and CF in binary and then store the binary difference into the accumulator (AC).	CF
	SBCI* X, Y	0 1 0 1 0 0 1 1 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC←(Rx)+$\overline{Y}$+CF (Rx)←AC	Subtract immediate data Y from the contents of address Rx and CF in binary and then store the binary difference into the accumulator (AC) and address Rx.	CF
	ADDI X, Y	0 1 0 1 0 1 0 0 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC←(Rx)+Y	Add the contents of address Rx and immediate data Y together in binary and then store the binary sum into the accumulator (AC).	CF
	ADDI* X, Y	0 1 0 1 0 1 0 1 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC←(Rx)+Y (Rx)←AC	Add the contents of address Rx and immediate data Y together in binary and then store the binary sum into the accumulator (AC) and address Rx.	CF
	SUBI X, Y	0 1 0 1 0 1 1 0 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC←(Rx)+$\overline{Y}$+1	Subtract immediate data Y from the contents of address Rx in binary and then store the binary difference into the accumulator (AC).	CF
	SUBI* X, Y	0 1 0 1 0 1 1 1 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC←(Rx)+$\overline{Y}$+1 (Rx)←AC	Subtract immediate data Y from the contents of address Rx in binary and then store the binary difference into the accumulator (AC) and address Rx.	CF
	ADNI X, Y	0 1 0 1 1 0 0 0 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC←(Rx)+Y	Add the contents of address Rx in the RAM and immediate data Y together in binary and then store the binary sum into the accumulator (AC).	
	ADNI* X, Y	0 1 0 1 1 0 0 1 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC←(Rx)+Y (Rx)←AC	Add the contents of address Rx in the RAM and immediate data Y together in binary and then store the binary sum into the accumulator (AC) and address Rx.	
Logical operation instruction	AND X	0 1 0 0 1 0 1 0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC←(Rx)∧(AC)	AND the contents of address Rx with those of the accumulator (AC) and then store the logical product into the accumulator (AC).	
	AND* X	0 1 0 0 1 0 1 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC←(Rx)∧(AC) (Rx)←AC	AND the contents of address Rx with those of the accumulator (AC) and then store the logical product into the accumulator (AC) and address Rx in the RAM.	
	EOR X	0 1 0 0 1 1 0 0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC←(Rx)∀(AC)	Exclusive OR the contents of address Rx with those of the accumulator (AC) and then store the logical sum into the accumulator (AC).	
	EOR* X	0 1 0 0 1 1 0 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC←(Rx)∀(AC) (Rx)←AC	Exclusive OR the contents of address Rx with those of the accumulator (AC) and then store the logical sum into the accumulator (AC) and address Rx.	
	OR X	0 1 0 0 1 1 1 0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC←(Rx)∨(AC)	OR the contents of address Rx with those of the accumulator (AC) and then store the logical sum into the accumulator (AC).	
	OR* X	0 1 0 0 1 1 1 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC←(Rx)∨(AC) (Rx)←AC	OR the contents of address Rx with immediate data and then store the logical sum into the accumulator (AC) and address Rx in the data memory (RAM).	
	ANDI X, Y	0 1 0 1 1 0 1 0 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC←(Rx)∧Y	AND the contents of address Rx with immediate data and then store the logical product into the accumulator (AC).	
	ANDI* X, Y	0 1 0 1 1 0 1 1 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC←(Rx)∧Y (Rx)←AC	AND the contents of address Rx with immediate data and then store the logical product into the accumulator (AC) and address Rx in the data memory (RAM).	
	EORI X, Y	0 1 0 1 1 1 0 0 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC←(Rx)∀Y	Exclusive OR the contents of address Rx with immediate data and then store the logical product into the accumulator (AC).	
	EORI* X, Y	0 1 0 1 1 1 0 1 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC←(Rx)∀Y (Rx)←AC	Exclusive OR the contents of address Rx with immediate data and then store the logical product into the accumulator (AC) and address Rx in the data memory (RAM).	
	ORI X, Y	0 1 0 1 1 1 1 0 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC←(Rx)∨Y	OR the contents of address Rx with immediate data and then store the logical sum into the accumulator (AC).	
	ORI* X, Y	0 1 0 1 1 1 1 1 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC←(Rx)∨Y (Rx)←AC	OR the contents of address Rx with immediate data and then store the logical sum into the accumulator (AC) and address Rx in the data memory (RAM).	
Branch instruction and Subroutine instruction	JMP X	1 1 0 0 0 X_{10} X_9 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	PC(X_{10}~X_0)←X_{10}~X_0 PC(X_{12}~X_{11})←ROM Page	Load the data specified by bits X_A to X_0 and the contents of the ROM page flag into the program counter (PC) and then jump unconditionally.	
	BAB0 X	1 0 0 0 0 X_{10} X_9 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	if AC_0=1 PC(X_{10}~X_0)←X_{10}~X_0 PC(X_{12}~X_{11})←ROM Page	Same as the JMP instruction if bit 0 of the accumulator (AC) is "1". Processed as the NOP instruction if bit 0 of the accumulator (AC) is "0".	
	BAB1 X	1 0 0 0 1 X_{10} X_9 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	if AC_1=1 PC(X_{10}~X_0)←X_{10}~X_0 PC(X_{12}~X_{11})←ROM Page	Same as the JMP instruction if bit 1 of the accumulator (AC) is "1". Processed as the NOP instruction if bit 1 of the accumulator (AC) is "0".	

Instruction type	Mnemonic	Op code	Operations	Operations description	Affected flags
Branch instruction and subroutine instruction	BAB2 X	1 0 0 1 0 $X_{10}X_9X_8$ $X_7X_6X_5X_4$ $X_3X_2X_1X_0$	if $AC_2=1$ PC(X_{10}~X_0) ← X_{10}~X_0 PC(X_{12}~X_{11}) ← ROM Page	Same as the JMP instruction if bit 2 of the accumulator (AC) is "1". Processed as the NOP instruction if bit 2 of the accumulator (AC) is "0".	
	BAB3 X	1 0 0 1 1 $X_{10}X_9X_8$ $X_7X_6X_5X_4$ $X_3X_2X_1X_0$	if $AC_3=1$ PC(X_{10}~X_0) ← X_{10}~X_0 PC(X_{12}~X_{11}) ← ROM Page	Same as the JMP instruction if bit 3 of the accumulator (AC) is "1". Processed as the NOP instruction if bit 3 of the accumulator (AC) is "0".	
	BAZ X	1 0 1 1 0 $X_{10}X_9X_8$ $X_7X_6X_5X_4$ $X_3X_2X_1X_0$	if AC = 0 PC(X_{10}~X_0) ← X_{10}~X_0 PC(X_{12}~X_{11}) ← ROM Page	Same as the JMP instruction if the content of the accumulator (AC) is "0". Processed as the NOP instruction if the content of the accumulator (AC) is not "0".	
	BANZ X	1 0 1 0 0 $X_{10}X_9X_8$ $X_7X_6X_5X_4$ $X_3X_2X_1X_0$	if AC ≠ 0 PC(X_{10}~X_0) ← X_{10}~X_0 PC(X_{12}~X_{11}) ← ROM Page	Same as the JMP instruction if the content of the accumulator (AC) is not "0". Processed as the NOP instruction if the content of the accumulator (AC) is "0".	
	BCH X	1 0 1 1 1 $X_{10}X_9X_8$ $X_7X_6X_5X_4$ $X_3X_2X_1X_0$	if CF = 1 PC(X_{10}~X_0) ← X_{10}~X_0 PC(X_{12}~X_{11}) ← ROM Page	Same as the JMP instruction if the content of the carry flag (CF) is "1". Processed as the NOP instruction if the content of the carry flag (CF) is "0".	
	BCNH X	1 0 1 0 1 $X_{10}X_9X_8$ $X_7X_6X_5X_4$ $X_3X_2X_1X_0$	if CF ≠ 1 PC(X_{10}~X_0) ← X_{10}~X_0 PC(X_{12}~X_{11}) ← ROM Page	Same as the JMP instruction if the content of the carry flag (CF) is "0". Processed as the NOP instruction if the content of the carry flag (CF) is "1".	
	CALL X	1 1 0 0 1 $X_{10}X_9X_8$ $X_7X_6X_5X_4$ $X_3X_2X_1X_0$	(STACK) ← (PC) + 1	Call a subroutine program stored at the address specified by immediate data X_0 to X_A and ROM page flag.	
	RTS	1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0	PC ← (STACK) DPF ← (STACK)	Return control to the main routine from a subroutine or an interrupt processing routine.	DPF
	RTSR	1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 1	PC ← (STACK) DPF ← (STACK)	Return control to the main routine from a subroutine or an interrupt processing routine. In this case, the HALT operation mode is released after control is transferred back to the main routine.	DPF
	POP	1 1 1 1 1 0 0 1 0 0 0 0 0 0 0 0	STACK ← STACK − 1	Decrement the stack pointer (STACK) by 1.	
CPU control instruction	SLOW	1 1 1 1 1 1 0 0 0 0 1 0 0 0 0 0	————	Force the system clock into the low speed (slow) operation mode.	
	FAST	1 1 1 1 1 1 0 0 0 1 0 0 0 0 0 0	————	Force the system clock into the high speed (fast) operation mode.	
	HALT	1 1 1 1 1 1 0 0 1 0 0 0 0 0 0 0	HALT	Force the CPU block operation into the HALT operation mode. The HALT mode can be released in the following conditions: - When interrupt request signal is accepted. - When any bit of status registers 3 and 4 (SCF0 to SCF7) is set.	
	HLTF	1 1 1 1 1 1 0 0 1 1 0 0 0 0 0 0	FAST & HALT	Force the system clock into the fast operation mode and then place the CPU in the HALT operation mode.	
	HLTL	1 1 1 1 1 1 0 0 1 0 1 0 0 0 0 0	SLOW & HALT	Force the system clock into the slow operation mode and then place the CPU in the HALT operation mode.	
	STOP	1 1 1 1 1 1 0 1 0 0 0 0 0 0 0 0	STOP	Put the CPU to the HALT state and then place the oscillator in the stop operation mode.	
	STPF	1 1 1 1 1 1 0 1 0 1 0 0 0 0 0 0	FAST & STOP	Force the system clock into the fast operation mode, and then place the CPU and the oscillator in the HALT mode and the stop mode respectively.	
	STPL	1 1 1 1 1 1 0 1 0 0 1 0 0 0 0 0	SLOW & STOP	Force the system clock into the slow operation mode, and then place the CPU and the oscillator in the HALT mode and the stop mode respectively.	

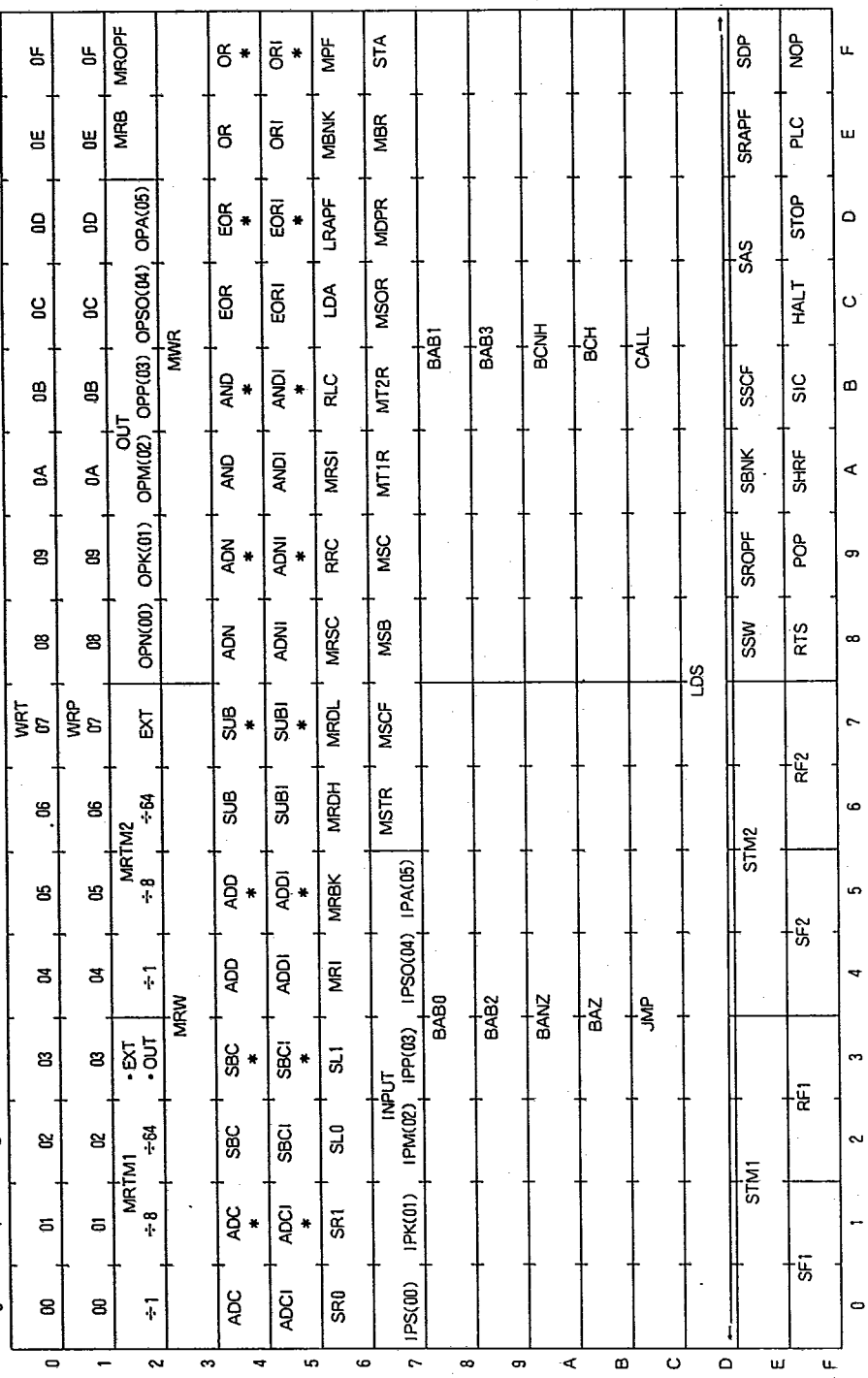
Instruction type	Mnemonic	Op code	Operations	Operations description	Affected flags
CPU control instruction	SHRF D	1 1 1 1 1 0 1 0 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Enable or disable interrupt request signals or HALT release request signals in the following manner: D_0: Enable (D_0 = 1) or disable (D_0 = 0) an interrupt request signal from the INT terminal. D_1: Enable (D_1 = 1) or disable (D_1 = 0) an interrupt request signal from the S/K port. D_2: Enable (D_2 = 1) or disable (D_2 = 0) an interrupt request signal from timer 1 or timer 2. D_3: Enable (D_3 = 1) or disable (D_3 = 0) an interrupt request signal from the SIO counter. D_4: Enable (D_4 = 1) or disable (D_4 = 0) a HALT release request caused by an overflow signal from the divider. D_5: Enable (D_5 = 1) or disable (D_5 = 0) a HALT release request caused by an underflow signal from timer 1. D_6: Enable (D_6 = 1) or disable (D_6 = 0) a HALT release request caused by an underflow signal from timer 2. D_7: D_5: Enable (D_7 = 1) or disable (D_7 = 0) a HALT release request caused by an overflow signal from the SIO counter.		$IEF_{0\sim3}$ $HRF_{0\sim3}$ Note: Interrupt enable flags IEF_0 to IEF_3 will be reset after interrupt requests are accepted.
	SIC D	1 1 1 1 1 0 1 1 0 0 0 0 D_3 D_2 D_1 D_0	$IEF_{0\sim3} \leftarrow D$ $D = 0\sim15$	Enable or disable the interrupt request signals corresponding to bits D0 to D3 of the SHRF instruction. This instruction sets the interrupt enable flag bits (IEF_0 to IEF_3).	$IEF_{0\sim3}$
	MRI X	0 1 1 0 0 1 0 0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$IEF_{0\sim3} \leftarrow (Rx)$ $D = 0\sim15$	Enable or disable the interrupt request signals corresponding to bits D_0 to D_3 of the SHRF instruction. This instruction is used to transfer the contents of address Rx in the RAM to 4-bit control register 3 (CTL3).	$IEF_{0\sim3}$
	PLC D	1 1 1 1 1 1 1 0 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Output the reset pulses according to the immediate data given by D_7 to D_0. D_0 : Reset HALT release request signal from the INT terminal. D_1 : Reset HALT release request signal from timer 1. D_2 : Reset HALT release request signal from timer 2. D_3 : Reset HALT release request signal from the SIO counter. D_4 : Reset the HALT release request caused by an overflow signal from the divider. D_5 : Reset the last 5 D-FFs (11 to 15)of the 16-level divider. D_6 : Reset the WD1 watchdog timer. D_7 : Reset the WD2 watchdog timer.		$HRF_{0\sim4}$
	MSB X	0 1 1 1 1 0 0 0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$AC \leftarrow (SCF_{0\sim3})$ $(Rx) \leftarrow AC$	- Load the contents of status register 3 (SCF_0 to SCF_3) into the accumulator (AC) and address Rx in the data memory (RAM). - The bits (SCF_0 to SCF_3) of status register 3 are set as follows. SCF_0 : Set when the INT terminal logic has been changed. SCF_1 : Set when the K port signal level has been changed. SCF_2 : Set when any flag bit of status register 4 has been set. SCF_3 : Set when the S port signal level has been changed.	
	MSC X	0 1 1 1 1 0 0 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$AC \leftarrow (SCF_{4\sim7})$ $(Rx) \leftarrow AC$	- Load the contents of status register 4 (SCF_4 to SCF_7) into the accumulator (AC) and address Rx in the data memory (RAM). - The bits (SCF_4 to SCF_7) of status register 4 are set as follows: SCF_4 : Set when the divider has output an overflow signal. SCF_5 : Set when timer 1 has output an underflow signal. SCF_6 : Set when timer 2 has output an underflow signal. SCF_7 : Set when the SIO counter has output an overflow signal or when the SO4 terminal logic has been changed.	
Timer control instruction	MSTR X	0 1 1 1 0 1 1 0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$(Rx)_{1,0} \leftarrow$ TM OVF $(Rx)_2 \leftarrow$ INT-port DATA $(Rx)_3 \leftarrow$ RESET FLAG	Load into the accumulator (AC) and address Rx in the data memory (RAM) the contents of the timer 1 and timer 2 overflow flags, INT terminal logic, and the internal reset flag.	
	STM1 M, D	1 1 1 0 0 0 M_1 M_0 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	$MS \leftarrow M_0\sim M_1$ $TM1 \leftarrow D$ $D = 0\sim255$	Select the timer 1 (or timer 2) operation mode and start its operation. The operation mode selection data is specified by immediate data (M1M0) and the count value is set in timer 1 (or in timer 2) by D_0 to D_7 (0 to 255).	
	STM2 M, D	1 1 1 0 0 1 M_1 M_0 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	$MS \leftarrow M_0\sim M_1$ $TM2 \leftarrow D$ $D = 0\sim255$		
	MRTM1 M, X	0 0 1 0 0 0 M_1 M_0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$MS \leftarrow M_0\sim M_1$ $TM1 \leftarrow (Rx)$	Select the timer 1 (or timer 2) operation mode and start its operation. The operation mode selection data must be stored in advance at address Rx in the data memory (RAM). This Rx contents are then transferred to the timer and the timer starts operation.	
	MRTM2 M, X	0 0 1 0 0 1 M_1 M_0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$MS \leftarrow M_0\sim M_1$ $TM2 \leftarrow (Rx)$		

Instruction type	Mnemonic	Op code	Operations	Operations description	Affected flags
Timer control instruction	MT1R X	0 1 1 1 1 0 1 0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	(Rx)←AC, AC←TM1(L) Breg←TM1(H)	Transfer the contents of TM1 (L) to the accumulator (AC) and address Rx in the data memory (RAM). At the same time, copy the contents of TM1 (H) to the B register.	
	MT2R X	0 1 1 1 1 0 1 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	(Rx)←AC, AC←TM2(L) Breg←TM2(H)	Transfer the contents of TM2 (L) to the accumulator (AC) and address Rx in the data memory (RAM). At the same time, copy the contents of TM2 (H) to the B register.	
Serial counter control instruction	MSOR X	0 1 1 1 1 1 0 0 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	(Rx)←AC, AC←SIO(L) Breg←SIO(H)	Transfer the contents of SIO (L) to the accumulator (AC) and address Rx in the data memory (RAM). At the same time, copy the contents of SIO (H) to the B register.	
	MRSI X	0 1 1 0 1 0 1 0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	SIO(L)←(Rx), AC←(Rx) SIO(H)←Breg	Transfer the contents of address Rx in the data memory (RAM) to the accumulator (AC) and SIO (L). At the same time, copy the contents of the B register to the SIO (H).	
	MSCF X	0 1 1 1 0 1 1 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC←STS2 (Rx)←GC	Transfer the contents of status register 2 to the accumulator (AC) and address Rx in the data memory (RAM). Note that the contents of status register 2 are as follows: Bit 3 : ICF --- Set to "H" when the internal clock mode has been selected. Bit 2 : CPHSF --- Set to "H" when data is output synchronized with falling clock signal edge and data is input with rising clock signal edge. Bit 1 : SIOF --- Set to "H" when the serial counter needs to be selected. Bit 0 : CSTF --- Set to "H" when the serial counter is to be started. Set to "L" when the serial counter is now in operation.	
	SSCF D	1 1 1 0 1 0 1 1 0 0 0 0 D_3 D_2 D_1 D_0	STS2←D	Load immediate data into status register 2 (STS2).	
	MRSC X	0 1 1 0 1 0 0 0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	STS2←AC, AC←(Rx)	Transfer the contents at address Rx in the data memory (RAM) to the accumulator (AC) and status register 2 (STS2).	
Data transfer instruction	MRW W, X	0 0 1 1 0 W_2 W_1 W_0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC←(Rx) (Rw)←AC	Transfer the contents at address Rx in the data memory (RAM) to the accumulator (AC) and working register Rw.	
	MWR X, W	0 0 1 1 1 W_2 W_1 W_0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC←(Rw) (Rx)←AC	Transfer the contents of working register Rw to the accumulator (AC) and address Rx in the data memory (RAM).	
	LDA X	0 1 1 0 1 1 0 0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC←(Rx)	Transfer the contents of address Rx in the data memory (RAM) to the accumulator (AC).	
	STA X	0 1 1 1 1 1 1 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	(Rx)←AC	Transfer the contents of the accumulator (AC) to address Rx in the data memory (RAM).	
	LDS X, D	1 1 0 1 D_3 D_2 D_1 D_0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC→D D=0~15 (Rx)←AC	Load immediate data into address Rx in the data memory (RAM).	
	MRB X	0 0 1 0 1 1 1 0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Breg←(Rx)	Transfer the contents of address Rx in the data memory (RAM) to the B register.	
	MBR X	0 1 1 1 1 1 1 0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC←Breg (Rx)←AC	Transfer the contents of the B register to address Rx in the data memory (RAM).	
	IPS X	0 1 1 1 0 0 0 0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC←(P(S)) (Rx)←AC	Transfer the contents of input port S to the accumulator (AC) and address Rx in the data memory (RAM).	
	IPK X	0 1 1 1 0 0 0 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC←(P(K)) (Rx)←AC	Transfer the contents of input/output port K to the accumulator (AC) and address Rx in the data memory (RAM).	
	IPM X	0 1 1 1 0 0 1 0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC←(P(M)) (Rx)←AC	Transfer the contents of input/output port M to the accumulator (AC) and address Rx in the data memory (RAM).	
	IPP X	0 1 1 1 0 0 1 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC←(P(P)) (Rx)←AC	Transfer the contents of input/output port P to the accumulator (AC) and address Rx in the data memory (RAM).	
	IPSO X	0 1 1 1 0 1 0 0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC←(P(SO)) (Rx)←AC	Transfer the contents of input/output port SO to the accumulator (AC) and address Rx in the data memory (RAM).	
	IPA X	0 1 1 1 0 1 0 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC←(P(A)) (Rx)←AC	Transfer the contents of input/output port A to the accumulator (AC) and address Rx in the data memory (RAM).	
	WRT Y, X	0 0 0 0 Y_3 Y_2 Y_1 Y_0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	decoder←(Rx) LCD latch (L_Y)←decoder LCD latch (L_Y)←CF	Transfer the contents of address Rx in the data memory (RAM) to the LCD latch circuit (Ly) via the data decoder.	
	WRP Y, X	0 0 0 1 Y_3 Y_2 Y_1 Y_0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	LCD latch (L_Y)←(Rx) LCD latch (L_Y)←Breg	Transfer the contents of address Rx in the data memory (RAM) and the B register to the LCD latch circuit (Ly).	
	OPN X	0 0 1 0 1 0 0 0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	(P(N))←(Rx)	Transfer the contents of address Rx in the data memory (RAM) to output port N.	
	OPK X	0 0 1 0 1 0 0 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	(P(K))←(Rx)	Transfer the contents of address Rx in the data memory (RAM) to input/output port K.	
	OPM X	0 0 1 0 1 0 1 0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	(P(M))←(Rx)	Transfer the contents of address Rx in the data memory (RAM) to input/output port M.	
	OPP X	0 0 1 0 1 0 1 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	(P(P))←(Rx)	Transfer the contents of address Rx in the data memory (RAM) to input/output port P.	
	OPSO X	0 0 1 0 1 1 0 0 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	(P(SO))←(Rx)	Transfer the contnts of address Rx in the data memory (RAM) to input/output port SO.	
	OPA X	0 0 1 0 1 1 0 1 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	(P(A))←(Rx)	Transfer the contents of address Rx in the data memory (RAM) to input/output port A.	

Instruction type	Mnemonic	Op code	Operations	Operations description	Affected flags
Flag set/reset instruction	SF1 D	1 1 1 1 0 0 0 0 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Set or reset the flags specified by immediate data bits D_8 to D_0. SF1 / RF1 D_0 : Set the carry flag (CF). / --Reset the carry flag (CF). D_1 : Set the data pointer flag (DPF). / --Reset the data pointer flag (DPF). D_2 : Set the overflow time of the divider to 125ms(250ms) / --Set the overflow time of the divider to 500ms(1000ms) D_3 : Set the K port to the output mode. / --Set the K port to the input mode. D_4 : Set the M port to the output mode. / --Set the M port to the input mode. D_5 : Set the P port to the output mode. / --Set the P port to the input mode. D_6 : Set the SO port to the output mode. / --Set the SO port to the input mode. D_7 : Set the A port to the output mode. / --Set the A port to the input mode. Reset the timer/SIO prescaler. D_8 : No significant		DPF HRF3 CF
	RF1 D	1 1 1 1 0 0 1 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0			DPF HRF3 CF
	SF2 D	1 1 1 1 0 1 0 0 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Set or reset the flags specified by immediate data bits D_7 to D_0. SF2 / RF2 D_0 : Enable HALT mode release request signal from the INT terminal. / --Disable HALT mode release request signal from the INT terminal. D_1 : Set LCD strobe to 10H to 1FH. / --Set LCD strobe to 00H to 0FH. D_2 : Set the internal resistor (UP/DOWN) of the S input port to ON state. / --Set the internal resistor (UP/DOWN) of the S input port to OFF state. D_3 : Set the internal resistor (UP/DOWN) of the K input port to ON state. / --Set the internal resistor (UP/DOWN) of the K input port to OFF state. D_4 : Set the internal resistor (UP/DOWN) of the M input port to ON state. / --Set the internal resistor (UP/DOWN) of the M input port to OFF state. D_5 : Set the internal resistor (UP/DOWN) of the P input port to ON state. / --Set the internal resistor (UP/DOWN) of the P input port to OFF state. D_6 : Set the internal resistor (UP/DOWN) of the SO input port to ON state. / --Set the internal resistor (UP/DOWN) of the SO input port to OFF state. D_7 : Set the internal resistor (UP/DOWN) of the A input port to ON state. / --Set the internal resistor (UP/DOWN) of the A input port to OFF state.		
	RF2 D	1 1 1 1 0 1 1 0 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0			
	COMD D	1 1 1 1 0 0 0 0 D_4 D_3 D_2 D_1 D_0 0 0 0		Same as D_3 to D_7 of SF1 instruction.	
	CIMD D	1 1 1 1 0 0 1 0 D_4 D_3 D_2 D_1 D_0 0 0 0		Same as D_3 to D_7 of the RF1 instruction.	
	SPDF D	1 1 1 1 0 1 0 0 D_5 D_4 D_3 D_2 D_1 D_0 0 0		Same as D_2 to D_7 of the SF2 instruction.	
	RPDF D	1 1 1 1 0 1 1 0 D_5 D_4 D_3 D_2 D_1 D_0 0 0		Same as D_2 to D_7 of the RF2 instruction.	
	SSW D	1 1 1 0 1 0 0 0 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Set or reset the flags specified by immediate data bits D7 to D0. D_0 : Enable or disable HALT mode release request or interrupt request at the rising edge or falling edge of a signal from the S1 terminal. D_1 : Enable or disable HALT mode release request or interrupt request at the rising edge or falling edge of a signal from the S2 terminal. D_2 : Enable or disable HALT mode release request or interrupt request at the rising edge or falling edge of a signal from the S3 terminal. D_3 : Enable or disable HALT mode release request or interrupt request at the rising edge or falling edge of a signal from the S4 terminal. D_4 : Enable or disable HALT mode release request or interrupt request at the rising edge of a signal from the K port. D_5 : Enable or disable HALT mode release request or interrupt request at the falling edge of a signal from the K port. D_6 : Enable or disable the flag allowing input data to the S port to be loaded into the accumulator (AC) and address Rx in the data memory (RAM). D_7 : Set to "H" when setting to 2 milliseconds the operating frequency of the chattering prevention circuit of the S/K port. (D7 = "L": operating frequency => 7.8 milliseconds. Condition: input clock frequency = 32.768 kHz.)		
Other instructions	SR0PF D	1 1 1 0 1 0 0 1 0 0 0 0 0 0 D_1 D_0	ROM page ← D	Select ROM pages.	0PG
	SAS D	1 1 1 0 1 1 0 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Select the alarm signal waveforms for the N4 terminal according to immediate data (D_8 to D_0). If D_8 = 1, the alarm signal waveform selected by D_6 and D_7 is output to the N4 terminal (condition: input clock = 32.768 kHz).		
	NOP	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	No operation		

D8~D7	D0=1	D1=1	D2=1	D3=1	D4=1
Enable	32Hz	16Hz	8 Hz	4 Hz	2 Hz
D8~D7	D5=1	D6=D7=0	D6=1, D7=0	D6=0, D7=1	D6=1, D7=1
Enable	1 Hz	1 kHz	2 kHz	4 kHz	DC

LC5863H/64H Mnemonic MAP

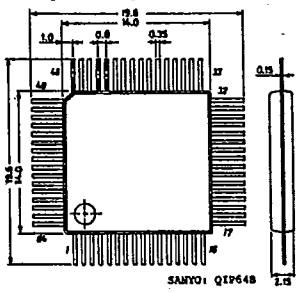


T-90-20

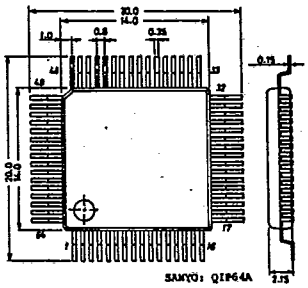
CASE OUTLINES OF 8/4-BIT MICROCOMPUTERS WITH LCD DRIVER

- All of Sanyo microcomputer case outlines are illustrated below.
- All dimensions are in mm, and dimensions which are not followed by min. or max. are represented by typical values.
- No marking is indicated.

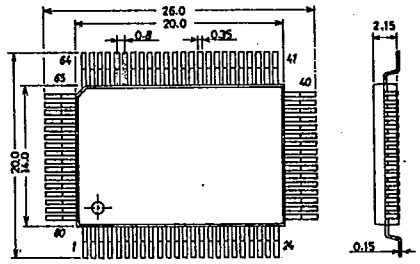
Case Outline—[3026B] unit:mm



Case Outline—[3057] unit:mm



Case Outline—[3044B] unit:mm



Case Outline—[3089] unit:mm