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TECHNICAL DATA**
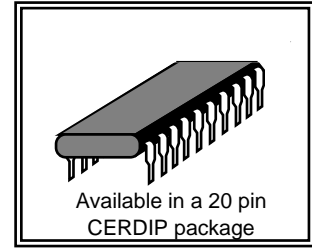
DSP56ADC16

Available in a 20 pin
CERDIP package

Technical Information
DSP56ADC16

16-bit Sigma-Delta Analog-to-Digital Converter

The DSP56ADC16 is a single chip, linear, 16-bit oversampling analog-to-digital (A/D) converter, providing output sample rates up to 100 KHz. Third order noise shaping sigma-delta technology is employed utilizing 64 times oversampling which yields 96 dB dynamic range and 90 dB signal-to-noise ratio for the signal bandwidths from 0 to 45.5 KHz with an in-band ripple of less than 0.001 dB. The DSP56ADC16 is an ideal choice for high performance digital audio systems, such as digital audio disks, tapes, and processors as well as voice-bandwidth communication and control applications. It does not require anti-aliasing filters and sample-and-hold circuitry because they are an inherent part of the sigma-delta technology. Due to the scalable design principles, the effective output sampling rate can be adjusted from 8 KHz to 100 KHz without losing specified characteristics. The DSP56ADC16 can easily be interfaced to the DSP56001/2 or other host processors using its flexible serial interface. An output is also provided before the final FIR decimation filter for applications requiring higher speed, lower group delay, and only 12-bit accuracy for AC levels. The DSP56ADC16 can also be used with an input multiplexer at a minimum output sampling interval of 15 μs in the comb filter output mode.

DSP56ADC16 Key Features

- 16-Bit Output Resolution (96 dB Typical Dynamic Range) at 100 KHz from the FIR Filter
- 12-Bit Output Resolution (72 dB Typical Dynamic Range) at 400 KHz from the Comb Filter
- 90 dB Signal-to-Noise Ratio (SNR)
- In-Band Ripple: < 0.001 dB
- Adjustable Output Sampling Rates: 8 KHz to 100 KHz (FIR FIlter)
                                                32 KHz to 400 KHz (Comb Filter)
- Maximum Input Sample Rate: 6.4 MHz
- Maximum Internal Clock Rate: 12.8 MHz
- Single +5 V ±10% Supply
- On-chip voltage reference
- 3.5 Volt p-p full-scale differential inputs
- Typical Power consumption: 300 mW at 100 KHz sampling rate
- 20-Pin CERDIP Package
- Single Chip
- Linear Phase Analog Front End and Internal Digital Filters
- Simple Serial Interface to Host Microprocessors
- No-glue Interface to DSP5600x/DSP561xx and Most Other General Purpose DSPs

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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INTERNAL ARCHITECTURE

The A/D converter is a key component in data acquisition systems, such as those found in digital audio systems, high-accuracy measurement systems, communications, and digital signal processing systems in general. High resolution A/D converters have typically used successive approximation techniques with complicated trimming/calibration or dual-ramp conversion techniques which require accurate comparators and expensive sample-and-hold (S/H) circuits to yield over 15 bits of accuracy. In addition, the anti-aliasing filter for these A/D converters generally sets severe limitations on the attainable signal-to-noise ratio and phase linearity.

The DSP56ADC16 uses an advanced third order sigma delta quantizer to implement an oversampled noise shaping A/D converter system on a single chip. By oversampling the input signal, the overall quantization noise spectrum expands well beyond the frequency band of interest. Third order noise shaping insures that this expanded noise spectrum contains very little noise power in the passband. The oversampled signal is lowpass filtered, effectively removing the out-of-band quantization noise. The lowpass filtering is then followed by decimation to reduce the output sample rate commensurate with the frequency band of interest and to increase the resolution. In the DSP56ADC16, the filtering and decimation are done in two steps to reduce digital filter complexity. Since the input signal is oversampled by a factor of 64, the need for a high order antialiasing filter can be eliminated.

The DSP56ADC16 consists of three major sections: 1) analog front end (AFE), 2) compensated decimation digital filters and 3) serial interface, as shown in Figure 1. The AFE consists primarily of three differential switched-capacitor linear integrators. These highly stable fully differential integrators perform the noise shaping function. The decimation digital filter section consists of a 16:1 decimation comb filter stage followed by a 4:1 decimation lowpass/compensation FIR filter stage which results in a total decimation ratio of 64:1. The frequency response of the decimation digital filters is described in the "**First and Second Stage Decimation Digital Filters**" section. The "**Serial Interface**" section provides serial communication to a host
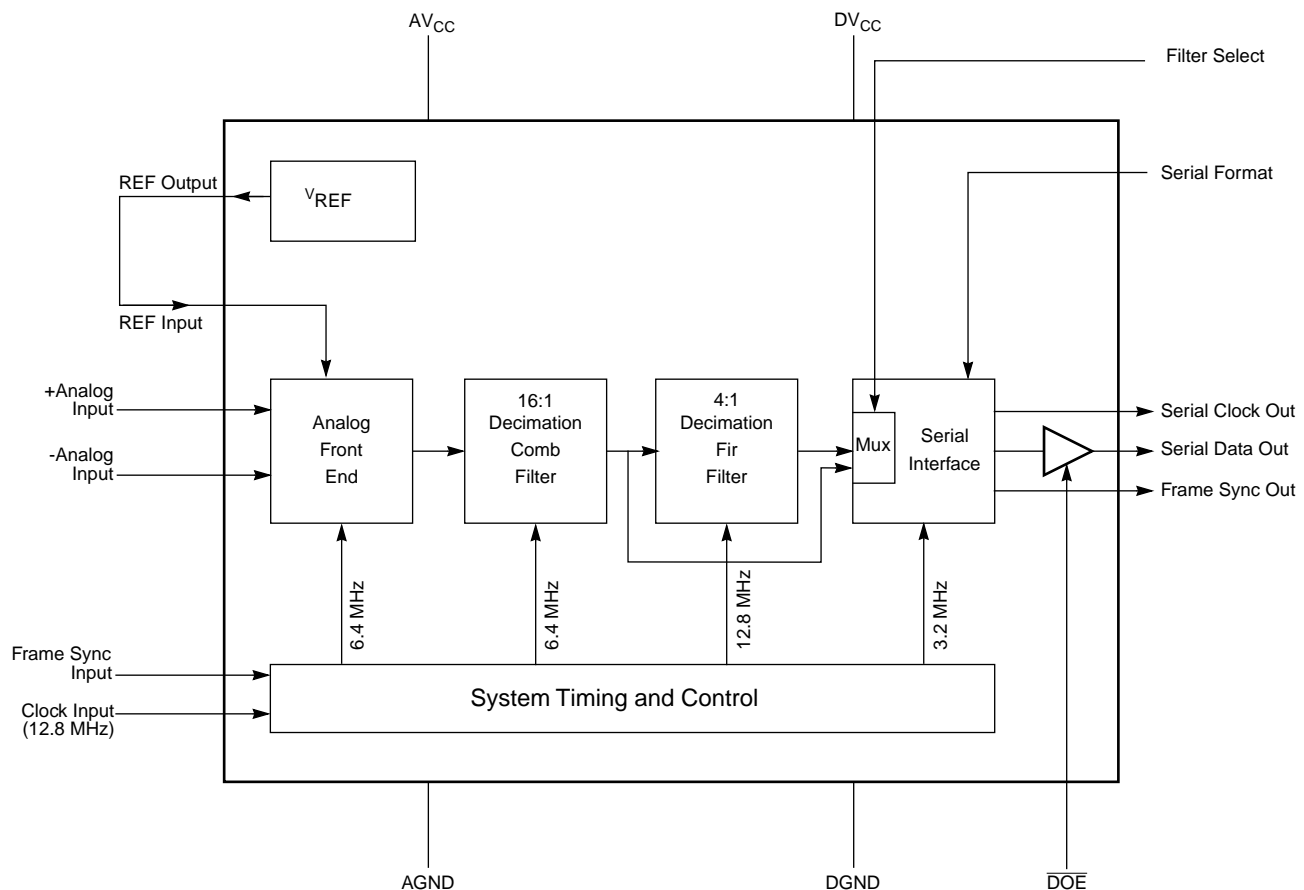

Figure 1. Internal Block Diagram

processor. This interface uses three dedicated pins — serial data output (SDO), frame sync output (FSO), and serial clock output (SCO). The serial interface format of operation is pin selectable. The timing diagrams for the serial interface are described in the "**AC Electrical Specifications**" section.

SIGNAL DESCRIPTION

The DSP56ADC16 is available in a 20-pin CERDIP package. The functional pin definitions and their mnemonics are listed below and shown in Figure 2.
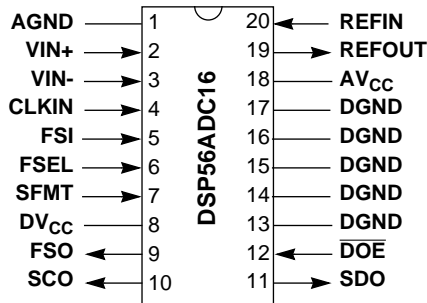
```
AGND ——————1      20 ◄——— REFIN
VIN+  ——————►2      19 ———► REFOUT
VIN-  ——————►3      18 ———— AV_CC
CLKIN ——————►4  D   17 ———— DGND
FSI   ——————►5  S   16 ———— DGND
FSEL  ——————►6  P   15 ———— DGND
SFMT  ——————►7  5   14 ———— DGND
DV_CC ——————8   6   13 ———— DGND
FSO   ◄——————9  A   12 ◄——— DOE
SCO   ◄——————10 D   11 ———► SDO
                C
                1
                6
```

Figure 2. DSP56ADC16 Pin Assignment

Clock Input (CLKIN)

This pin accepts the input clock for the DSP56ADC16. This TTL level compatible input accepts clock frequencies in the range of 1.0 to 12.8 MHz. The output sample rate is equal to the CLKIN frequency divided by 128.

Frame Sync Input (FSI)

This active high input is used to start or reset the serial data output and synchronize internal circuits. It is not a start conversion pulse since the DSP56ADC16 is always converting at a rate of CLKIN/128. FSI is sampled on the falling edge of CLKIN (see the timing diagram shown in Figure 21). When this signal goes high, the DSP56ADC16 will begin transmitting bits via the serial data out (SDO) pin. Frame sync input is an optional input signal. If the FSI pin is grounded, frame sync's will be internally generated. The purpose of FSI is to allow external control of the A/D conversion process phasing. FSI should be a periodic signal occurring every 16 SCO clock periods in the comb filter output mode and every 32 SCO clock periods in the FIR filter output mode. In all cases FSI must be synchronized to CLKIN as defined in the timing specification. FSI allows multiple DSP56ADC16's to be synchronized using a common frame sync source. A common CLKIN signal is required when using a common frame sync signal with multiple DSP56ADC16s.

Analog + Input (V_{IN}^+)

This pin is the A/D converter analog non-inverting input. If an input anti-aliasing filter is used prior to the V_{IN} inputs, high quality polystyrene or equivalent capacitors must be used in order to meet the published THD specification. See the connection diagram example in Figure 7 for a typical single pole input filter. The maximum peak-to-peak input signal is a function of the reference input voltage, V_{refin}, which is expressed as

Maximum input range = 2 * V_{refin} - 0.5 Volts p-p

The constant 0.5 Vp-p in the equation above is used for internal dither circuitry.

Analog - Input (V_{IN}^-)

This pin is the A/D converter analog inverting input with the same characteristics as VIN^+.

Reference Input (REFIN)

This pin is the analog reference voltage (V_{refin}) applied to this pin sets the analog input range. Its magnitude sets both the positive and negative full-scale range. The maximum input is +2.0 volts. Since this input is extremely sensitive to induced noise, reference input decoupling is suggested to achieve the maximum performance as shown in Figures 7 and 15. Failure to decouple may result in a degradation of the SNR. The output of the DSP56ADC16 is

$$\frac{V_{in}^+ - V_{in}^-}{V_{refin}}$$

Reference Output (REFOUT)

This pin is the on-board reference voltage output (V_{refout}) of +2.0 volts when using a +5.0 volt supply. This pin should be connected to REFIN when an external voltage reference is not used. When REFOUT is loaded by REFIN as shown in Figures 15 and 16, the value V_{refout} is

$$V_{refout} = \frac{2*AV_{CC}}{5}$$

Serial Clock Output (SCO)

This pin provides the serial bit clock for the SDO port. When the FIR filter output is selected by setting FSEL= 0, the rate of this output is CLKIN divided by

four; when the comb filter output is selected by setting FSEL = 1, the rate of this output is CLKIN divided by two. See Figures 22 and 24 for more details.

Serial Data Output (SDO)

A 16-bit serial data stream is output on the SDO pin once per frame sync output cycle. This data changes synchronously with the serial clock out (SCO) pin. The format used is fractional 2's complement transmitted most-significant-bit first. See Figures 22 and 24 for timing details.

Serial Format (SFMT)

This pin selects the formats of the FSO and SCO when the FIR filter output is selected by setting FSEL=0. The two formats of operation are shown in Figure 22.

Frame Sync Output (FSO)

This output is used to indicate the beginning of serial word transmission on the SDO pin. The shape and timing of the frame sync output pulse are controlled by the SFMT pin. Refer to Figures 22 and 24 for timing details of FSO.

Analog Vcc Supply (AVCC)

This pin is the positive analog power supply (+5 volts ±10%) for the analog integrator section.

NOTE

Analog Vcc and digital Vcc should be decoupled with respect to AGND and DGND, respectively, to obtain the published specifications. This decoupling is intended to isolate digital noise from the analog section. Decoupling capacitors should be as close as possible to their respective analog and digital supply pins.

Digital Vcc supply (DVCC)

This pin is the positive digital power supply (+5 volts ±10%) for digital internal circuitry and pin drivers (see AVCC).

Analog Ground (AGND)

This pin is the analog ground return for the analog front end. This pin is NOT internally connected to digital ground (DGND).

Digital Ground (DGND)

This pin is the ground connection for digital internal circuitry and pin drivers.

Filter Select (FSEL)

This input allows selection of the FIR filter output or the comb filter output. When FSEL is low, the SDO pin will deliver the final lowpass/compensation FIR filter output. When FSEL is high, the SDO will deliver the comb filter output at a four times faster output sample rate with a two times faster clock rate than the FIR filter output and the SFMT pin is disabled such that SFMT=0 as shown in Figure 24. (also see SCO in this section and Figure 22).

Data Output Enable ($\overline{\text{DOE}}$)

Serial data output three-state control pin. When DOE bar is asserted (low), the SDO will be active. When DOE bar is deasserted (high), the SDO will go to a high impedance state. This can be used for multiplexing several A/D converters into one host serial input. This pin is an asynchronous input and operates independently of input or output clocks (see Figure 25).
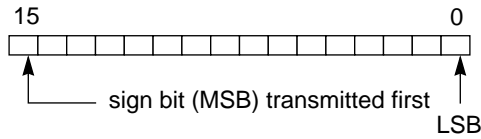
INPUT/OUTPUT CLOCKS AND CONTROL

The DSP56ADC16 output sample rate is defined by a combination of the CLKIN frequency and the output filter selected as determined by the FSEL pin. When FSEL=0 the FIR filter is selected and the output sample rate is equal to CLKIN divided by 128. When FSEL=1 the comb section is selected, the decimation ratio is changed to 16:1 and the output sample rate is equal to CLKIN divided by 32. The input sample rate is always the CLKIN frequency divided by two. In normal mode (FSEL=0), the clock rate of the SCO is defined as the CLKIN frequency divided by four, giving a maximum serial clock output of 3.2 MHz as shown in Figure 22. However, when the comb filter output is selected (FSEL=1), the rate is changed to the CLKIN frequency divided by two which makes the maximum rate of 6.4 MHz as shown in Figure 24. The timing relationships among CLKIN, FSI and SCO are detailed in the "**AC Electrical Specifications**" section Figures 21 through 23 for when the filter selection (FSEL) pin is set to 0 selecting the FIR filter output (see FSEL in the "**Signal Description**" section).

SERIAL INTERFACE

The DSP56ADC16 has three output pins for the serial interface: 1) serial data out (SDO), 2) frame sync out (FSO), and 3) serial clock out (SCO). The corresponding internal block diagram is shown in Figure 3. The serial port can interface with general purpose digital signal processors such as the DSP5600x,

DSP561xx, NEC772x, TMS320Cxx and DSP16x without additional interface circuitry. The format of the fractional data output from the A/D converter is MSB first, 16-bit serial and two's complement. The serial data format for interfaces is defined as:

15   0

└─── sign bit (MSB) transmitted first
                                  LSB

The Serial Format (SFMT) pin selects between a one clock wide high-true frame sync pulse and a one data word wide low-true frame sync pulse as shown in Figure 22.

FIRST AND SECOND STAGE DECIMATION

The first stage comb filter provides initial filtering of the quantized output from the analog front end as well as decimation of the input sample rate by a factor of 16:1. The z-domain transfer function of this stage can be expressed as:

$$H(z) = \frac{[1 - z^{-16}]^4}{[1 - z^{-1}]^4}$$

The frequency domain (in Hz) equivalent of the transfer function is

$$\bar{H}(f) = \left[\frac{1}{16} \frac{\sin(16\pi fT)}{\sin(\pi fT)} \right]^4$$

where

$$T = \frac{1}{f_s}$$

and f_s is the input sampling rate for the AFE (maximum 6.4 MHz).

Figure 4 shows the magnitude response of the comb filter section. Since the comb filter has a non-flat lowpass like frequency response in the passband region, the following second stage FIR filter should compensate for the passband droop as well as providing the final sharp cutoff required for 16 bits of dynamic range. Figures 5 and 6 illustrate the frequency responses of the lowpass FIR filter and the compensation, respectively. The 255-tap FIR filter coefficients are designed for a lowpass filter with 9% transition band and passband amplitude compensation whose characteristics are — passband cutoff frequency: 45.5 KHz, stopband cutoff frequency: 50 KHz, passband ripple: 0.001 dB and a stopband ripple: -96 dB when the chip is operated at a CLKIN frequency of 12.8 MHz. The 16-bit output of the first-stage comb filter is used as the input to the second-stage FIR filter. This filter removes the out-of-band noise components and also acts as the system anti-aliasing filter. Since the in-band signal has been shaped by the third-order noise-shaping integrators, the signal-to-noise ratio achieved is more than 90 dB. It is important to note
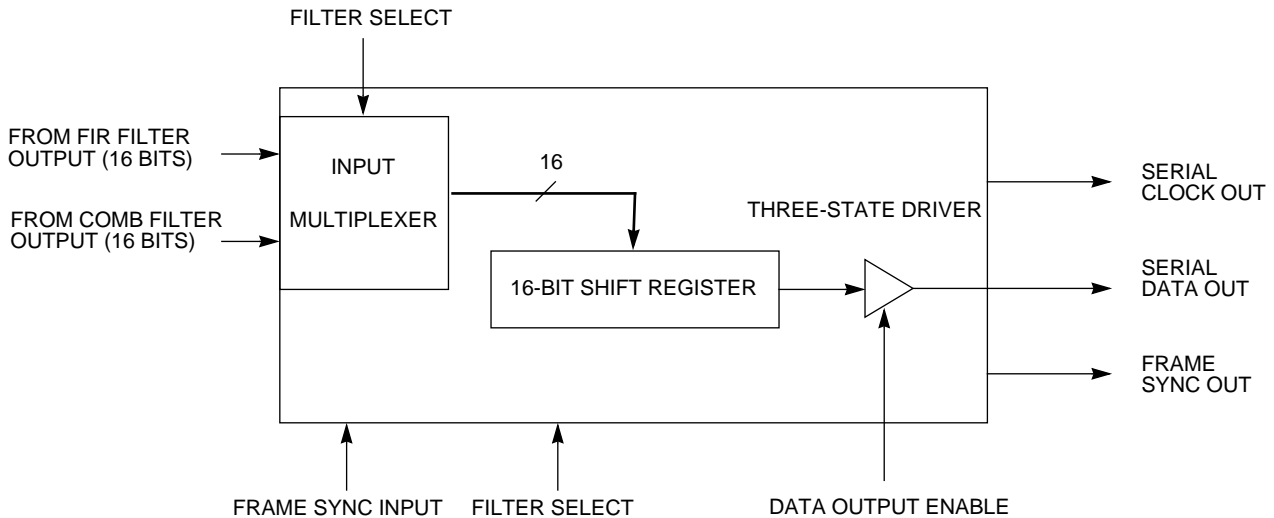

Figure 3. Block Diagram of Serial Interface

that the passband and stopband frequencies of both the comb and FIR filters scale linearly with the CLKIN frequency.
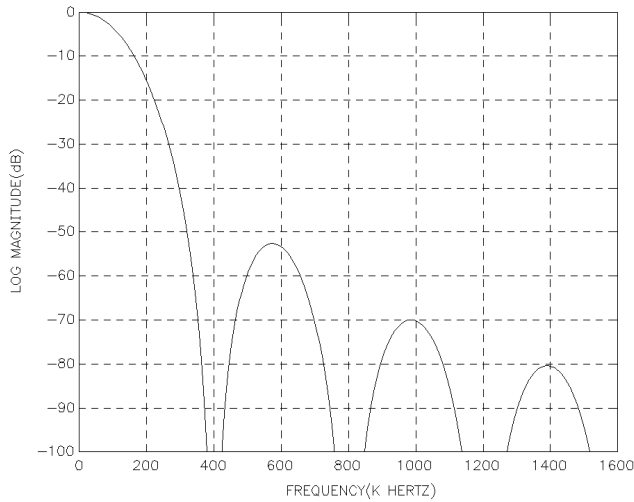

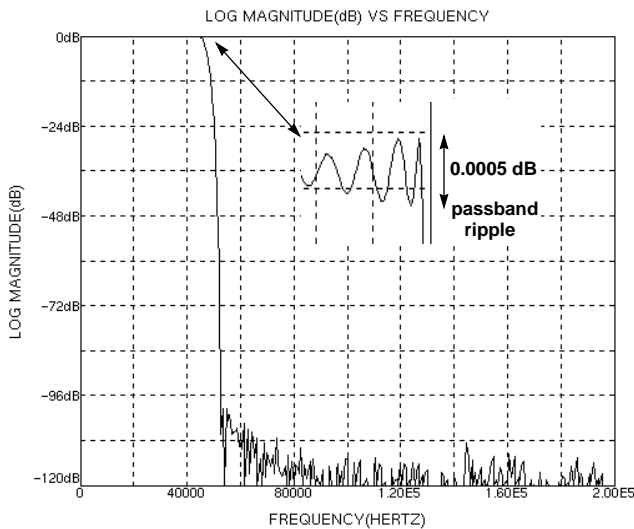**Figure 4. Magnitude Response of Comb Filter (CLKIN = 12.8 MHz)**

Figure 5. Magnitude Response of Lowpass FIR Filter

TECHNOLOGY COMPARISONS

The 38-bit FIR filter accumulator is convergently rounded for 16-bit output to the "**Serial Interface**" section. This provides 90 dB signal-to-noise ratio (SNR), and 96 dB dynamic range in the 0 to 45.5 KHz band which makes this device suitable for high performance digital audio applications. Three techniques have traditionally been used in A/D converter implementation: successive approximation (SA), integrating, and flash. They are implemented using the Nyquist sampled data criterion (set a minimum of

Figure 6. Magnitude Response of FIR Filter with Compensation

twice the signal frequency) instead of the oversampled method used by the sigma-delta technology.

Successive approximation A/D converters compare the unknown input with sums of accurately known fractions of the reference voltage in the successive approximation register (SAR). Starting with the largest fraction, each sum is sequentially compared to the input. If the sum is larger than the input, that fractional voltage is deleted from the sum and the next smaller fraction is added. This process is repeated until all available fractions have been either added or rejected from the sum. The on-chip D/A converter used to generate the sum of fractions must be very accurate and may require external trimming. The settling time for 16 approximations in succession for 16-bit performance must be less than 10 μs for a 100 KHz sample rate. Allowing 5 μs to acquire the signal to the specified linear error, 5 μs is left for the 16-bit digitization process which yields approximately 0.3 μs for each bit.

Integrating A/D converters count pulses for a period proportional to the input. Dual slope integrating converters count the period required for the integral of the reference to equal the average value of the input over a fixed period of time. As with SA, external trimming is required.

Flash A/D converters give simple and fast conversions in low resolution and high speed applications. This method requires only one step in determining the input voltage, a series of comparators test the input signal against a set of voltage thresholds established by a ladder network. Digital logic is then employed to convert the comparator outputs to a binary number.

To operate in such a fast manner $2^{B}-1$ comparators are required, where B denotes the number of bits of resolution. For 16-bit resolution, therefore, 65,535 comparators would be needed and a significant amount of priority encoding logic would be required to achieve performance comparable to Sigma-Delta converters.

Sigma Delta A/D converters use a low resolution A/D converter (one bit quantizer) in a feedback configuration. The high resolution (96 dB SNR) is achieved by the noise-shaper (third order for the DSP56ADC16). The noise transfer function is essentially a high pass filter so that the noise is shifted to higher, out-of-band frequencies where it is then filtered out. The input sampling rate for sigma-delta modulation is much higher (64 times for the DSP56ADC16) than the rate for the other three techniques for the same bandwidth. Because of the high sampling rate and the low precision A/D conversion used on the front end of a sigma-delta system, a sample and hold circuit is not needed. Since the sampling rate is much higher, the anti-aliasing filter is not required or a simple one-pole

RC filter can be used to attenuate a high frequency input signal.

The SA, integrating and flash techniques require extremely high performance analog anti-aliasing filtering and precise sample-and-hold (SAH) circuits to ensure 16-bit accuracy and 100 KHz sample rate. The anti-aliasing filter, therefore, has to be a very steep "brick wall" filter outside the passband. A 30-pole Bessel-approximated IIR filter is necessary to obtain almost linear-phase and less than 0.0001 ripple over the entire passband, 96 dB stop band attenuation and fast transition between passband and stop band, which is impractical. Also, the allowable aperture jitter of the sample-and-hold circuit is only 48.6 ps which is very expensive to make.

In contrast, sigma-delta modulation based A/D technology can meet the performance goals of 16-bit resolution and 100 KHz sample rate with moderate cost. A tutorial of sigma-delta technology can be found in the Motorola Digital Signal Processing Operation Application Report, **APR8/D**, entitled "**Principles of Sigma-Delta Modulation for Analog-to-Digital**
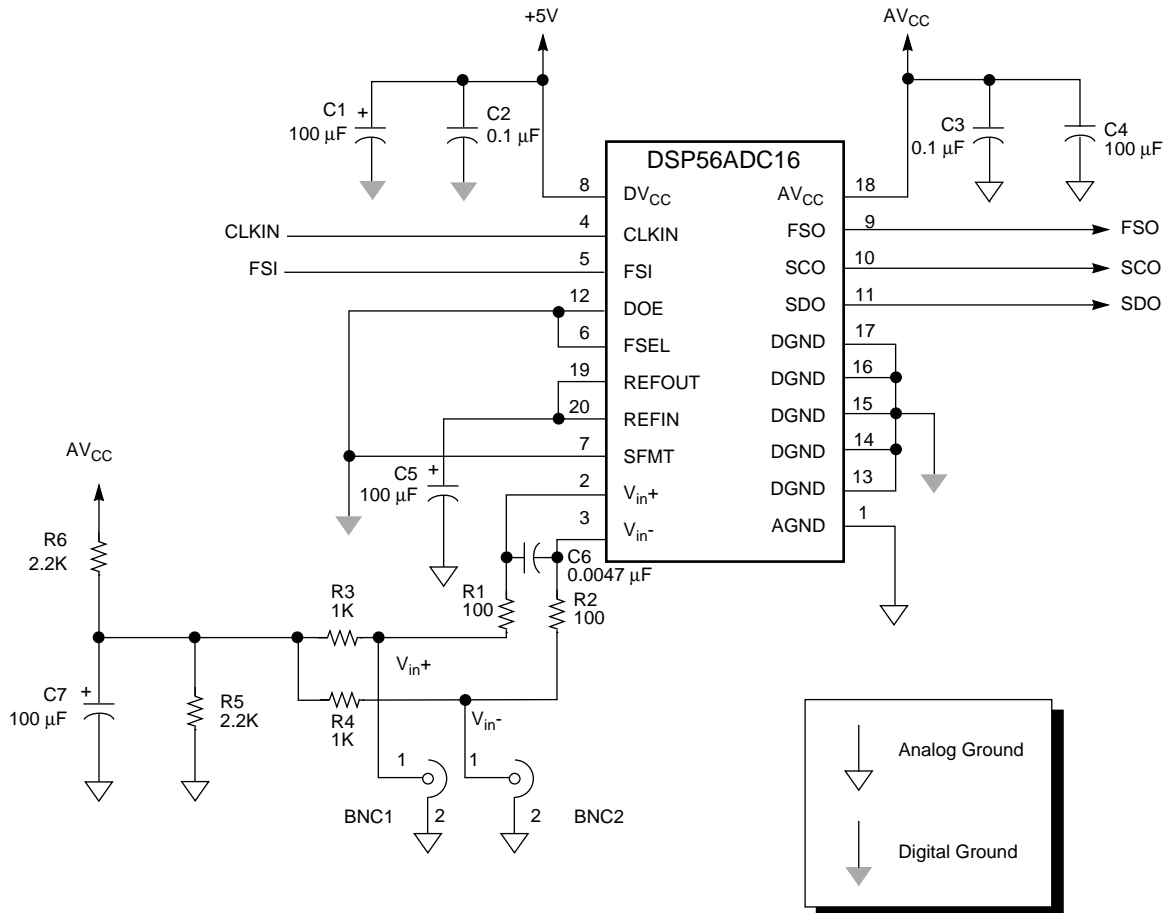

Figure 7. Functional Test Circuit

Converters" which can be requested from:

Motorola Literature Distribution
P.O. Box 20912
Phoenix, Arizona 85036

or from the other Motorola literature distribution centers listed on the back cover of this data sheet.

PERFORMANCE EVALUATIONS

Figure 7 shows the input circuitry used for testing signal-to-noise and signal-to-THD ratios. A low distortion (>96 dB SNR) signal generator is applied differentially to the BNC inputs and an FFT with the Blackman-Harris window is performed to measure the noise and distortion. AC characteristics of digital outputs, FSO, SDO, and SCO, are measured while connected to one standard TTL load.

Figure 8 shows the spectral purity of the DSP56ADC16 with a 10 KHz, full scale, sine-wave input when the output sampling rate is 50K samples per second. Since the 1024-point FFT has 512 spectral bins up to Nyquist frequency, the typical noise floor and the harmonic distortion can be measured by summing the power of corresponding bins; this gives -90 dB and -88 dB, respectively. The typical spectral plot for the comb filter output is shown in Figure 9.

Figure 8. Typical Spectrum of FIR Filter Output (512 Bins of 1024 FFT)

Figure10 illustrates the differential non-linearity (DNL) plots of the DSP56ADC16. It has been shown that Sigma-Delta converters are inherently linear and do not suffer from appreciable DNL or missing codes. The plot shows the distributions of 2^{16} = 65,536 possible codes for the 16-bit converter. The distribution of DNL codes are within ± 0.5 LSB.

Measurements of the group delay and settling time due to the internal propagation delay and linear-phase filter operation may be useful for multiplexed applications. Figures 11 and 12 illustrate the rectangular pulse responses of the comb filter output and FIR filter output, respectively, while Figures 13 and 14 are for a sine wave input response. Note that the output response includes not only the internal delays of the DSP56ADC16, but also the measurement delays for these plots such as data transfer time and D/A conversion time of 2.5 μs and 3.0 μs, respectively.
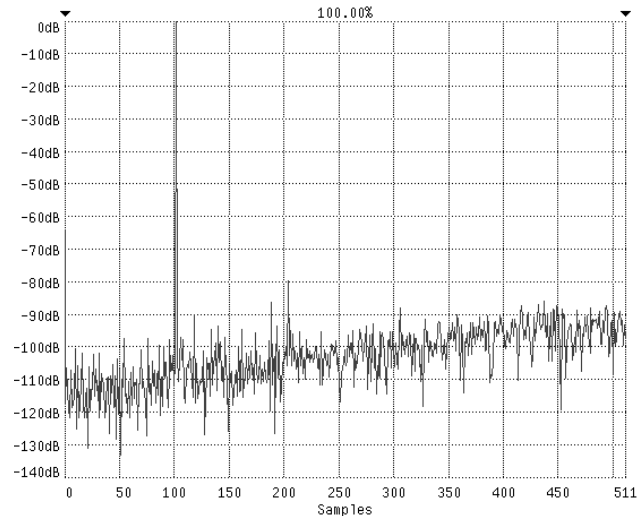

Figure 9. Typical Spectrum of Comb Filter Output (512 Bins of 1024 FFT)
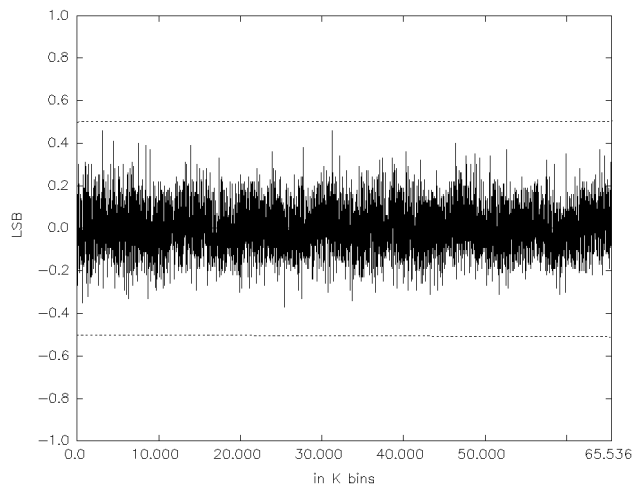

Figure 10. Typical Differential Nonlinearity (DNL) Plot

The DSP56ADC16 can also be used with an input

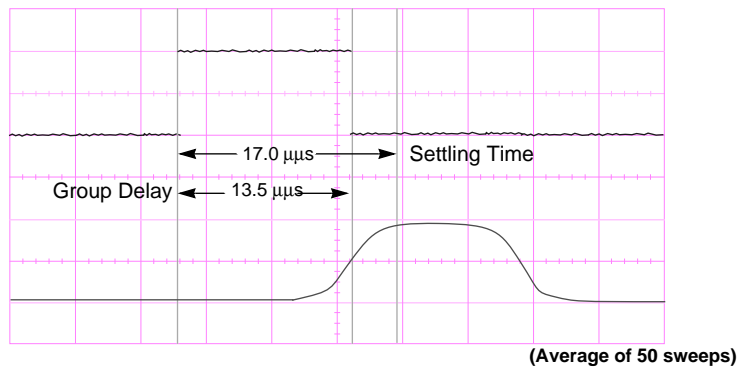**(Average of 50 sweeps)**

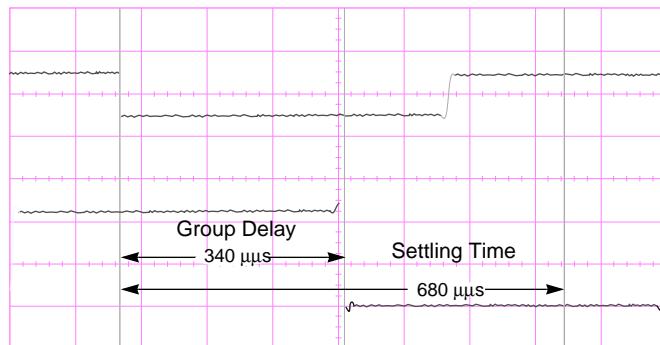**Figure 11. Typical Measured Group Delay and Settling Time of Comb Filter Output (CLKIN = 12.8 MHz)**

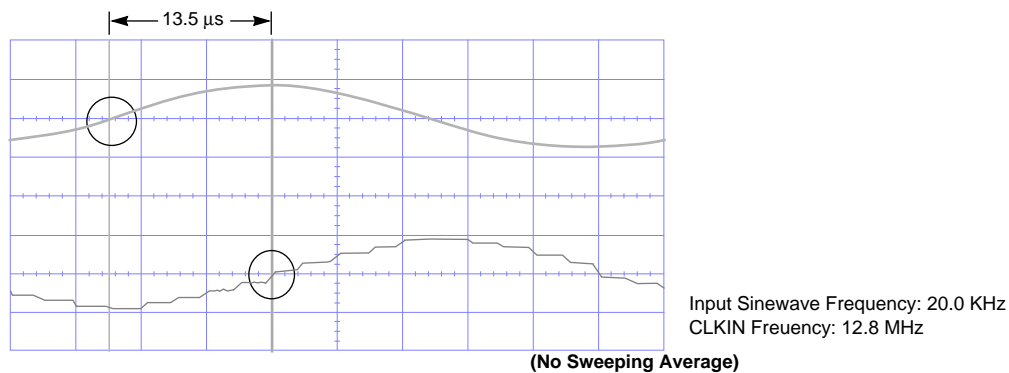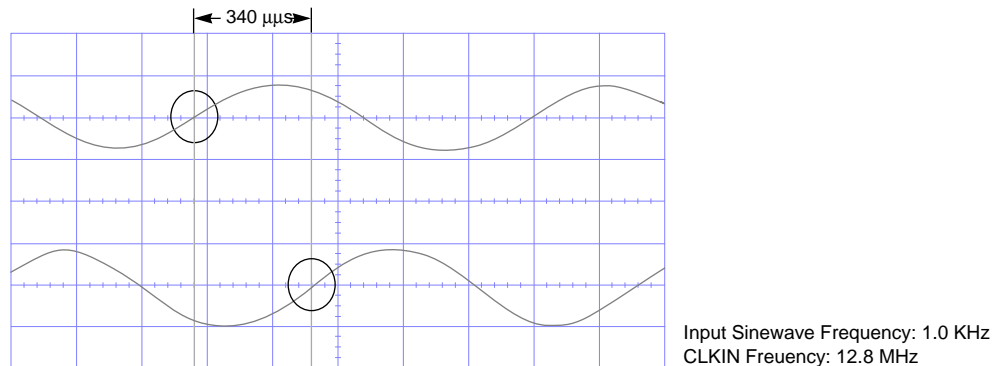**Figure 12. Typical Measured Group Delay and Settling Time of FIR Filter Output (CLKIN = 12.8 MHz)**

Input Sinewave Frequency: 20.0 KHz
CLKIN Freuency: 12.8 MHz

(No Sweeping Average)

Figure 13. Typical Measured Group Delay of Comb Filter Output

Input Sinewave Frequency: 1.0 KHz
CLKIN Freuency: 12.8 MHz

Figure 14. Typical Measured Group Delay of FIR Filter Output

multiplexer when the comb filter output is selected by setting FSEL=1 (see the **Signal Descriptions** section). The minimum multiplex intervals which depend on the settling time as shown in Figure 11, can be given by

$$\tau_{mux} \geq \frac{162}{f_{clk}} \;;$$

excluding the time required to shift the data out from the serial interface, and

$$\tau_{mux}^{S} \geq \frac{194}{f_{clk}} \;;$$

including the time required to shift the data out from the serial interface.

These expressions are based on theoretical analysis. However, there are practical aspects which need to be considered. First, the multiplex interval must be a multiple of 32 clock periods (i.e., the comb filter output rate). If the FSI and the multiplexer can be perfectly synchronized, this results in the multiplex intervals of $\tau_{mux} \geq 5T_s$ and $\tau_{mux}^{S} \geq 6T_s$ where T_s equals 32 t_{clk} (output sample interval). If the FSI and the multiplexer are not synchronized, there can be one sample of time uncertainty so that $\tau_{mux} \geq 6T_s$ and $\tau_{mux}^{S} \geq 7T_s$. If f_{clk} = 12.8 MHz, the minimum multiplex intervals, τ_{mux} and τ_{mux}^{S}, are 15 μs and 17.5 μs, respectively. These results were verified by synchronizing a square wave input to the DSP56ADC16 and collecting and analyzing buffers of 32 data samples. In addition to these synchronization aspects, the following must be considered: 1) the response time of the multiplexer itself, 2) rolloff caused by any external anti-aliasing filter, and 3) if a DAC is used to display the output data, its response characteristic must be considered

SINGLE-ENDED TO DIFFERENTIAL INPUTS

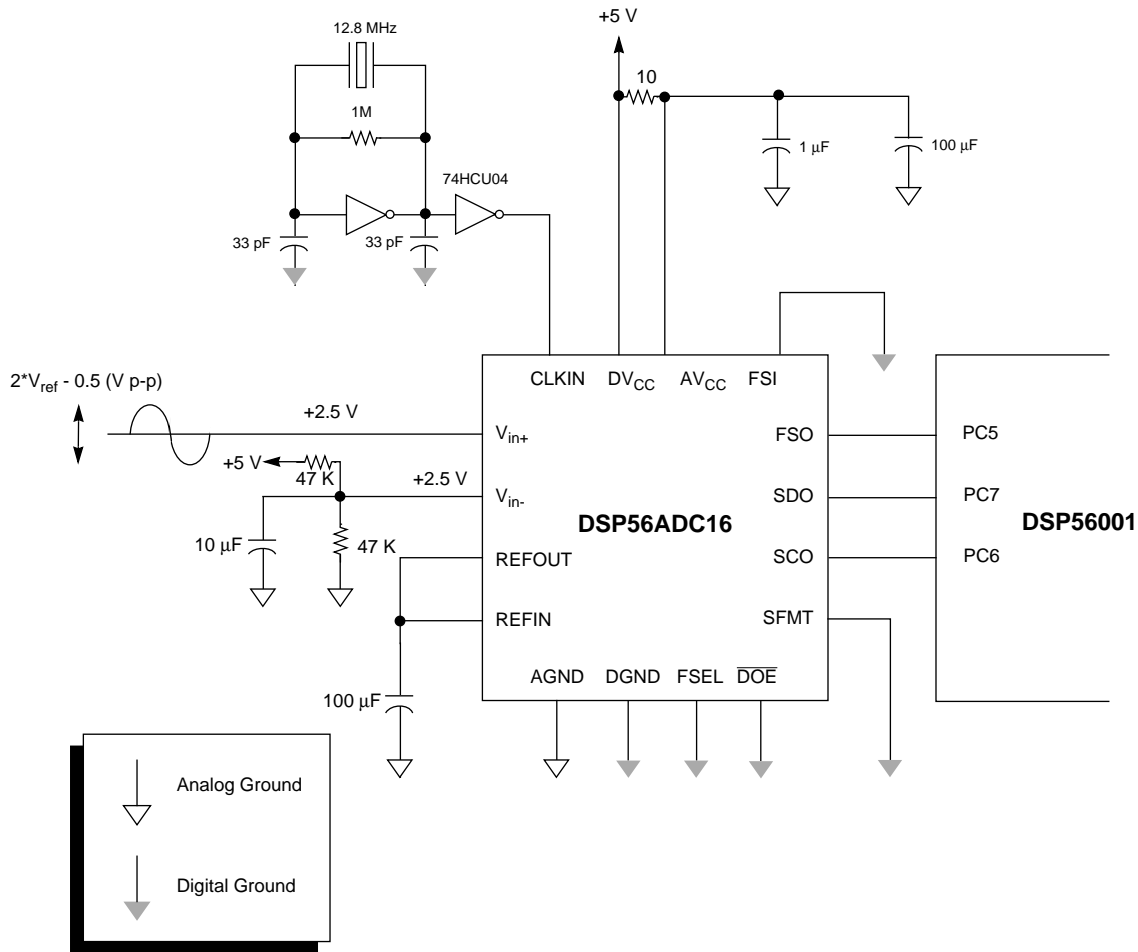A general system connection diagram for a single

Figure 15. Single Ended Mode Input Circuit

ended input signal is shown in Figure 15, while Figure 16 illustrates the schematic diagram for multiplexing two DSP56ADC16's with the DSP56001. Figure 17 shows the system interface diagrams for popular general purpose digital signal processors.

Although a differential input is recommended to obtain the specified performance, the DSP56ADC16 can be used with a single-ended input system with a slight SNR performance degradation of 3-4 dB. For better performance, the recommended conversion circuit diagram from single-ended input to differential input is illustrated in Figure 18. Using this diagram, the analog input voltage range can be conditioned to utilize the maximum dynamic range of the DSP56ADC16.

Two DSP56ADC16's can be multiplexed on a single serial port. Note in Figure 23 that there are 32 SCO cycles in one FSO cycle. The SDO pin outputs valid
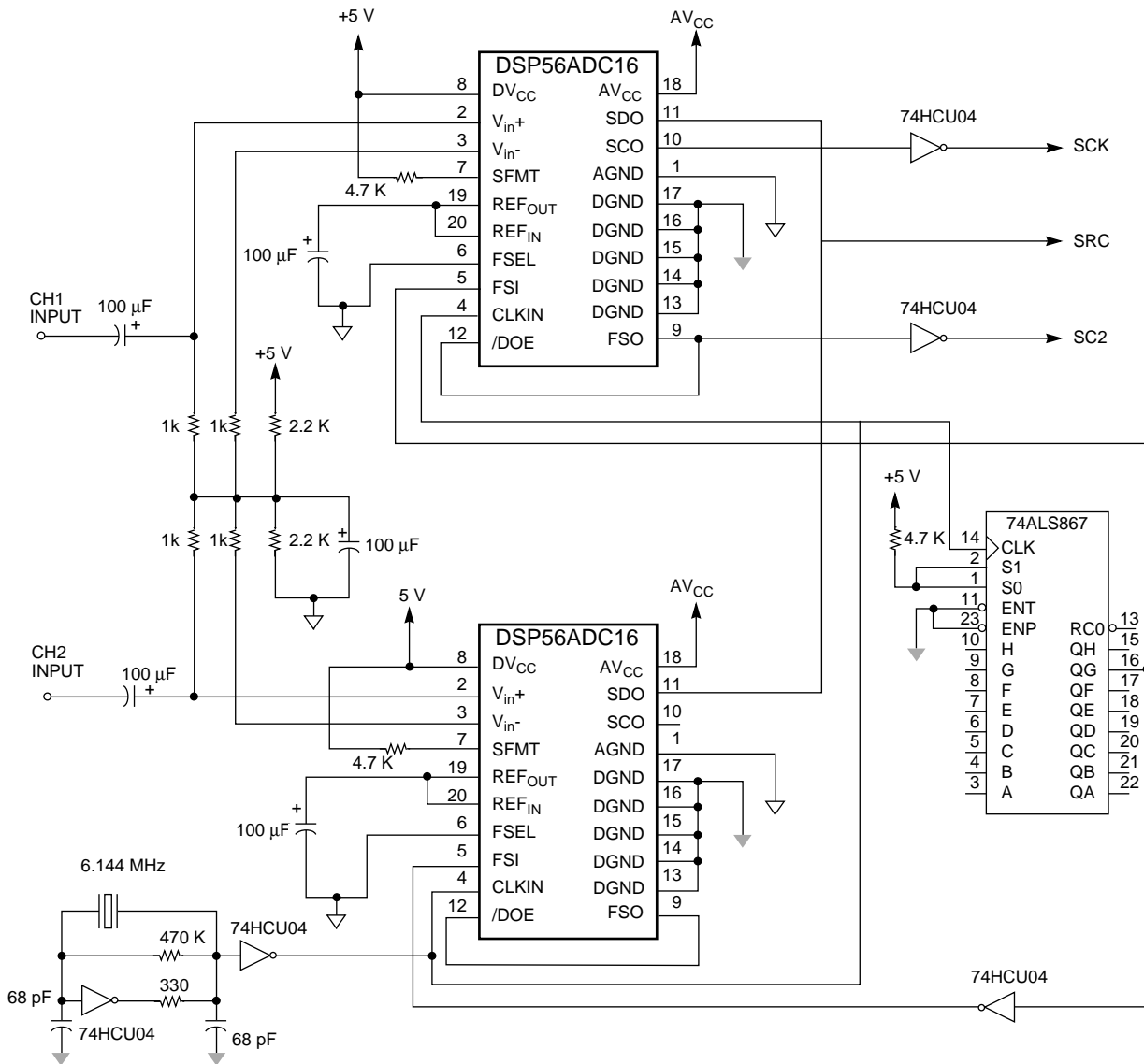

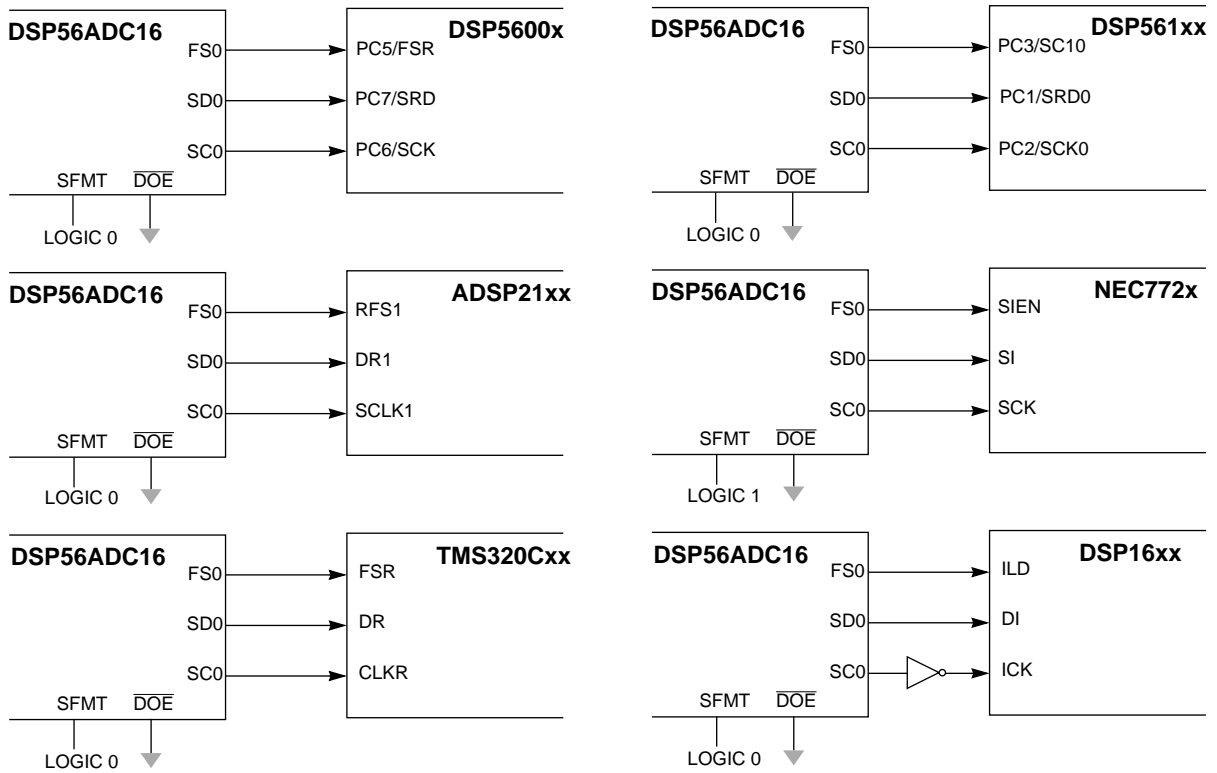**Figure 16. Schematic Diagram for Multiplexing Two DSP56ADC16s with the DSP56001**
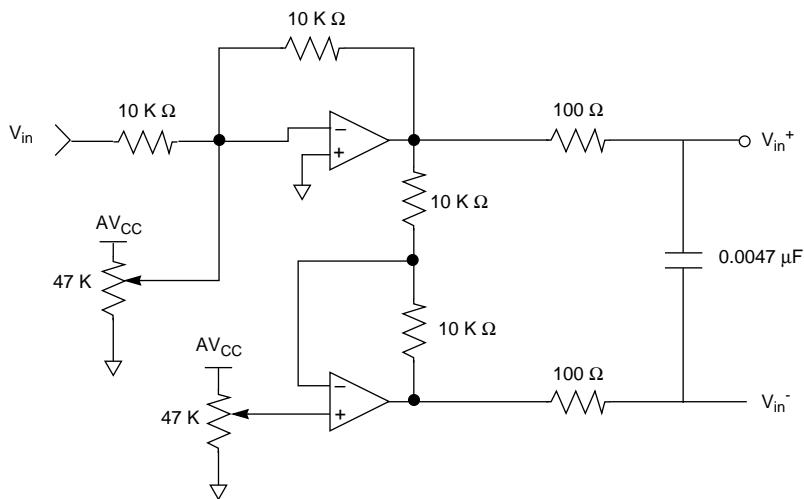
Figure 17. Connection Diagram Examples

Figure 18. Single Ended to Differential Analog Input Diagram

data for the first 16 SCO cycles and then the next 16 SCO cycles are zero.

SYNCHRONIZING TWO CHANNELS

For an application where the two converters must synchronously be sampled, two 8-bit shift registers (or one 16-bit shift register) clocked by the SCO, may be connected to the second converter SDO pin to delay 16 SCO cycles as shown in Figure 19. A single FSI pulse from the octal counter (74ASL867) is used for both DSP56ADC16s to make sure that the FSIs for both chips are occurring at the same time. The outputs of the first DSP56ADC16 and the 16-bit shift register can be combined by one OR gate to yield one serial output to the SSI port. When more than two channels have to be sampled synchronously, the memory mapped addressing and direct read from the data bus scheme can be used as shown in Figure 20.

Power Dissipation

The power dissipation of the DSP56ADC16 is a function of CLKIN. The DSP56ADC16 analog section typically consumes 100 mW. This value is independent of the clock frequency. However, the power consumption of the remaining circuitry in the DSP56ADC16 is linear with the clock frequency. The following equations show some examples of power dissipation with respect to the CLKIN values.

$$12.8 \text{ MHz} \rightarrow 100 + 200 = 300 \text{ mW}$$
$$6.4 \text{ MHz} \rightarrow 100 + 200/2 = 200 \text{ mW}$$
$$1.0 \text{ MHz} \rightarrow 100 + 200/12.8 = 116 \text{ mW}$$

INPUT IMPEDANCES

The analog input impedance, Z_{in}, and the minimum reference input impedance, Z_{ref}, can be computed by following equations:

$$Z_{in} = \frac{10^{12}}{3f_{clk}}$$

$$Z_{ref} \geq \frac{10^{12}}{2.5f_{clk}}$$

where f_{clk} denotes the input clock rate. Table 1 shows the input impedances for selected input clock rates.

Table 1: Analog and Reference Input Impedance

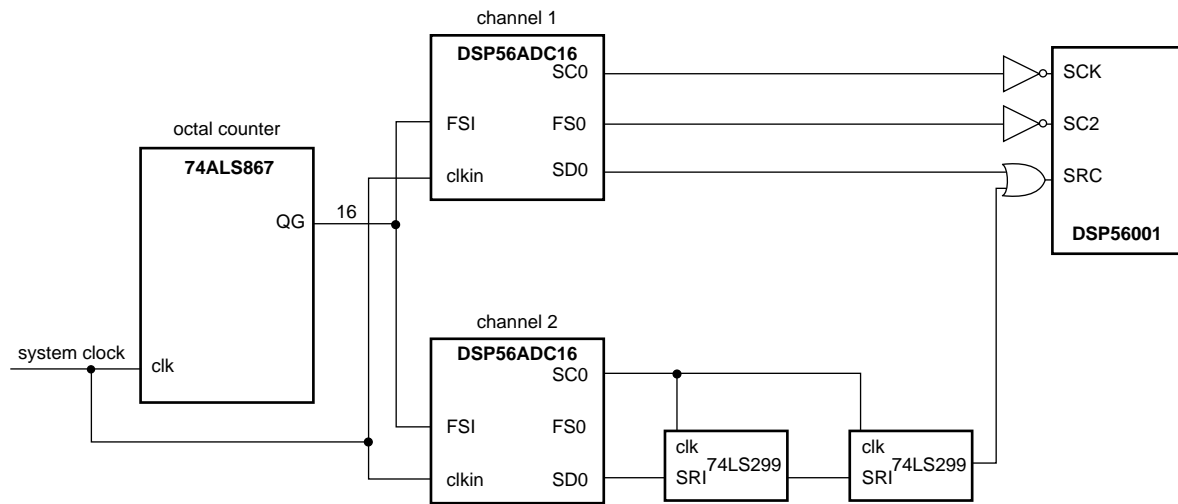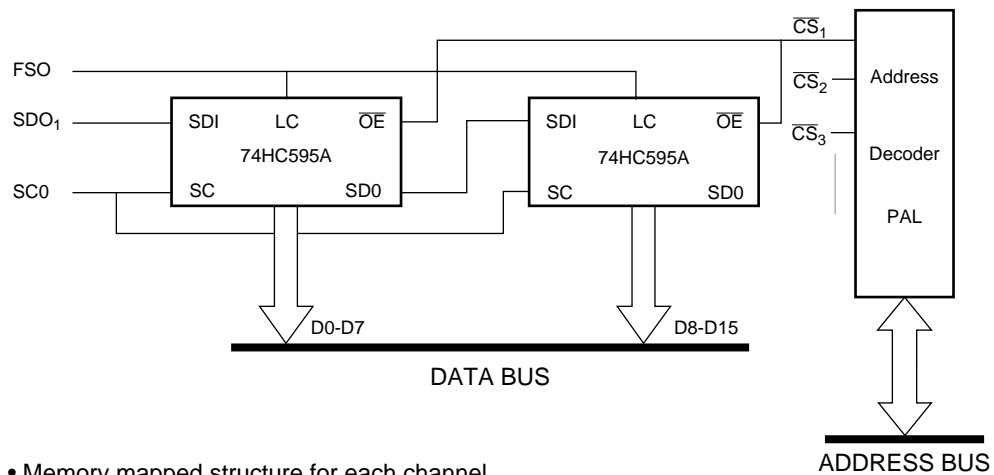| Input Clock Rate (MHz)	Output Sample Rate (KHz)	Analog Input Impedance (KΩ)	Minimum Reference Input Impedance (KΩ)
12.8	100.0	26.0	31.3
6.4	50.0	52.0	62.5
6.144	48.0	54.3	65.1
5.6448	44.1	59.0	70.9
1.024	8.0	325.5	390.6

Figure 19. Synchronized Two Channel Input Sampling for Stereo Applications

• Memory mapped structure for each channel

• Can be expanded to N channels

Figure 20. Block Diagram for Synchronized Sampling of more than Two Analog Channels

DSP56ADC16 Electrical Characteristics

Electrical Specifications

The DSP56ADC16 is fabricated in high density HCMOS with TTL compatible inputs and CMOS compatible outputs.

This device contains protective circuitry against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either Vcc or GND).

Maximum Electrical Ratings (V_{SS} = 0 Vdc)

Rating	Symbol	Value	Unit
Supply Voltage	Vcc	-0.3 to +7.0	V
All Input Voltages	V_{in}	- 0.5 to Vcc + 0.5	V
Current Drain per Pin excluding Vdd and VSS	I	10	mA
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Full Scale Input Voltage at V_{REF} = 2.0V	V_{pp}	3.5	V

Thermal Characteristics —CERDIP Package

Characteristics Thermal Resistance — Ceramic	Symbol	Value	Rating
Junction to Ambient	Θ_{JA}	68	°C/W
Junction to Case (estimated)	Θ_{JC}	0.7	°C/W

Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JA}) \tag{1}$$

Where:

T_A = Ambient Temperature, °C

Θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times$ Vcc, Watts - Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins - User Determined

For most applications $P_{I/O} << P_{INT}$ and can be neglected. An appropriate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K/(T_J + 273° C) \tag{2}$$

DSP56ADC16 Electrical Characteristics

Solving equations (1) and (2) for K gives:

$$K = P_D \times (T_A + 273^\circ\,C) + \Theta_{JA} \times P_D{}^2 \qquad\qquad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation (2) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A. The total thermal resistance of a package (Θ_{JA}) can be separated into two components, Θ_{JC} and C_A, representing the barrier to heat flow from the semiconductor junction to the package (case) surface (Θ_{JC}) and from the case to the outside ambient (C_A). These terms are related by the equation:

$$\Theta_{JA} = \Theta_{JC} + C_A \qquad\qquad (4)$$

Θ_{JC} is device related and cannot be influenced by the user. However, C_A is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling, and thermal convection. Thus, good thermal management on the part of the user can significantly reduce C_A so that Θ_{JA} approximately equals Θ_{JC}. Substitution of Θ_{JC} for Θ_{JA} in equation (1) will result in a lower semiconductor junction temperature. Values for thermal resistance presented in this document, unless estimated, were derived using the procedure described in Motorola Reliability Report 7843, "Thermal Resistance Measurement Method for MC68XX Microcomponent Devices", and are provided for design purposes only. Thermal measurements are complex and dependent on procedure and setup. User-derived values for thermal resistance may differ.

DSP56ADC16 Electrical Characteristics

Electrical Specifications (Vcc=5V ±10%, T_A=-40 to +85 ^{o}C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	2.0		Vcc	V
Input Low Voltage	V_{IL}	-0.3		0.8	V
Input Leakage Current	I_{in}			1.0	μA
Hi-Z (OFF State) Input Current for SDO (V_{in} = 0.4 to 2.4 V)	I_{TSI}			10	μA
Output High Voltage (I_{OH} = -400 μA)	V_{OH}	2.4			V
Output Low Voltage (I_{OL} = 2mA)	V_{OL}			0.5	V
Power Dissipation at f = 12.8 MHz: (Note 1)	P_D		300	400	mW
Input Impedance (Analog Input)	Z_{in}		Note 2		Ω
Input Impedance (Reference Input)	Z_{ref}		Note 2		Ω
Input Capacitance	C_{in}		10		pF

Note 1: Power dissipation is the function of CLKIN. For CLKIN less than 12.8 MHz (see **Power Dissipation** on page 13).
Note 2: Impedances for the analog input and voltage reference input are functions of CLKIN (see **Input Imped-ances** on page 13).

Analog Characteristics [Vcc=5V, Vin = 1.2 V_{RMS} (10 kHz differential sinewave), V_{cm} = 2.5V, T_A= 25 ^{o}C, Clkin = 6.4 MHz, FIR Mode (word wide frame sync), Internal V_{ref}]

Characteristic	Symbol	Min	Typ	Max	Unit
Resolution		12		16	Bits
Signal-to-Noise Ratio	SNR	88	90		dB
Signal-to-Total Harmonic Distortion Ratio (Note 1)	S/THD	80	83		dB
Differential Nonlinearity	DNL		(Note 2)		LSBs
Gain Drift			50		ppm/$^\circ$C
DC Offset Error			0.3	3.0	mV
V_{refout} Voltage (Loaded by V_{refin})		0.4*Vcc - 4%	0.4*Vcc	0.4*Vcc+ 4%	V

Note 1: THD performance can be improved, depending on the applications, by making slight adjustments to the DC common mode voltage at the analog inputs.
Note 2: See **Performance Evaluations** on page 8 for detail.

DSP56ADC16 Electrical Characteristics

AC Electrical Specifications - Clock In/Out and Frame Sync (Vcc=5V ±10%, T_A=-40 to +85 ^{o}C)

Num	Characteristic	Symbol	Min	Max	Unit
	Clock In Frequency (t_{ck} = 1/f)	f	1	12.8	MHz
1	Clock Period	t_{ck}	78	1000	ns
2	Duty Cycle	t_{PW}	0.475	0.525	t_{ck}
3	Clock Rise Time	t_r	5		ns
4	Clock Fall Time	t_f	5		ns
5	Frame Sync Input Setup Time	t_{fsisu}	20	$1/t_{ck}$	ns
6	Frame Sync Input Hold Time	t_{fsih}	20	Note 1	ns
7	Serial Clock Output Delay Time	t_{scod}	25	75	ns

Note 1: The FSI input must be deasserted for at least two CLKIN periods prior to being asserted.

AC Electrical Specifications - FSO/SCO/SDO when FSEL=0 (Vcc=5V ±10%, T_A=-40 to +85 ^{o}C)

Num	Characteristic	Symbol	Min	Max	Unit
9	Frame Sync Output Setup Time before Falling Edge of SCO (SFMT=0)	t_{fsckl}	130	-	ns
10	Frame Sync Output Hold Time after Falling Edge of SCO (SFMT=0)	t_{clklfs}	130	-	ns
11	Serial Data Output Setup Time	t_{dsu}	130	-	ns
12	Serial Data Output Hold Time	t_{dh}	130	-	ns
13	Frame Sync Output Setup Time before SCO Rising Edge (SFMT=1)	t_{fslckh}	110	-	ns
14	Frame Sync Output High to SCO Rising Edge (SFMT=1)	t_{fshckh}	110	-	ns
15	Delay from Frame Sync Input to Frame Sync Output (SFMT=0)	$t_{fsifsob}$	5	-	cyc
16	Delay from Frame Sync Input to Frame Sync Output (SFMT=1)	$t_{fsifsow}$	8	-	cyc
17	Serial Clock Output Period	t_{sckout}	4	4	t_{ck}

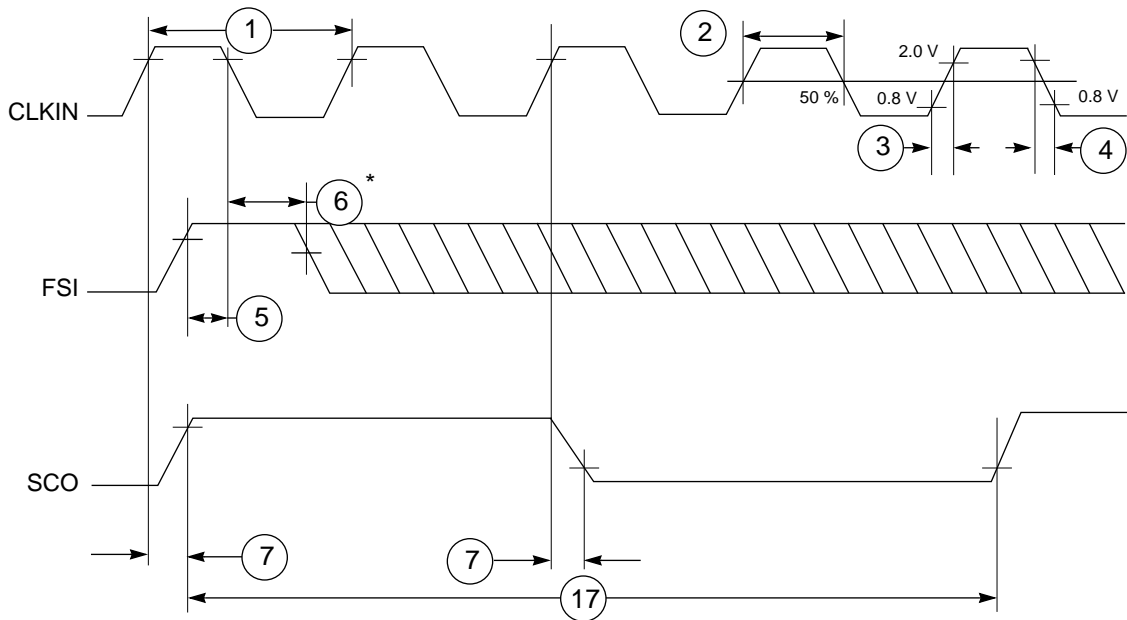**AC Electrical Specifications - FSO/SCO/SDO when FSEL=1** (Vcc=5V ±10%, T_A=-40 to +85 ^{o}C)

Num	Characteristic	Symbol	Min	Typ	Max	Unit
18	Frame Sync Output Setup Time before Falling Edge of SCO	t_{fsckl}		65	-	ns
19	Frame Sync Output Hold Time after Falling Edge of SCO	t_{clklfs}		65	-	ns
20	Serial Data Output Setup Time	t_{sdosu}	40		-	ns
21	Serial Data Output Hold Time	t_{sdoh}	40		-	ns
22	Delay from Frame Sync Input to Frame Sync Output	t_{fsifso}	1.5		-	cyc
23	Serial Clock Output Period	t_{sckout}	2		2	t_{ck}

DSP56ADC16 Electrical Characteristics

AC Electrical Specifications - $\overline{\text{DOE}}$ (Vcc=5V ±10%, T_A=-40 to +85 °C)

	Characteristic	Symbol	Min	Max	Unit
24	Serial Data Output Enable Delay Time	t_{doedv}	0	20	ns
25	Serial Data Output Disable Delay Time	t_{doedz}‡	0	20	ns

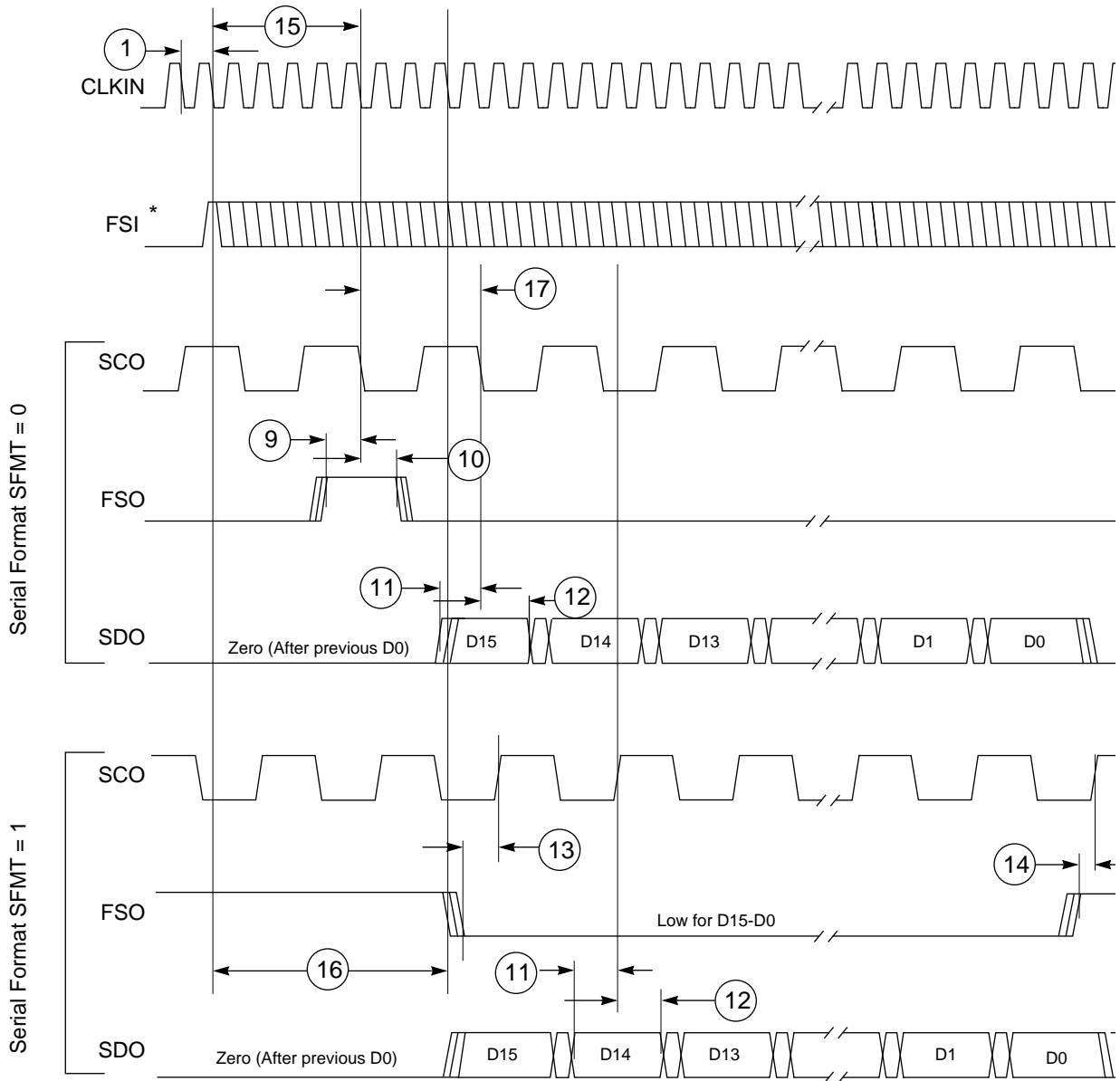‡ t_{doedz} is three-state 500 mV from 2.4 V or 0.5 V level with C_L=50 pF+1 TTL load.

FIR Filter Output Mode

*The FSI must be deasserted for at least two CLKIN periods prior to being asserted.

Figure 21. Timing Diagram for CLKIN/FSI/SCO When FSEL=0

DSP56ADC16 Electrical Characteristics

*The FSI input must be deasserted for at least two CLKIN periods prior to being asserted.

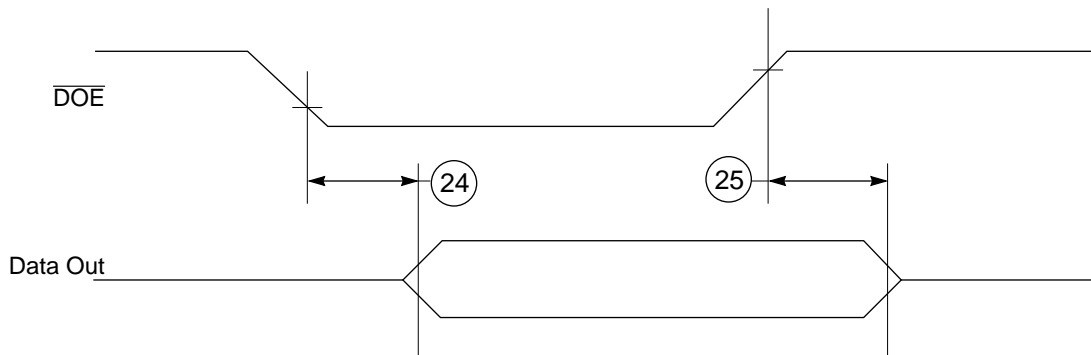**Figure 22. Timing Diagram for FSO/SCO/SDO When FSEL=0**

DSP56ADC16 Electrical Characteristics

FIR Filter Output Mode

Figure 23. Timing Diagram for FSO/SCO/SDO When FSEL=0

DSP56ADC16 Electrical Characteristics

COMB Filter Output Mode

*The FSI must be deasserted for at least two CLKIN periods prior to being asserted.

Figure 24. Timing Diagrams for FSO/SCO/SDO When FSEL=1

Figure 25. Timing Diagrams of $\overline{DOE}$ and Data Output

DSP56ADC16 Electrical Characteristics

SPECIFICATION DEFINITIONS

V_{ref} is the voltage at the REFOUT pin, measured when the maximum V_{refin} current is sourced from that pin.

LSB is the smallest voltage change that is required at the device input to produce a one bit change in the device output code.

SNR is the ratio of the fundamental signal power versus the total non-harmonic noise power within a finite bandwidth. Expressed in dB, SNR represents the peak signal versus RMS noise ratio.

S/THD is the ratio of the fundamental signal power versus the total signal harmonic power. Expressed in dB. The number of harmonics included must be specified.

S/THD+N is the ratio of the fundamental signal power versus the sum total of the band limited non-harmonic RMS noise power and the signal harmonic power. The number of harmonics and the applicable bandwidth must be specified.

DC Offset is the differential DC input voltage required to produce a zero output code.

Offset Error is the difference between the actual and the ideal input signal voltage required to produce a negative full-scale output code value. This is normally specified since the transfer curve is well represented by DC offset and gain error specifications.

The **FIR Pass-band Frequency** is the frequency at which the device response is within the ripple specification.

The **FIR Cut Off Frequency** is the frequency at which the device response is -3 dB below the pass-band response.

The **FIR Stop-band Frequency** is the frequency at which the device response is - 3 dB above the noise floor.

DNL is the width (in LSBs) of any code step, measured from code transition "n" to code transition "n+1", over the entire code conversion range.

Dynamic Range is the input signal range defined as the ratio of the maximum usable input signal and the noise floor of the device in operation, expressed in dB.

Resolution is the number of serial output bits which contain useful information.

In-Band Ripple is the response variation of the converter in the defined pass-band region, specified in dB.

DSP56ADC16 Electrical Characteristics

Input Impedance is the actual input impedance (resistive and reactive) seen at the input of the device, measured with respect to device analog ground return pin. The analog input amplitude/frequency range and input sampling clock rate must be specified.

Input Capacitance is the actual input capacitance seen at the input of the device, measured with respect to the device analog ground return pin. The analog input amplitude/frequency range and input sampling clock rate must be specified

Single-Ended Operation is when one of the two analog inputs is held at a fixed voltage level and the signal to be converted is applied to the remaining input, possibly with a DC bias level included. The device still converts the voltage seen differentially across the two inputs.

Differential Operation is when both of the two analog inputs are driven with complementary signals. D.C. bias levels may be applied to either of the input pins. The device converts the voltage seen differentially across the two inputs.

Input Analog Voltage Range is the range of input voltage over which meaningful digital output codes are produced which properly represent the input voltage signal.

Package Dimensions

Ordering Information
Order this part by the part number:
DSP56ADC16S

Literature Distribution Centers:

USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.

EUROPE: Motorola Ltd.; European Literature Center; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.

JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.

ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbor Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

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Order this document
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Rev 2

Errata to
DSP56ADC16
16-bit Sigma-Delta Analog-to-Digital Converter

The following changes apply to the DSP56ADC16 Advanced Information Data Sheet (ADI1525).

On Page 20:

Under the heading "Thermal Characteristics," the line that reads "Thermal Resistance Plastic" should read "Thermal Resistance Ceramic".

Under the heading "AC Electrical Specifications":

The maximum Clock Period, which now reads "100", should be "1000".

The minimum Duty Cycle, which now reads "0.473", should read "0.475 t_{clk}".

The maximum Duty Cycle, which now reads "0.525", should read "0.525 t_{clk}".

The Duty Cycle unit, which now reads "t_{clk}", should read "ns".

The Serial Clock Output Delay Time (minimum), which now reads "30", should read "25 ns".

The Frame Sync Output Set-up Time before SCO Rising Edge (minimum), which now reads "130", should read "110 ns".

The Frame Sync Output High to SCO Rising Edge (minimum), which now reads "130", should read "110 ns".

The Input Capacitance, which now reads "10 pF maximum", should read "10 pF typical".

Specifications added for clarity:

	Min	Typical	Max
V_{refout}	(V_{cc} x 0.4) - 4% Volts	V_{cc} x 0.4 Volts	(V_{cc} x 0.4) + 4% Volts
Signal - to - Noise	88 dB	90 dB	-
Total Harmonic Distortion	-	-	-80 dB
Full-Scale Input Voltage	-	2 x V_{ref} - 0.5 Volts p-p	-

SNR and THD test conditions: V_{cc} = 5 Volts; V_{in} = 1.2 Volts RMS; V_{cm} = 2.5 Volts; T_a = 25°C

10 kHz Differential Sinewave; CLKIN = 6.4 MHz; FIR word-wide Mode; Using Internal V_{ref}