SONY

CXP888P60

CMOS 8-bit Single Chip Microcomputer

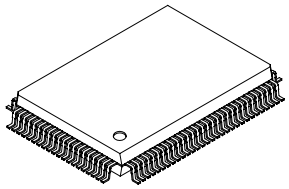
Description

The CXP888P60 is a CMOS 8-bit micro-computer which consists of A/D converter, serial interface, timer/counter, time base timer, high precision timing pattern generation circuits, PWM output, VISS/VASS circuit, 32kHz timer/counter, remote control receiving circuit, VSYNC separator and the measurement circuit which measure signals of capstan FG amplifier and drum FG/PG amplifier and other servo systems, as well as basic configurations like 8-bit CPU, PROM, RAM and I/O port. They are integrated into a single chip.

Also, CXP888P60 provides sleep/stop function which enables to lower power consumption.

The CXP888P60 is the PROM-incorporated version of the CXP88860 with built-in mask ROM. This provides the additional feature of being able to write directly into the program. Thus, it is most suitable for evaluation use during system development and for small-quantity production.

100 pin QFP (Plastic)



Structure

Silicon gate CMOS IC

Features

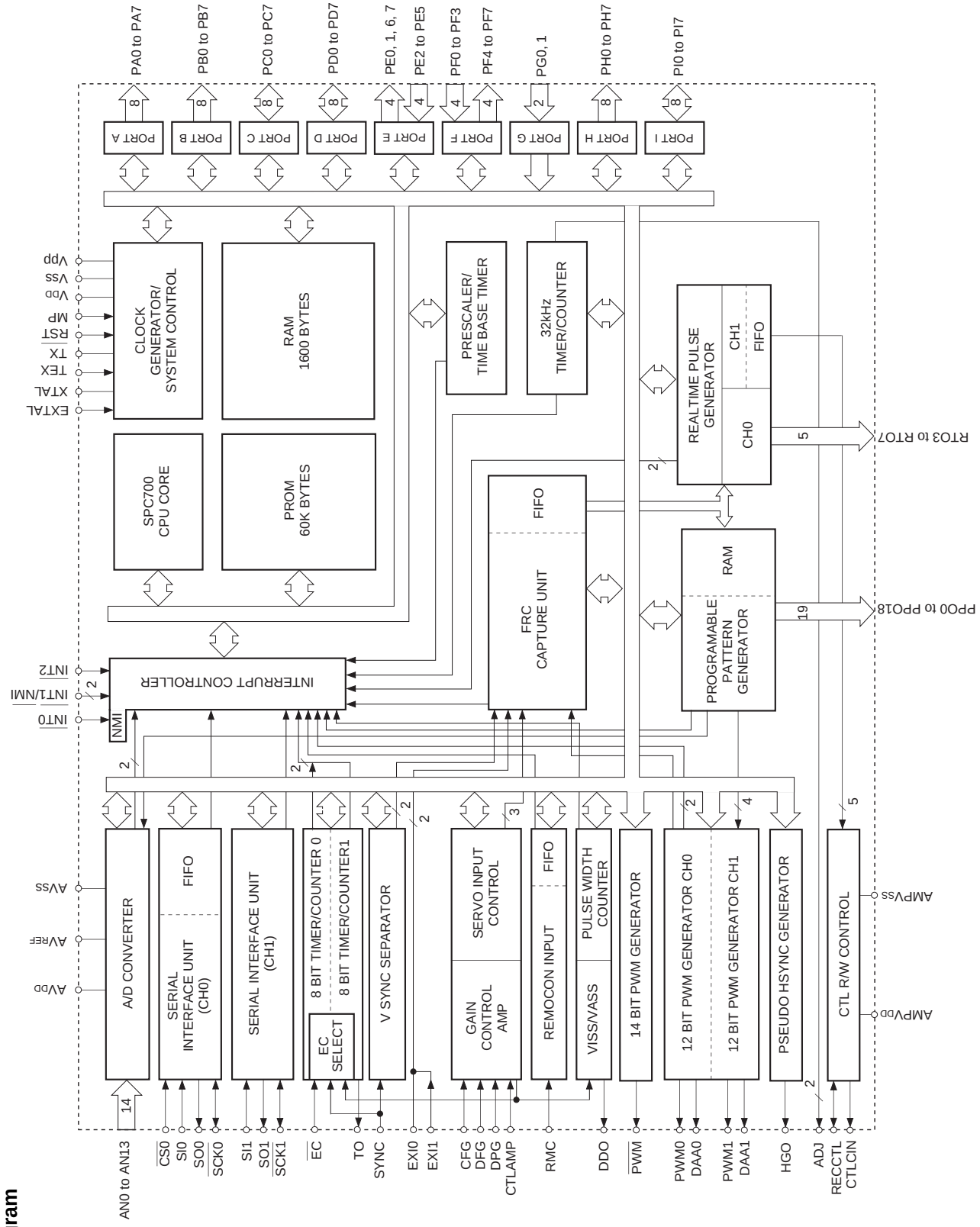
- A wide instruction set (213 instructions) which cover various types of data
  — 16-bit arithmetic/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle 250ns at 16MHz operation
  122µs at 32kHz operation
- Incorporated PROM capacity 60K bytes
- Incorporated RAM capacity 1600 bytes (including PPG RAM)
- Peripheral function

— A/D converter	8 bits, 8 channels, successive approximation system (Conversion time of 20µs/16MHz)
— Serial interface	Incorporated 8-bit, 8-stage FIFO for data (Auto transfer for 1 to 8 bytes), 1 channel 8-bit clock sync type, 1 channel
— Timer	8-bit timer/counter, 2 channels 19-bit time base timer 32kHz timer/counter
— High precision timing pattern generation	PPG 19 pins 32-stage programmable circuit RTG 5 pins, 1 channel 5-bit, 8-satge FIFO (RECCTL control), 1channel
— PWM/DA gate output	12 bits, 2 channels (Repetitive frequency 62.5kHz/16MHz) DA gate pulse output, 13 bits, 2 channels
— Analog signal input circuit	Capstan FG amplifier circuit Drum FG amplifier circuit Drum PG amplifier circuit PBCTL amplifier circuit
— CTL write/rewrite circuit	Recording current control circuit
— Servo input control	Capstan FG, Drum FG/PG, CTL input
— VSYNC separator	
— FRC capture unit	Incorporated 26-bit and 8-stage FIFO
— PWM output	14-bit, 1 channel
— VISS/VASS circuit	Pulse duty auto detection circuit
— 32kHz timer/event counter	32kHz oscillation circuit, ultra-low speed instruction mode
— Remote control reception circuit	8-bit pulse measurement counter, 6-stage FIFO
— Tri-state output	PPG 1 pin, output 8 pins
— Pseudo HSYNC output function	
— High speed head switching circuit	

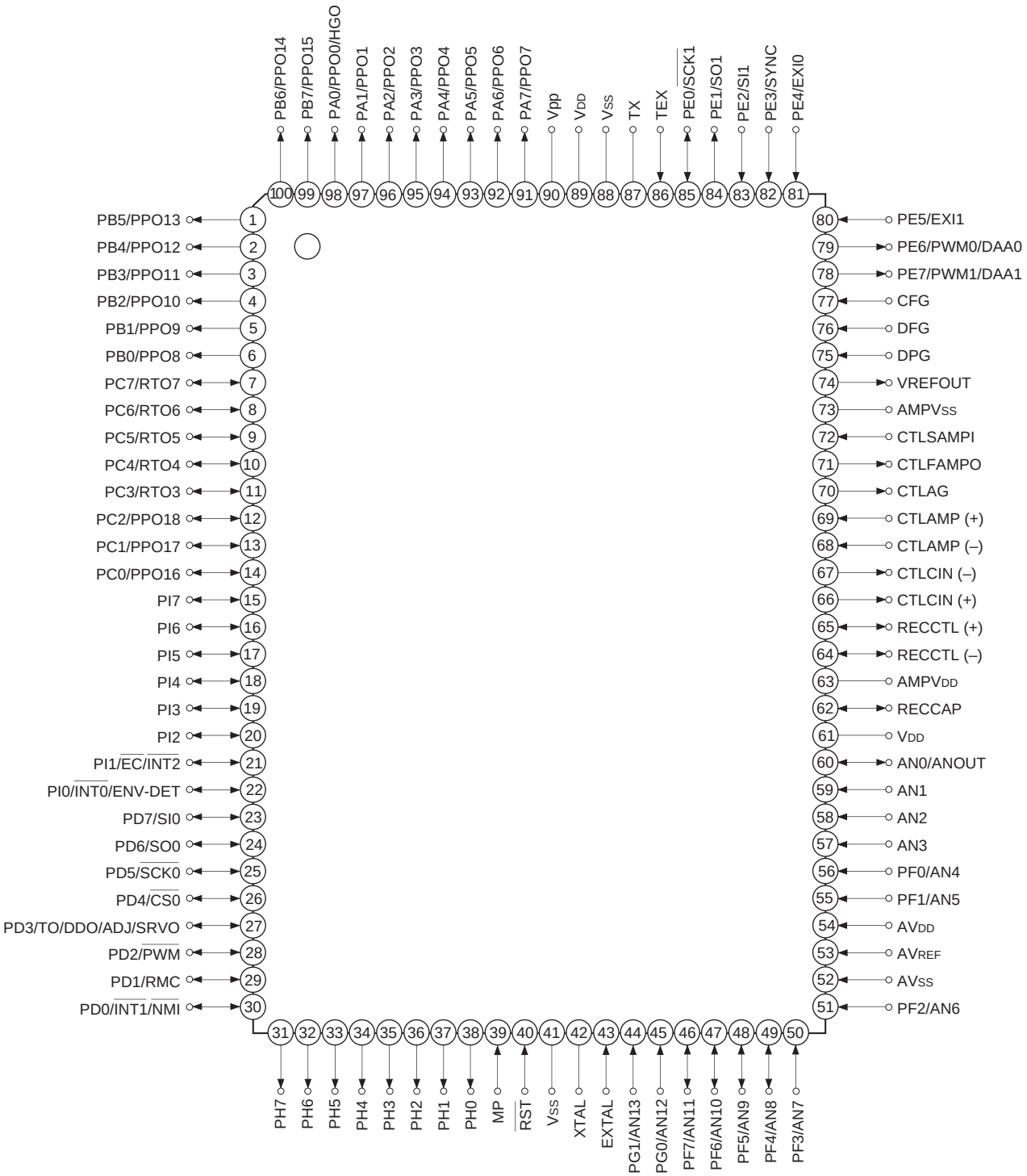
- Interruption 20 factors, 15 vectors, multi-interruption possible
- Standby mode SLEEP/STOP
- Package 100-pin plastic QFP

E96107-ST

Block Diagram



Pin Assignment (Top View)



Note) 1. Vpp (Pin 90) is always connected to V_{DD}.
2. V_{DD} (Pins 61 and 89) are both connected to V_{DD}
3. Vss (Pins 41 and 88) are both connected to GND.
4. MP (Pin 39) must be connected to GND.

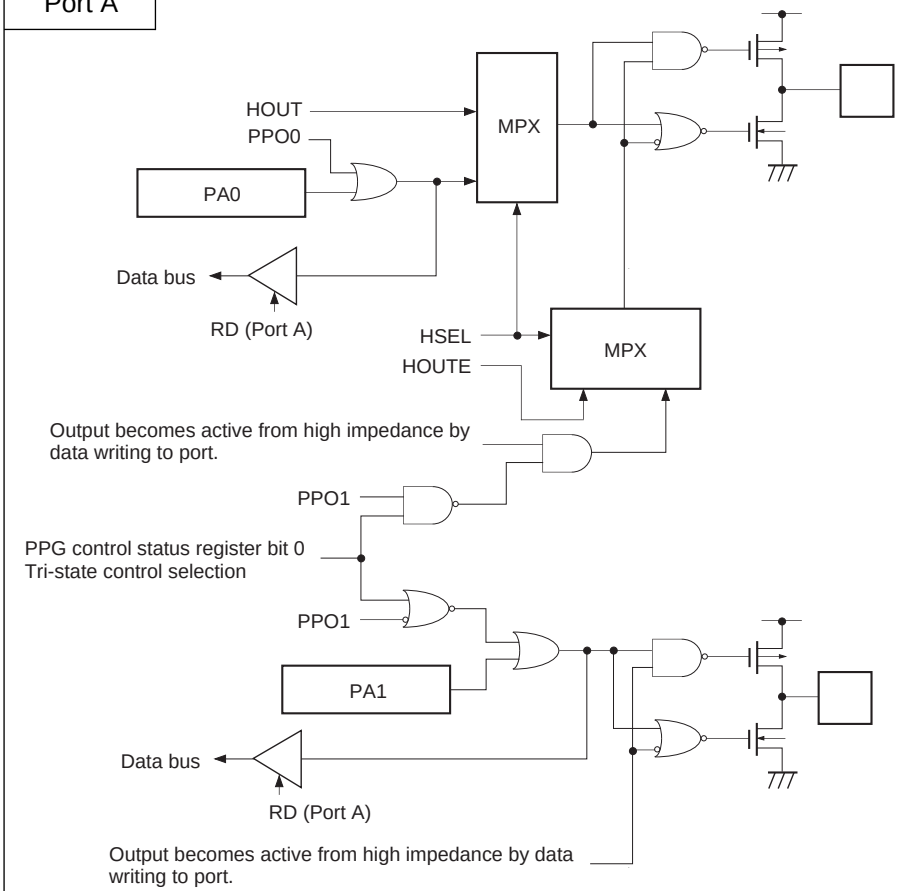
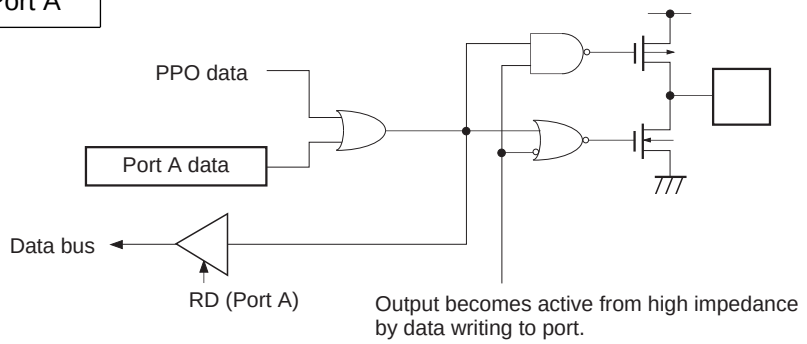
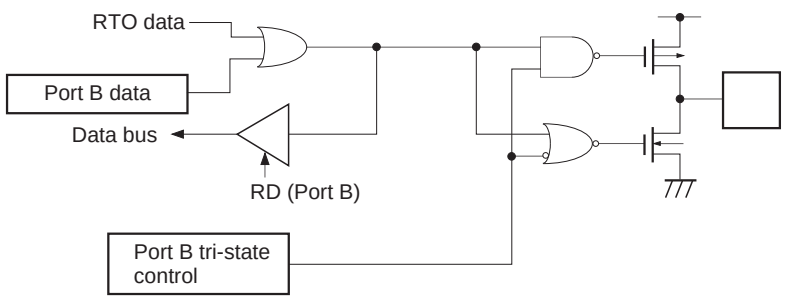
Pin Description

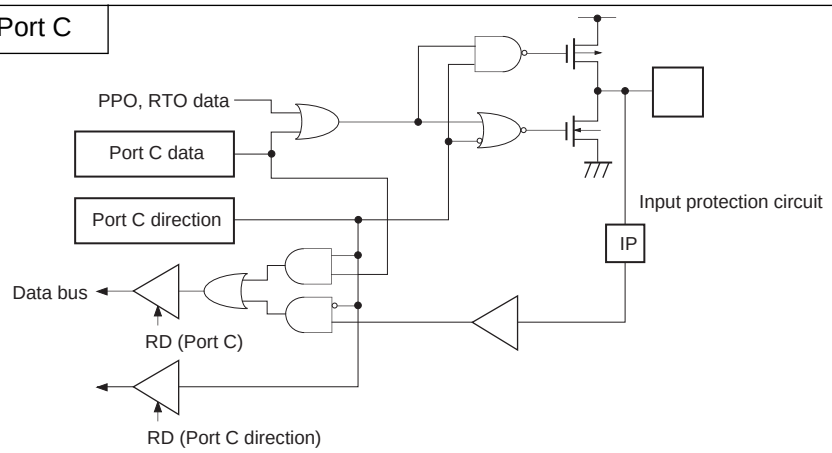
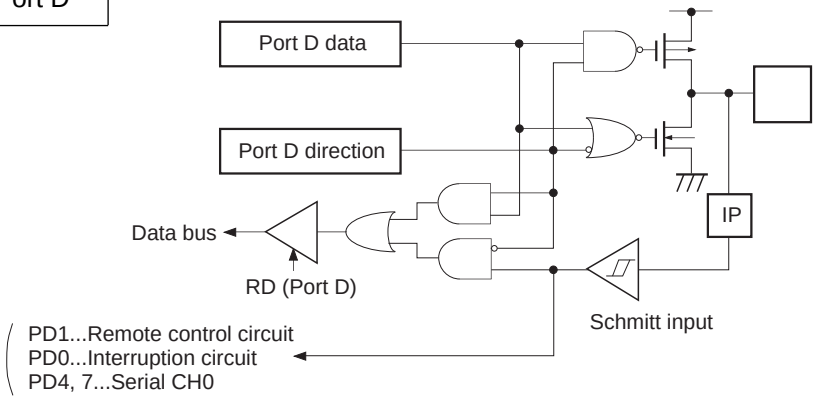
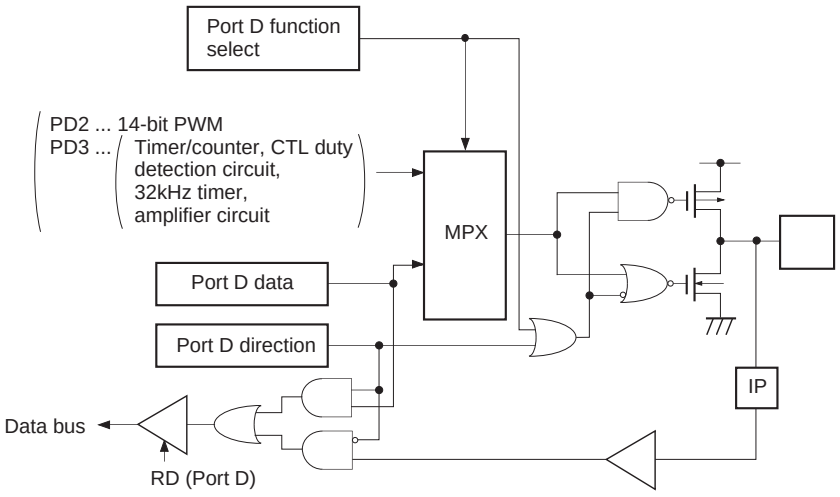
<table>
<tr><th>Symbol</th><th>I/O</th><th colspan="3">Description</th></tr>
<tr><td>PA0/PPO0
/HGO</td><td>Output/Real-time output/Output</td><td rowspan="2">(Port A)
8-bit output port. Data is gated with PPO contents by OR-gate and they are output.
(8 pins)</td><td colspan="2">Pseudo HSYNC output pin.</td></tr>
<tr><td>PA1/PPO1
to
PA7/PPO7</td><td>Output/
Real-time output</td><td colspan="2" rowspan="3">Programmable pattern generator (PPG) output. Functions as high precision real-time pulse output port.
(19 pins)
PA0 can be tri-state controlled with PPG.</td></tr>
<tr><td>PB0/PPO8
to
PB7/PPO15</td><td>Output/
Real-time output</td><td>(Port B)
8-bit output port. Data is gated with PPO contents by OR-gate and they are output.
Tri-state control is possible.
(8 pins)</td></tr>
<tr><td>PC0/PPO16
to
PC2/PPO18</td><td>I/O/
Real-time output</td><td rowspan="2">(Port C)
8-bit I/O port. I/O can be set in a unit of single bits. Data is gated with PPO or RT contents by OR-gate and they are output.
(8 pins)</td></tr>
<tr><td>PC3/RTO3
to
PC7/RTO7</td><td>I/O/
Real-time output</td><td colspan="2">Real-time pulse generator (RTG) output. Functions as high precision real-time pulse output port.
(5 pins)</td></tr>
<tr><td>PD0/$\overline{\text{INT1}}$/
$\overline{\text{NMI}}$</td><td>I/O/Input/Input</td><td rowspan="8">(Port D)
8-bit I/O port. I/O can be set in a unit of single bits.
(8 pins)</td><td colspan="2">Input pin to request external interruption and non-maskable interruption.</td></tr>
<tr><td>PD1/RMC</td><td>I/O/Input</td><td colspan="2">Remote control receiving circuit input pin.</td></tr>
<tr><td>PD2/$\overline{\text{PWM}}$</td><td>I/O/Output</td><td colspan="2">14-bit PWM output pin.</td></tr>
<tr><td>PD3 /TO
DDO/ADJ
SRVO</td><td>I/O/Output/Output/
Output/Output</td><td colspan="2">Timer/counter, CTL duty detector, 32kHz oscillation adjustment and servo amplifier output pin.</td></tr>
<tr><td>PD4/$\overline{\text{CS0}}$</td><td>I/O/Input</td><td colspan="2">Serial chip select (CH0) input pin.</td></tr>
<tr><td>PD5/$\overline{\text{SCK0}}$</td><td>I/O/I/O</td><td colspan="2">Serial clock (CH0) I/O pin.</td></tr>
<tr><td>PD6/SO0</td><td>I/O/Output</td><td colspan="2">Serial data (CH0) output pin.</td></tr>
<tr><td>PD7/SI0</td><td>I/O/Input</td><td colspan="2">Serial data (CH0) input pin.</td></tr>
<tr><td>PE0/$\overline{\text{SCK1}}$</td><td>Output/I/O</td><td rowspan="8">(Port E)
8-bit port. Bits 2, 3, 4 and 5 are for inputs; bits 0, 1, 6 and 7 are for outputs.
(8 pins)</td><td colspan="2">Serial clock (CH1) I/O pin</td></tr>
<tr><td>PE1/SO1</td><td>Output/Output</td><td colspan="2">Serial data (CH1) output pin</td></tr>
<tr><td>PE2/SI1</td><td>Input/Input</td><td colspan="2">Serial data (CH1) input pin</td></tr>
<tr><td>PE3/SYNC</td><td>Input/Input</td><td colspan="2">Composite sync signal input pin.</td></tr>
<tr><td>PE4/EXI0</td><td>Input/Input</td><td colspan="2" rowspan="2">External input pin for FRC capture unit.
(2 pins)</td></tr>
<tr><td>PE5/EXI1</td><td>Input/Input</td></tr>
<tr><td>PE6/PWM0/
DAA0</td><td>Output/Output</td><td rowspan="2">PWM output pin.
(2 pins)</td><td rowspan="2">DA gate pulse output pin.
(2 pins)</td></tr>
<tr><td>PE7/PWM1/
DAA1</td><td>Output/Output</td></tr>
</table>

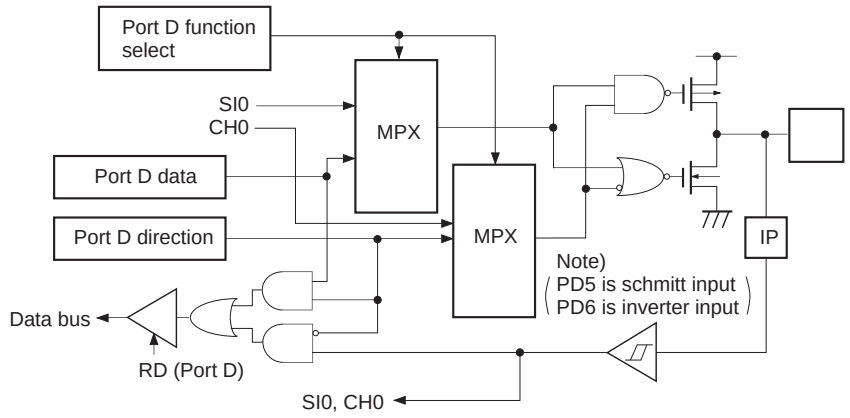
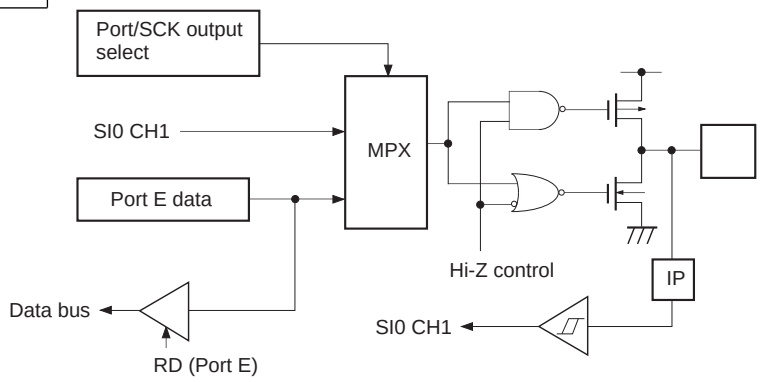
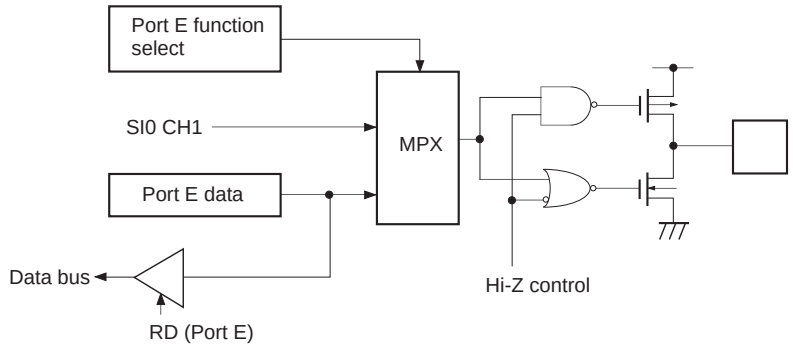
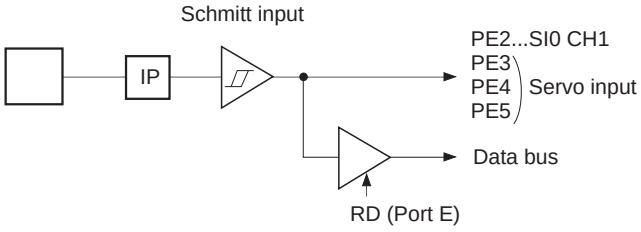
Description	I/O	Description		
AN0/ANOUT	Input/Output			Analog circuit internal waveform output pin.
AN1 to AN3	Input			
PF0/AN4 to PF3/AN7	Input/Input	(Port F) Lower 4 bits are for inputs; upper 4 bits are for outputs. Lower 4 bits are standby release input pins. (8 pins)		Analog input pin for A/D converter. (14 pins)
PF4/AN8 to PF7/AN11	Output/Input			
PG0/AN12 PG1/AN13	Input/Input	(Port G) 2-bit input port. (2 pins)		
PH0 to PH7	Output	(Port H) 8-bit output port; N-ch open drain output of medium drive voltage (12V) and large current (12mA). (8 pins)		
PI0/$\overline{\text{INT0}}$/ ENV-DET	I/O/Input	(Port I) 8-bit I/O port. I/O can be set in a unit of single bits. Function as standby release input can be set in a unit of single bits. (8 pins)	Input pin to request external interruption. Active when falling edge.	Trigger pulse input pin for head switching.
$\overline{\text{PI1}}$/$\overline{\text{EC}}$/ $\overline{\text{INT2}}$	I/O/Input/Input		External event input pin for timer/counter.	Input pin to request external interruption. Active when falling edge.
PI2 to PI7	I/O			
CFG	Input	Capstan FG input pin.		
DFG	Input	Drum FG input pin.		
DPG	Input	Drum PG input pin.		
RECCTL (+) RECCTL (–)	I/O	RECCTL signal output pin. (2 pins)	PBCTL signal input pin. (2 pins)	
CTLCIN (+) CTLCIN (–)	Output	Connected to RECCTL (+) and RECCTL (–) with the internal switch for playback. (2 pins)		
CTLAMP (+) CTLAMP(–)	Input	Input PBCTL signal with capacitor coupled. (2 pins)		
CTLFAMPO	Output	PBCTL signal 1st amplifier output.		
CTLSAMPI	Input	PBCTL signal 2nd amplifier input.		
RECCAP	I/O	Capacitor connecting pin for the slope setting of the CTL writing trapezoidal wave.		
VREFOUT	Output	Capacitor connecting pin for the VREF level smoothing of DPG, DFG and CFG.		
CTLAG	Output	Capacitor connecting pin for the CTL and AGND smoothing.		
$AMPV_{SS}$		Analog signal input circuit GND pin.		
$AMPV_{DD}$		Analog signal input circuit power supply pin.		

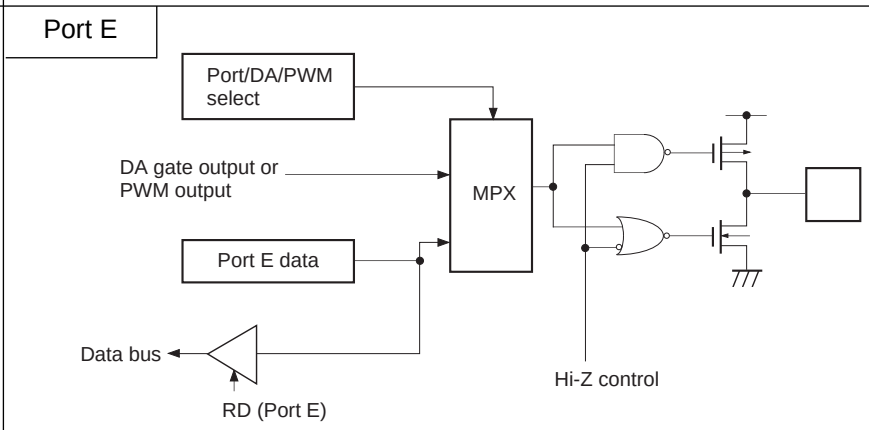
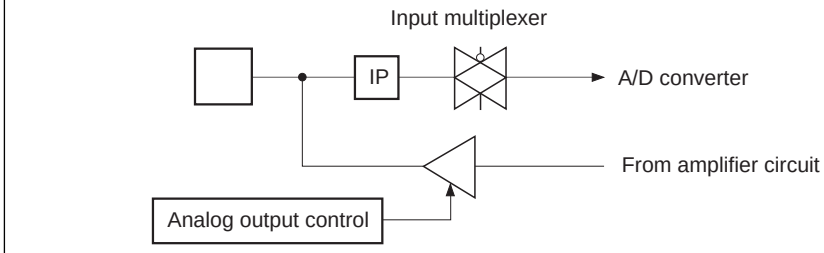
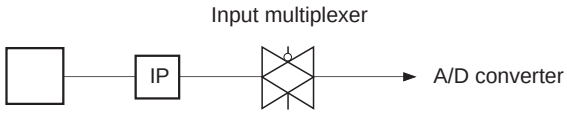
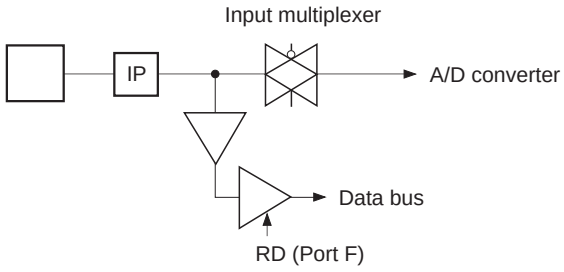
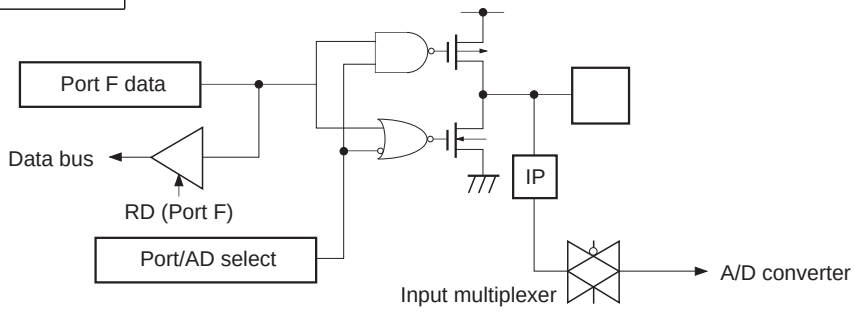
Symbol	I/O	Description
EXTAL	Input	Connecting pin of crystal oscillator for system clock. When supplying the external clock, input it to EXTAL pin and input the opposite phase clock to XTAL pin.
XTAL	Output	
TEX	Input	Connecting pin of crystal oscillator for 32kHz timer clock. When used as event counter, input to TEX pin and leave TX pin open. (In this time, feedback resistor is not removed.)
TX	Output	
$\overline{RST}$	Input	System reset pin; Low level active.
MP	Input	Test mode input pin. Always connect to GND.
AV_{DD}		Positive power supply pin for A/D converter.
AV_{REF}	Input	Reference voltage input pin for A/D converter.
AV_{SS}		GND pin for A/D converter.
V_{DD}		Positive power supply pin.
Vpp		Positive power supply for incorporated PROM writing. Connect this pin to V_{DD} for normal operation.
V_{SS}		GND pin. Connect both Vss pins to GND.

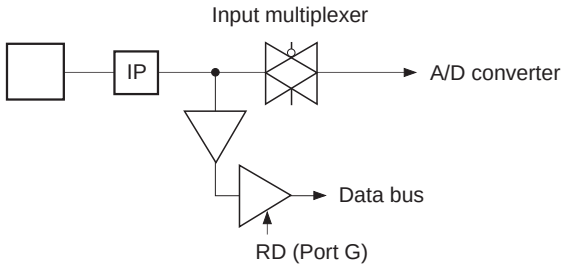
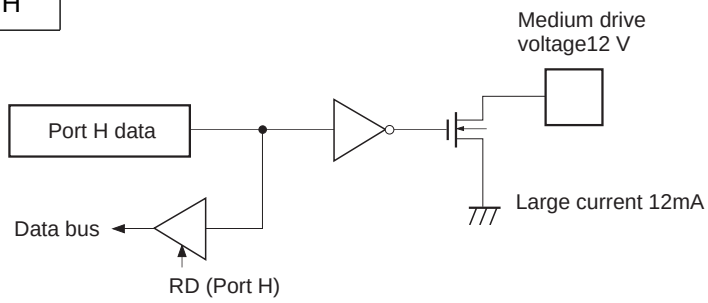
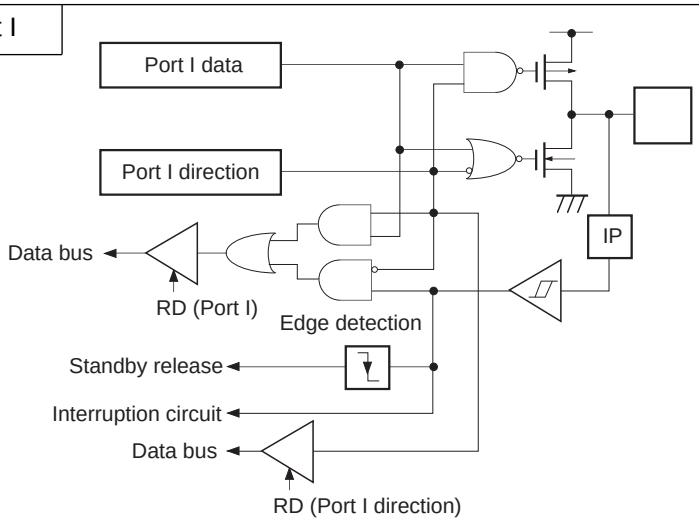
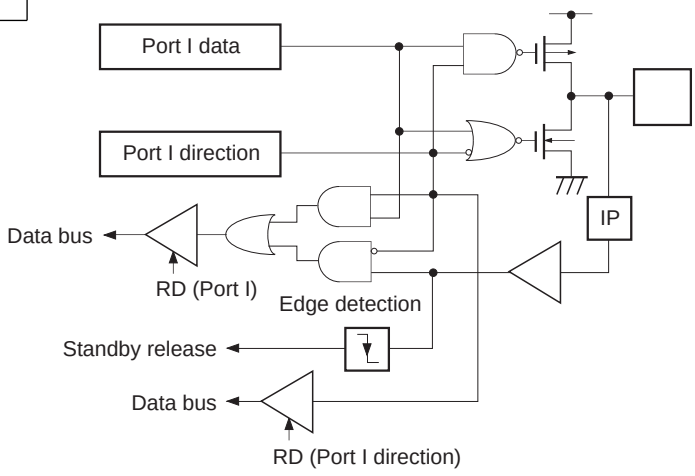
Input/Output Circuit Formats for Pins

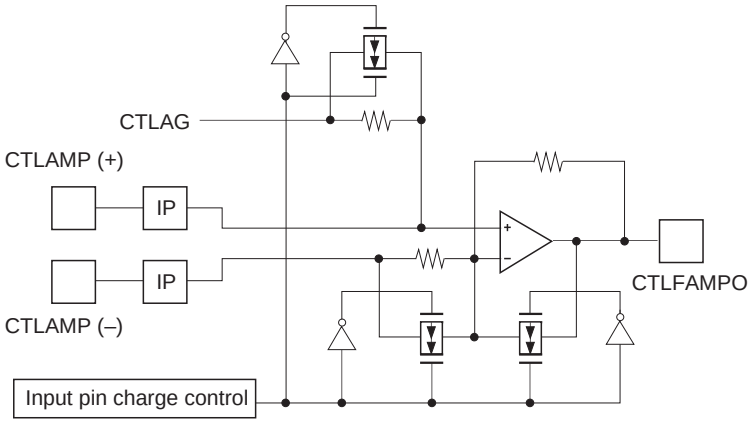
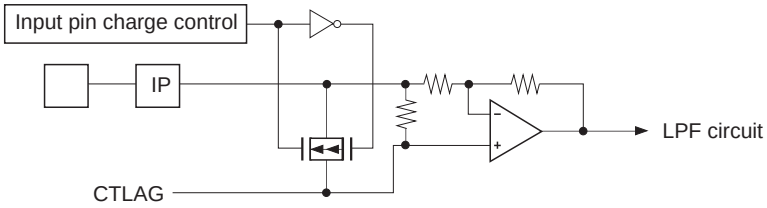
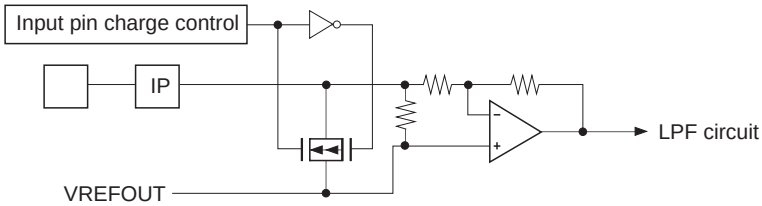
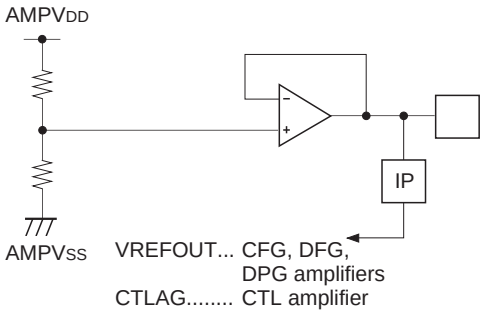
Pin	Circuit format	When reset
PA0/PPO0/ HGO 1 pin PA1/PPO1 1 pin	Port A 	Hi-Z Hi-Z
PA2/PPO2 to PA7/PPO7 6 pins	Port A 	Hi-Z
PB0/PPO8 to PB7/PPO15 8 pins	Port B 	Hi-Z

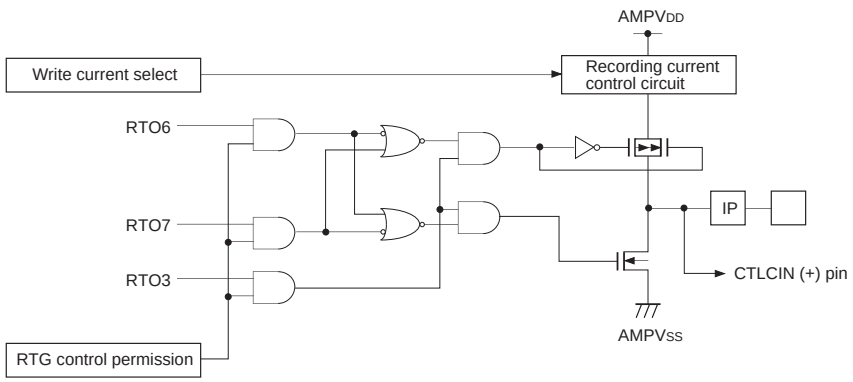
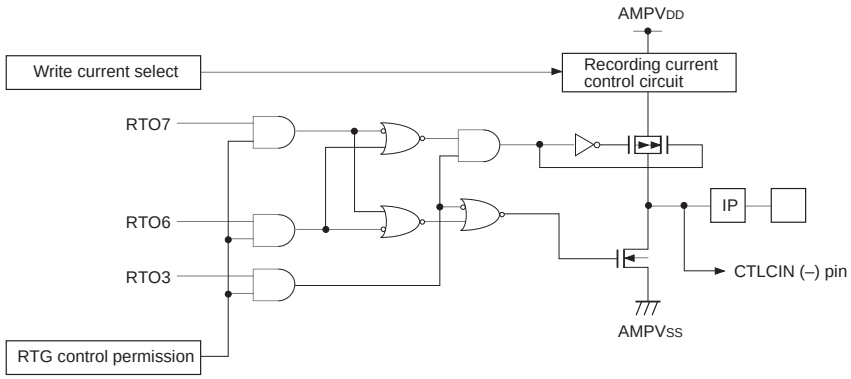
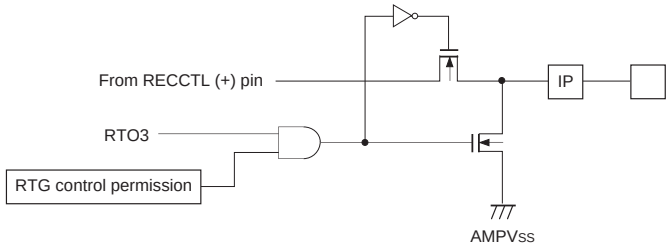
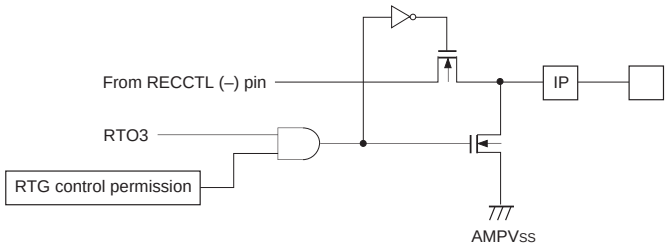
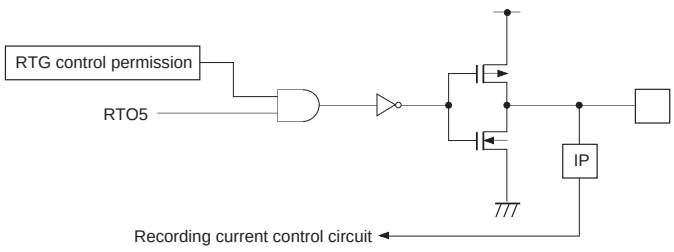
Pin	Circuit format	When reset
PC0/PPO16 to PC2/PPO18 PC3/RTO3 to PC7/RTO7 8 pins	Port C 	Hi-Z
PD0/$\overline{INT1}$/$\overline{NMI}$ PD1/RMC PD4/$\overline{CS0}$ PD7/SI0 4 pins	Port D 	Hi-Z
PD2/$\overline{PWM}$ PD3/TO/ DDO/ADJ/ SRVO 2 pins	Port D 	Hi-Z

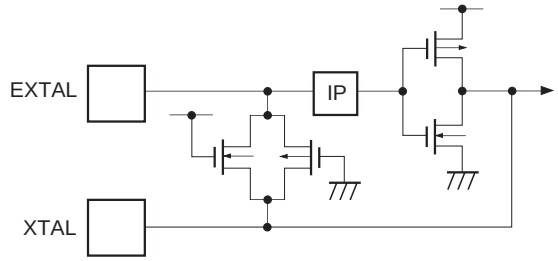
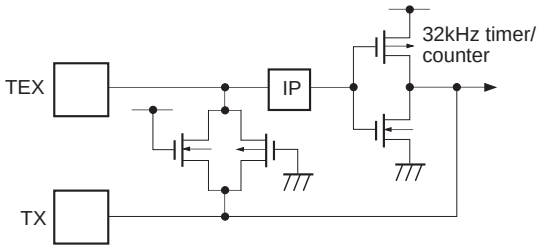
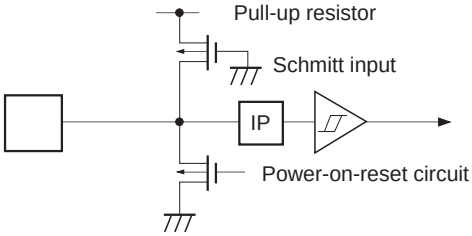
Pin	Circuit format	When reset
PD5/$\overline{SCK0}$ PD6/SO0 2 pins	Port D 	Hi-Z
PE0/$\overline{SCK1}$ 1 pin	Port E 	Hi-Z
PE1/SO1 1 pin	Port E 	Hi-Z
PE2/SI1 PE3/SYNC PE4/EXI0 PE5/EXI1 4 pins	Port E 	Hi-Z

Pin	Circuit format	When reset
PE6/PWM0/DAA0 PE7/PWM1/DAA1 2 pins	Port E 	High level
AN0/ANOUT 1 pin	Port E 	Hi-Z
AN1 to AN3 3 pin		Hi-Z
PFO/AN4 to PF3/AN7 4 pins	Port F 	Hi-Z
PF4/AN8 to PF7/AN11 4 pins	Port F 	Hi-Z

Pin	Circuit format	When reset
PG0/AN12 to PG1/AN13 2 pins	Port G 	Hi-Z
PH0 to PH7 8 pins	Port H 	Hi-Z
PI0/$\overline{\text{INT0}}$/ EVN-DET to PI1/$\overline{\text{EC}}$/$\overline{\text{INT2}}$ 2 pins	Port I 	Hi-Z
PI2 to PI7 6 pins	Port I 	Hi-Z

Pin	Circuit format	When reset
CTLAMP (+) CTLAMP (–) CTLFAMPO 3 pins		1/2AMPV$_{DD}$
CTLSAMPI 1 pin		1/2AMPV$_{DD}$
CFG DFG DPG 3 pins		1/2AMPV$_{DD}$
CTLAG VREFOUT 2 pins		1/2AMPV$_{DD}$

Pin	Circuit format	When reset
RECCTL (+) 1 pin		Hi-Z
RECCTL (–) 1 pin		Hi-Z
CTLCIN (+) 1 pin		Hi-Z
CTLCIN (–) 1 pin		Hi-Z
RECCAP 1 pin		Low level

Pin	Circuit format	When reset
EXTAL XTAL 2 pins	 • Shows the circuit composition during oscillation. • Feedback resistor is removed and XTAL becomes High level during stop.	Oscillation
TEX TX 2 pins	 • Shows the circuit composition during oscillation. • Feedback resistor is removed during 32kHz oscillation circuit stop by software. At this time, TEX pin outputs Low level and TX pin outputs High level.	Oscillation
$\overline{\text{RST}}$ 1 pin		Low level

Absolute Maximum Ratings (Vss = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
	Vpp	–0.3 to +13	V	Incorporated PROM
	AV_{DD}	AVss to +7.0 *1	V	
	AV_{SS}	–0.3 to +0.3	V	
	$AMPV_{DD}$	$AMPV_{SS}$ to +7.0 *2	V	
	$AMPV_{SS}$	–0.3 to +0.3	V	
Input voltage	V_{IN}	–0.3 to +7.0 *3	V	
Output voltage	V_{OUT}	–0.3 to +7.0 *3	V	
Medium drive output voltage	V_{OUTP}	–0.3 to +15.0	V	Port PH
High level output current	I_{OH}	–5	mA	
High level total output current	$\sum I_{OH}$	–50	mA	Total of output pins
Low level output current	I_{OL}	15	mA	Other than large current output ports (value per pin)
	I_{OLC}	20	mA	Large current output port *4 (value per pin)
Low level total output current	$\sum I_{OL}$	130	mA	Total of output pins
Operating temperature	Topr	–10 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	QFP package type

*1) AV_{DD} and V_{DD} must not exceed +0.3V.

*2) $AMPV_{DD}$ and V_{DD} must not exceed +0.3V.

*3) V_{IN} and V_{OUT} must not exceed V_{DD} +0.3V.

*4) The large current output port is port H (PH).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	Guaranteed operation range for 1/2 and 1/4 frequency dividing clock
		3.5	5.5		Guaranteed operation range for 1/16 frequency dividing clock or during SLEEP mode
		2.7	5.5		Guaranteed operation range by TEX clock
		2.5	5.5		Guaranteed data hold operation range during STOP
	Vpp	Vpp = V_{DD}			
Analog power supply	AV_{DD}	4.5	5.5	V	*1
	$AMPV_{DD}$	4.5	5.5	V	*2
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	*3
	V_{IHS}	0.8V_{DD}	V_{DD}	V	CMOS schmitt input *4
	V_{IHTS}	2.2	V_{DD}	V	TTL schmitt input *5
	V_{IHEX}	V_{DD} – 0.4	V_{DD} + 0.3	V	EXTAL pin*6 TEX pin*7
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	*3
	V_{ILS}	0	0.2V_{DD}	V	CMOS schmitt input *4
	V_{ILTS}	0	0.8	V	TTL schmitt input *5
	V_{ILEX}	–0.3	0.4	V	EXTAL pin *6 TEX pin *7
Operating temperature	Topr	–10	+75	°C	

*1) AV_{DD} and V_{DD} should be set to the same voltage.

*2) $AMPV_{DD}$ and V_{DD} should be set to the same voltage.

*3) Normal input port (each pin of PC, PD2, PD3, PD6, PF0 to PF3, PG and PI2 to PI7), MP pin

*4) Each pin of $\overline{RST}$, PD0/$\overline{INT1}$/$\overline{NMI}$, PD1/RMC, PD4/$\overline{CS0}$, PD5/SCK0, PD7/SI0, PE0/$\overline{SCK1}$, PE2/SI1, PE3/SYNC, PE4/EXI0, PE5/EXI1, PI0/$\overline{INT0}$, PI1/$\overline{EC}$/$\overline{INT2}$ (For PE3/SYNC, when CMOS schmitt input is selected with mask option.)

*5) PE3/SYNC

*6) Specifies only during external clock input.

*7) Specifies only during external event input.

Electrical Characteristics

DC Characteristics (V_{DD} = 4.5 to 5.5V) (Ta = –10 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE0 to PE1, PE6 to PE7, PF4 to PF7, PH (V_{OL} only) PI $\overline{RST}$*1 (V_{OL} only)	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output voltage	V_{OL}		V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PD, PH	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{IHT}	TEX	V_{DD} = 5.5V, V_{IH} = 5.5V	0.1		10	µA
	I_{ILT}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$		–1.5		–400	µA
I/O leakage current	I_{IZ}	PA to PG, PI, MP, AN0 to AN3,	V_{DD} = 5.5V, V_I = 0, 5.5V			±10	µA
Open drain output leakage current (N-CH Tr off state)	I_{LOH}	PH	V_{DD} = 5.5V V_{OH} = 12V			50	µA
Supply current*2	I_{DD1}	V_{DD}, V_{SS}	16MHz crystal oscillation (C_1 = C_2 = 15pF) V_{DD} = 5.5V*3		35	45	mA
	I_{DDS1}		SLEEP mode V_{DD} = 5.5V		2.0	8	mA
	I_{DD2}		32kHz crystal oscillation (C_1 = C_2 = 47pF) V_{DD} = 3.3V		50	100	µA
	I_{DDS2}		SLEEP mode V_{DD} = 3V ± 0.3V		9	35	µA
	I_{DDS3}		STOP mode (EXTAL and TEX pins oscillation stop) V_{DD} = 5V±0.5V			30	µA
Input capacity	C_{IN}	PC, PD, PE0, PE2 to PE5 PF, PG, PI, RECCTL (+), RECCTL (–), CTLAMP (+), CTLAMP (–), CTLSAMPI, CFG, DFG, DPG	Clock 1MHz 0V other than the measured pins		10	20	pF

*1) $\overline{RST}$ pin specifies the low level input voltage only when the power-on-reset circuit is selected.

*2) When entire output pins are open.

*3) When setting upper 2 bits (CPU clock selection) of clock control register (CLC: 00FE$_H$) to "00" and operating in high speed mode (1/2 frequency dividing clock).

AC Characteristics

(1) Clock timing (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	1		16	MHz
System clock input pulse width	t_{XL}, t_{XH}	XTAL EXTAL	Fig. 1, Fig. 2 External clock drive	28			ns
System clock input rise and fall times	t_{CR}, t_{CF}	XTAL EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count clock input pulse width	t_{EH}, t_{EL}	$\overline{EC}$	Fig. 3	t_{sys} + 200*1			ns
Event count clock input rise and fall times	t_{ER}, t_{EF}	$\overline{EC}$	Fig. 3			20	ms
System clock frequency	f_C	TEX TX	V_{DD} = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count clock input pulse width	t_{TL}, t_{TH}	TEX	Fig. 3	10			µs
Event count clock input rise and fall times	t_{TR}, t_{TF}	TEX	Fig. 3			20	ms

*1) t_{sys} indicates three values according to the contents of the clock control register (CLC; 00FE$_H$) upper 2 bits (CPU clock selection).
t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Fig. 1. Clock timing

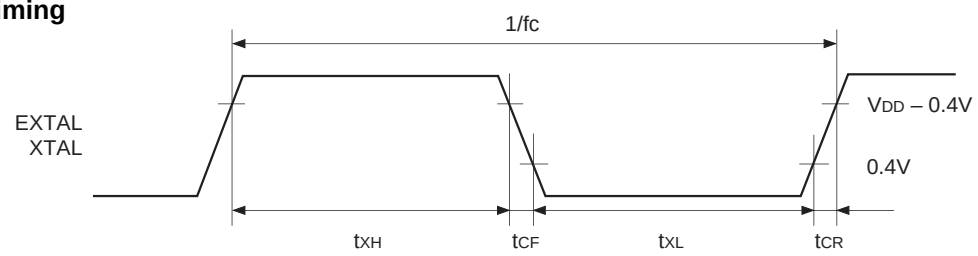


Fig. 2. Clock applied condition

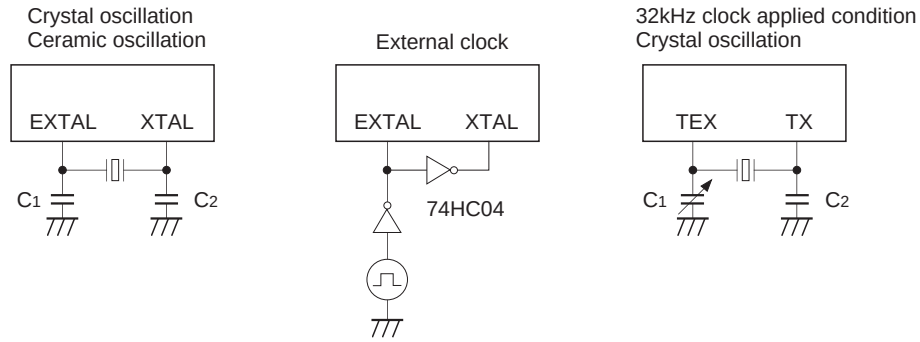
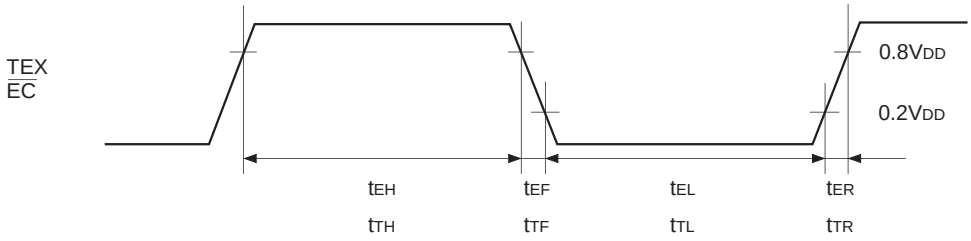


Fig. 3. Event count clock timing



(2) Serial transfer (CH0) (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

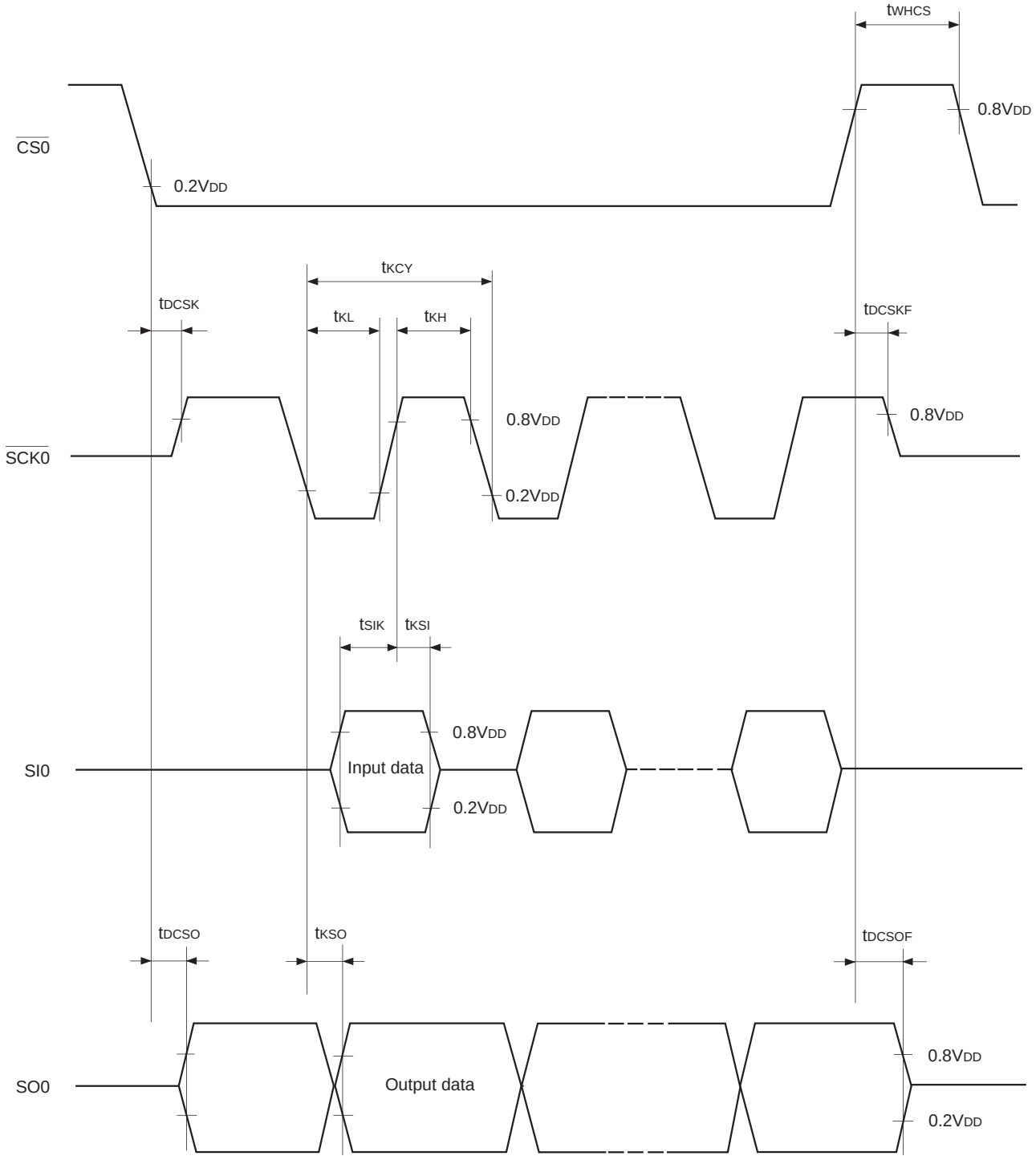
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0}\downarrow \rightarrow \overline{SCK0}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		tsys + 200	ns
$\overline{CS0}\uparrow \rightarrow \overline{SCK0}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		tsys + 200	ns
$\overline{CS0}\downarrow \rightarrow$ SO0 delay time	t_{DCSO}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS0}\uparrow \rightarrow$ SO0 floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS0}$ high level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK0}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys + 100		ns
			Output mode	8000/fc – 50		ns
SI0 input set-up time (against $\overline{SCK0}\uparrow$)	t_{SIK}	SI0	$\overline{SCK0}$ input mode	100		ns
			$\overline{SCK0}$ output mode	200		ns
SI0 input hold time (against $\overline{SCK0}\uparrow$)	t_{KSI}	SI0	$\overline{SCK0}$ input mode	tsys + 200		ns
			$\overline{SCK0}$ output mode	100		ns
$\overline{SCK0}\downarrow \rightarrow$ SO0 delay time	t_{KSO}	SO0	$\overline{SCK0}$ input mode		tsys + 200	ns
			$\overline{SCK0}$ output mode		100	ns

Note 1) tsys indicates three values according to the contents of the clock control register (CLC; $00FE_H$) upper 2 bits (CPU clock selection).

tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) The load of $\overline{SCK0}$ output mode and SO0 output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer timing (CH0)

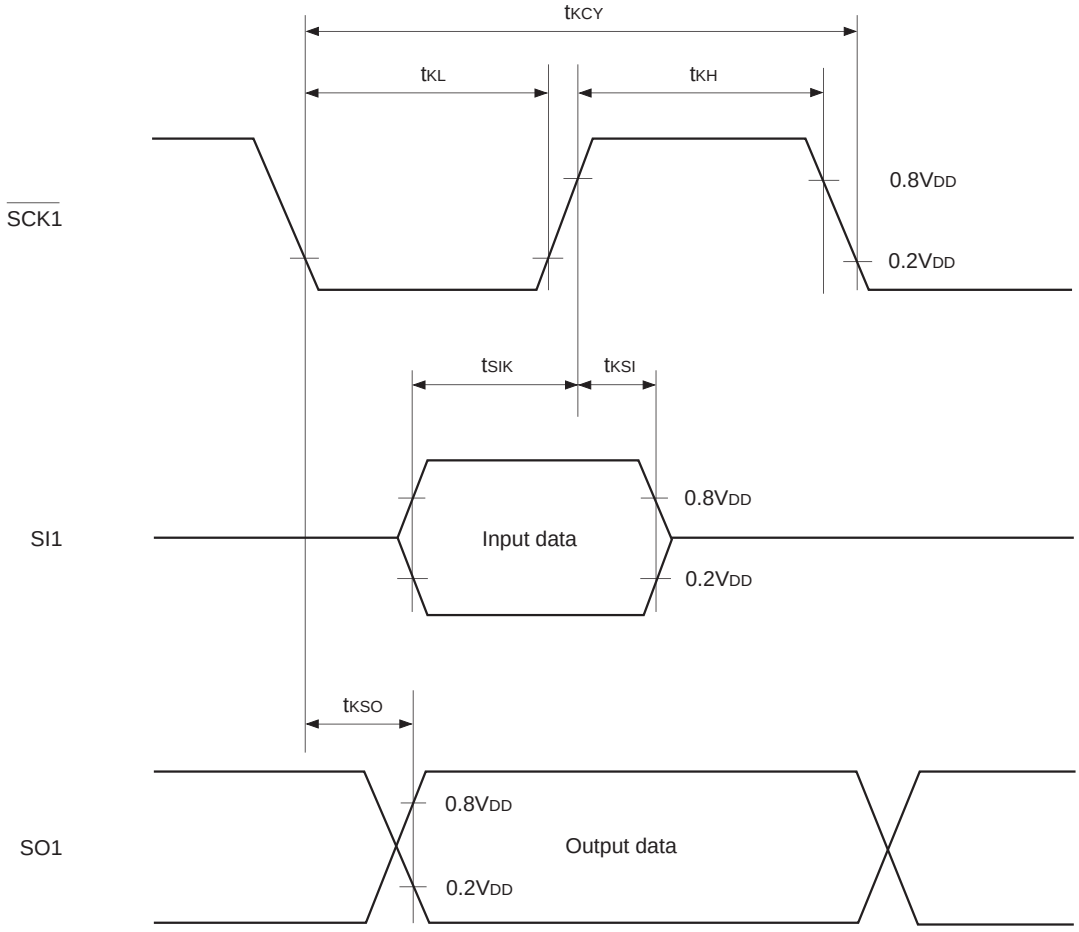


Serial transfer (CH1) (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	1000		ns
			Output mode	16000/fc		ns
$\overline{SCK1}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK1}$	Input mode	400		ns
			Output mode	8000/fc – 50		ns
SI1 input set-up time (against $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ output mode	200		ns
SI1 input hold time (against $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	200		ns
			$\overline{SCK1}$output mode	100		ns
$\overline{SCK1}$ ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		200	ns
			$\overline{SCK1}$ output mode		100	ns

Note) The load of $\overline{SCK1}$ output mode and SO1 output delay time is 50pF + 1TTL.

Fig. 5. Serial transfer timing (CH1)

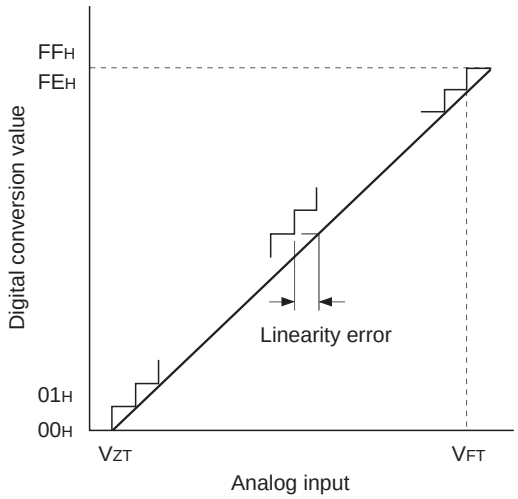


(3) A/D converter characteristics

(Ta = –10 to +75°C, V_{DD} = AV_{DD} = 4.5 to 5.5V, AV_{REF} = 4.0 to AV_{DD}, Vss = AVss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Only for A/D converter operation Ta = 25°C V_{DD} = AV_{DD} = AV_{REF} = 5.0V V_{DD} = AVss = 0V			±1	LSB
Absolute error						±2	LSB
Conversion time	t_{CONV}			160/f_{ADC} *1			µs
Sampling time	t_{SAMP}			12/f_{ADC} *1			µs
Reference input voltage	V_{REF}	AV_{REF}		AV_{DD} – 0.5		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN7		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operation mode		0.6	1.0	mA
			SLEEP mode STOP mode 32kHz operation mode			10	µA

Fig. 6. Definitions of A/D converter terms



*1) f_{ADC} indicates the below values due to the contents of bit 0 (ADCCK) of the ADC operation clock selection register (MSC: $01FF_H$), bits 7 (PCK1) and 6 (PCK0) of the clock control register (address: $00FE_H$).

ADCCK / PCK1, PCK0	0 (ϕ/2 selection)	1 (ϕselection)
00 (ϕ = f_{EX}/2)	f_{ADC} = fc/2	f_{ADC} = fc
01 (ϕ = f_{EX}/4)	f_{ADC} = fc/4	f_{ADC} = fc/2
11 (ϕ = f_{EX}/16)	f_{ADC} = fc/16	f_{ADC} = fc/8

(4) Interruption, reset input (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t_{IH} t_{IL}	$\overline{INT0}$ $\overline{INT1}$ $\overline{INT2}$ $\overline{NMI}$		1		µs
Reset input low level width	t_{RSL}	$\overline{RST}$		32/fc		µs

Fig. 7. Interruption input timing

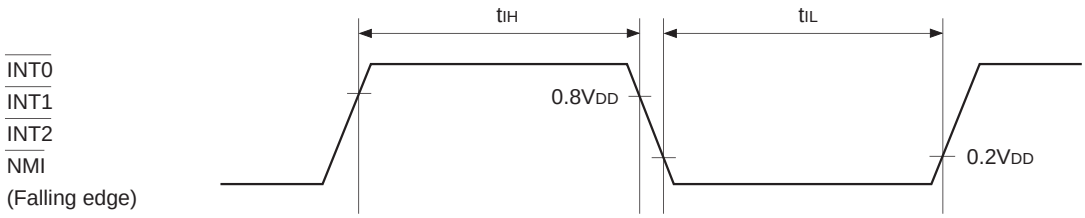
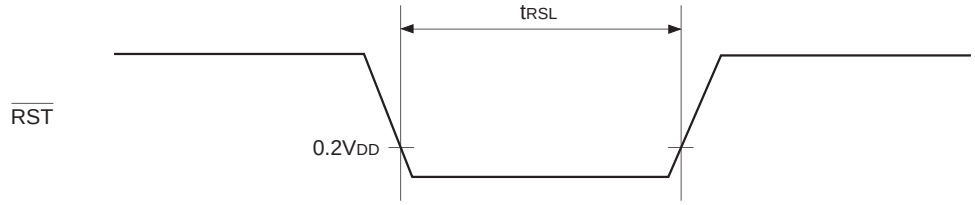


Fig. 8. Reset input timing



Analog Circuit Characteristics

(1) Amplifier circuit reference voltage characteristics

(Ta = –10 to +75°C, V_{DD} = $AMPV_{DD}$ = 5.0V, Vss = $AMPV_{SS}$ = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Reference level output voltage	V_{OR}	VREFOUT		2.2	2.4	2.6	V
		CTLAG		2.15	2.35	2.55	V
Reference level output current	I_{OR}	VREFOUT	VREFOUT = VREFOUT + 0.5V	3.50	6.5		mA
			VREFOUT = VREFOUT – 0.5V	–0.30	–0.85		mA
		CTLAG	CTLAG = CTLAG + 0.5V	2.80	5.5		mA
			CTLAG = CTLAG – 0.5V	–0.30	–0.85		mA

(2) CTL 1st amplifier characteristics

(Ta = –10 to +75°C, V_{DD} = $AMPV_{DD}$ = 5.0V, Vss = $AMPV_{SS}$ = 0V, CTLAG reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Voltage gain *1	A_{VCTL1}	RECCTL (+) CTLFAMPO*2	Gain = 16dB RECCTL (–) = 0V	12.5	14.5	16.5	dB
			Gain = 27dB RECCTL (–) = 0V	23.5	25.5	27.5	dB
			Gain = 42dB RECCTL (–) = 0V	39.0	41.5	44.0	dB
			Gain = 58dB RECCTL (–) = 0V	54.5	57.0	59.5	dB
Offset voltage	V_{OSCTL1}		CTLAMP (+) and CTLAMP (–) = open	–40	0	+40	mV
Input resistance	R_{INCTL1}	CTLAMP (+)	Charge switch OFF CTLAMP (+) = +0.2V	26.0	44.5		kΩ
		CTLAMP (–)	Charge switch OFF CTLAMP (–) = +0.2V	1.20	2.0		kΩ
Charge switch ON resistance	R_{CCTL1}	CTLAMP (+)	Charge switch ON CTLAMP (+) = +0.5V		560	1010	Ω
		CTLAMP (–)	Charge switch ON CTLAMP (–) = +0.5V		560	1010	Ω
RECCTL and CTLCIN connection switch ON resistance	R_{READ}	RECCTL (+) CTLCIN (+)	During CTL read operation, CTLCIN (+) – RECCTL (+) = 0.2V	315	400	770	Ω
		RECCTL (–) CTLCIN (–)	During CTL read operation, CTLCIN (–) – RECCTL (–) = 0.2V	315	400	770	Ω
CTLCIN 0V fix switch ON resistance	R_{WRITE}	CTLCIN (+)	During CTL write operation, CTLCIN (+) = $AMPV_{SS}$ + 0.2V		250	310	Ω
		CTLCIN (–)	During CTL write operation, CTLCIN (–) = $AMPV_{SS}$ + 0.2V		250	310	Ω

*1) When CTLCIN (+), CTLAMP (+) pins and CTLCIN (–), CTLAMP (–) pins are AC coupled, and then the signal is input from RECCTL (+) pin.

*2) The result after measuring the CTLFAMPO output waveform or voltage gain.

Note) The gain increases by approximately 1.5dB when the AC coupling capacitor (47µF) is connected to CTLAMP (+) and CTLAMP (–) pins, and the signal is input from CTLAMP (+) and CTLAMP (–) pins.

(3) CTL 2nd amplifier characteristics

(Ta = –10 to +75°C, V_{DD} = $AMPV_{DD}$ = 5.0V, Vss = $AMPV_{SS}$ = 0V, CTLAG reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Voltage gain*1, *2	A_{VCTL2}	CTLSAMPI	Gain = 5dB	4.8	5.8	6.8	dB
			Gain = 11dB	10.4	11.5	12.6	dB
			Gain = 16dB	15.3	16.5	17.7	dB
			Gain = 20dB	19.3	20.5	21.7	dB
LPF cut-off frequency *1, 2	f_{CCTL}		f_{DC} – 3dB	15.0	25.0	40.0	kHz
Offset voltage *2	V_{OSCTL2}		CTLSAMPI = open	–50	0	+50	mV
Comparator level *2	V_{CCTL}		Comparator level = +100mV0-p	70.0	100	130	mV0-p
			Comparator level = +250mV0-p	215	245	275	mV0-p
			Comparator level = +400mV0-p	370	400	430	mV0-p
			Comparator level = –100mV0-p	–70.0	–100	–130	mV0-p
			Comparator level = –250mV0-p	–220	–250	–280	mV0-p
			Comparator level = –400mV0-p	–370	–400	–430	mV0-p
Input resistance	R_{INCTL2}		Charge switch OFF CTLSAMPI = +0.2V	10.0	18.0		kΩ
Charge switch ON resistance	R_{CCTL2}		Charge switch ON CTLSAMPI = +0.5V		770	1140	Ω

*1) When the signal is input with the AC coupling capacitor (47µF) connected to CTLSAMPI pin.

*2) The result after measuring the output waveform of amplifier internal low-pass filter or voltage value.

(4) CTLAMP characteristics (1st amplifier + 2nd amplifier)

(Ta = –10 to +75°C, V_{DD} = $AMPV_{DD}$ = 5.0V, Vss = $AMPV_{SS}$ = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Voltage gain *1	A_{VCTL}	RECCTL (+)	CTL 1st amplifier gain = 16dB CTL 2nd amplifier gain = 20dB RECCTL (–) = 0V	31.8	35.0	38.2	dB
Input amplitude (peak value)	V_{PKCTL}		RECCTL (–) = 0V			±300	mV0-p
Input sensitivity	V_{SCTL}		CTL 1st amplifier gain = 58dB CTL 2nd amplifier gain = 20dB Comparator level = +400mV0-p –400mV0-p RECCTL (–) = 0V		0.08	0.10	mV0-p
Input dead band	V_{NSCTL}			0.015	0.04		mV0-p

*1) As for other combinations of the amplifier gains, CTL 1st amplifier and CTL 2nd amplifier are added respectively.

Note) The result when the signal is input from RECCTL (+) pin with CTL 1st amplifier + CTL 2nd amplifier after performing AC coupling of CTLCIN (+), CTLAMP (+) pins and CTLCIN (–), CTLAMP (–) pins, and CTLFAMPO, CTLSAMPI pins.

(5) CFGAMP characteristics

(Ta = –10 to +75°C, V_{DD} = $AMPV_{DD}$ = 5.0V, Vss = $AMPV_{DD}$ = 0V, VREFOUT reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Voltage gain *1, *2	A_{VCFG}	CFG	Gain = 0dB	–0.3	0.6	2.2	dB
			Gain = 20dB	19.2	20.8	22.4	dB
			Gain = 34dB	33.2	34.8	36.4	dB
			Gain = 38dB	37.0	38.7	40.4	dB
LPF cut-off frequency *1, *2	f_{CCFG}		f_{DC} – 3dB	30.0	55.0	80.0	kHz
Offset voltage *2	V_{OSCFG}		CFG = open	–50	0	+50	mV
Comparator judgment level width *2	V_{CCFG}		Comparator schimitt width = 320mVp-p	260	320	360	mVp-p
			Comparator schimitt width = 160mVp-p	110	155	200	mVp-p
Input sensitivity *1	V_{SCFG}		Gain = 38dB Comparator level = 320mVp-p		4.20	5.00	mVp-p
			Gain = 38dB Comparator level = 160mVp-p		2.10	2.40	mVp-p
Input dead band *1	V_{NSCFG}		Gain = 38dB Comparator level = 320mVp-p	3.40	4.10		mVp-p
			Gain = 38dB Comparator level = 160mVp-p	1.50	2.00		mVp-p
Input resistance	R_{INCFG}		Charge switch OFF CFG = +0.2V	5.5	8.3		kΩ
Charge switch ON resistance	R_{CCFG}		Charge switch ON CFG = +0.5V		455	710	Ω
Digital output waveform duty *1, *3	D_{TYCFG}		CFG = sine wave with 50% duty	48.0	50.0	52.0	%
Input amplitude (peak value) *1	V_{PKCFG}					±2.4	V_0-p

*1) When the signal is input with the AC coupling capacitor (47µF) connected to CFG pin.

*2) The result after measuring the output waveform of amplifier internal low-pass filter or voltage value.

*3) The result after measuring the digital signal waveform output from the amplifier circuit.

(6) DFGAMP characteristics

(Ta = –10 to +75°C, V_{DD} = $AMPV_{DD}$ = 5.0V, Vss = $AMPV_{SS}$ = 0V, VREFOUT reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Voltage gain *1, *2	A_{VDFG}	DFG	Gain = 0dB	–0.3	0.6	2.2	dB
			Gain = 20dB	19.2	20.8	22.4	dB
			Gain = 34dB	33.2	34.8	36.4	dB
			Gain = 38dB	37.0	38.7	40.4	dB
LPF cut-off frequency *1, *2	f_{CDFG}		f_{DC} – 3dB	30.0	55.0	80.0	kHz
Offset voltage *2	V_{OSDFG}		DFG = open	–50	0	+50	mV
Comparator judgment level width *2	V_{CDFG}		Comparator schmitt width = 320mVp-p	260	320	360	mVp-p
			Comparator schmitt width = 160mVp-p	110	155	200	mVp-p
Input sensitivity *1	V_{SDFG}		Gain = 38dB Comparator level = 320mVp-p		4.20	5.00	mVp-p
			Gain = 38dB Comparator level = 160mVp-p		2.10	2.40	mVp-p
Input dead band *1	V_{NSDFG}		Gain = 38dB Comparator level = 320mVp-p	3.40	4.10		mVp-p
			Gain = 38dB Comparator level = 160mVp-p	1.50	2.00		mVp-p
Input resistance	R_{INDFG}		Charge switch OFF DFG = +0.2V	5.5	8.3		kΩ
Charge switch ON resistance	R_{CDFG}		Charge switch ON DFG = +0.5V		455	710	Ω
Digital output waveform duty *1, 3	D_{TYDFG}		CFG = sine wave of 50% duty	48.0	50.0	52.0	%
Input amplitude (peak value) *1	V_{PKDFG}					±2.4	V_0-p

*1) When the signal is input with the AC coupling capacitor (47µF) connected to DFG pin.

*2) The result after measuring the output waveform of amplifier internal low-pass filter or voltage value.

*3) The result after measuring the digital signal waveform output from the amplifier circuit.

(7) DPGAMP characteristics

(Ta = –10 to +75°C, V_{DD} = $AMPV_{DD}$ = 5.0V, Vss = $AMPV_{SS}$ = 0V, VREFOUT reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Voltage gain *1, *2	A_{VDPG}	DPG		11.1	12.0	13.2	dB
LPF cut-off frequency *1, *2	f_{CDPG}		f_{DC} – 3dB	30.0	55.0	85.0	kHz
Offset voltage *2	V_{OSDPG}		DFG = open	–35	0	+35	mV
Comparator level *2	V_{CDPG}		Comparator level = 600mV_0-p	570	605	640	mV_0-p
			Comparator level = 400mV_0-p	370	400	432	mV_0-p
			Comparator level = 200mV_0-p	175	200	220	mV_0-p
			Comparator level = 100mV_0-p	72	100	125	mV_0-p
			Comparator level = –600mV_0-p	–572	–605	–643	mV_0-p
			Comparator level = –400mV_0-p	–368	–400	–438	mV_0-p
			Comparator level = –200mV_0-p	–174	–200	–223	mV_0-p
			Comparator level = –100mV_0-p	–71	–100	–124	mV_0-p
Input sensitivity *1	V_{SDPG}		Comparator level = 600mV_0-p, 200mV_0-p		150	180	mV_0-p
			Comparator level = 400mV_0-p, 100mV_0-p		100	120	mV_0-p
			Comparator level = –600mV_0-p, –200mV_0-p		–155	–185	mV_0-p
			Comparator level = –400mV_0-p, –100mV_0-p		–109	–130	mV_0-p
Input dead band *1	V_{NSDPG}		Comparator level = 600mV_0-p, 200mV_0-p	113	142		mV_0-p
			Comparator level = 400mV_0-p, 100mV_0-p	70	90		mV_0-p
			Comparator level = –600mV_0-p, –200mV_0-p	–120	–150		mV_0-p
			Comparator level = –400mV_0-p, –100mV_0-p	–80	–103		mV_0-p
Input resistance	R_{INDPG}		Charge switch OFF DPG = +0.2V	24.0	44.5		kΩ
Charge switch ON resistance	R_{CDPG}		Charge switch ON DPG = +0.5V		450	860	Ω
Input amplitude (peak value) *1	V_{PKDPG}					±2.4	V

*1) When the signal is input with the AC coupling capacitor (47µF) connected to DPG pin.

*2) The result after measuring the output waveform of amplifier internal low-pass filter or voltage value.

(8) CTL write circuit characteristics

(Ta = –10 to +75°C, V_{DD} = $AMPV_{DD}$ = 5.0V, Vss = $AMPV_{SS}$ = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Output resistance	R_{OH}	RECCAP	RECCAP = $AMPV_{DD}$ – 0.5V	450	625	1005	Ω
	R_{OL}		RECCAP = $AMPV_{DD}$ + 0.5V	410	555	840	Ω
Output current *1	I_{OREC}	RECCTL (+) RECCTL (–)	Write current = 2.0mA	1.3	2.0	2.9	mA
			Write current = 2.5mA	1.7	2.5	3.7	mA
			Write current = 3.0mA	2.1	3.1	4.5	mA
			Write current = 3.5mA	2.6	3.6	5.2	mA
			Write current = 4.0mA	2.9	4.0	5.9	mA
			Write current = 4.5mA	3.3	4.6	6.6	mA
			Write current = 5.0mA	3.7	5.1	7.2	mA
			Write current = 5.5mA	4.0	5.6	8.0	mA
			Write current = 6.0mA	4.4	6.1	8.9	mA

*1) The current value which flows when RECCTL (+) pin and RECCTL (–) pin are shorted.

(9) Amplifier operating current characteristics

(Ta = –10 to +75°C, V_{DD} = $AMPV_{DD}$ = 5.0V, Vss = $AMPV_{SS}$ = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Amplifier operating current	I_{AMP}	$AMPV_{DD}$	When the amplifier is operating *1		7.6	12.0	mA
			When the amplifier is not operating			10	µA

*1) The CTL recording current is added during CTL write.

Note) The amplifier operation and NOT-operation is controlled according to the contents of amplifier power supply control register (ASWC: $05E2_H$) bits 5, 4, 1 and 0.

Supplement

Fig. 9. Recommended oscillation circuit

Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00	5	5		
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16 (12)	16 (12)	0	(i)
		10.00	16 (12)	16 (12)		
		12.00	12	12		
		16.00	12	12		
	P3	32.768kHz	30	18	470k	(ii)

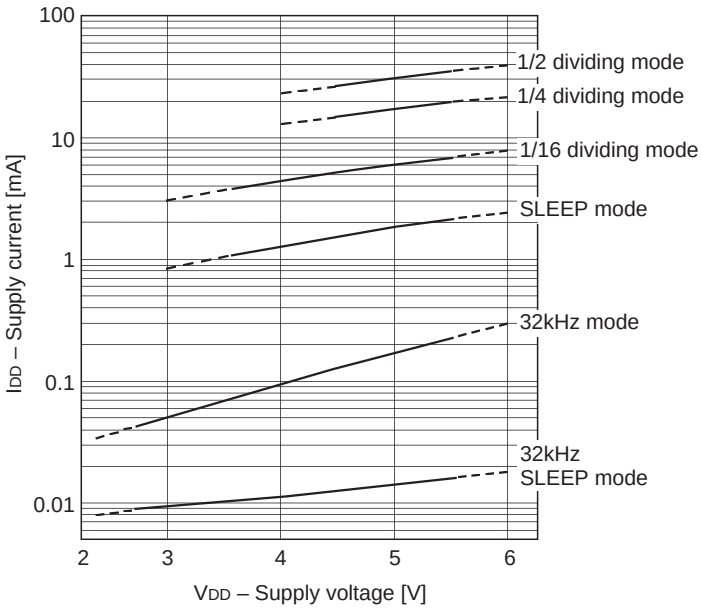
Mask option table

Item	Mask product	CXP888P60Q-1-□□□	CXO888P60Q-2-□□□
Reset pin pull-up resistor	Existent/Non-existent	Existent	Existent
Input circuit format*1	CMOS schmitt/ TTL schmitt	TTL schmitt	TTL schmitt
Power-on-reset circuit	Existent (CXP88616/24) Non-existent (CXP88732/40/48, CXP88852/60)	Non-existent	Existent

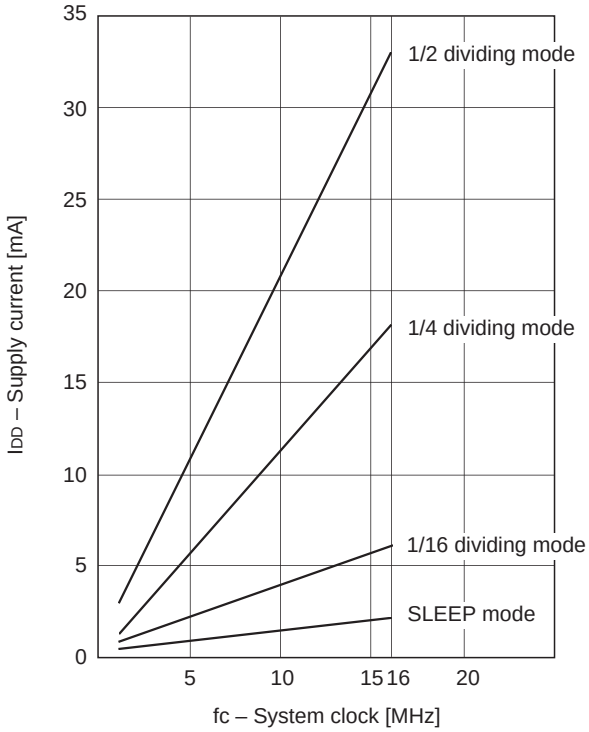
*1) The input circuit format can be selected for PE3/SYNC pin.

Characteristics Curve

IDD vs. VDD
(fc = 16MHz, Ta = 25°C, Typical)

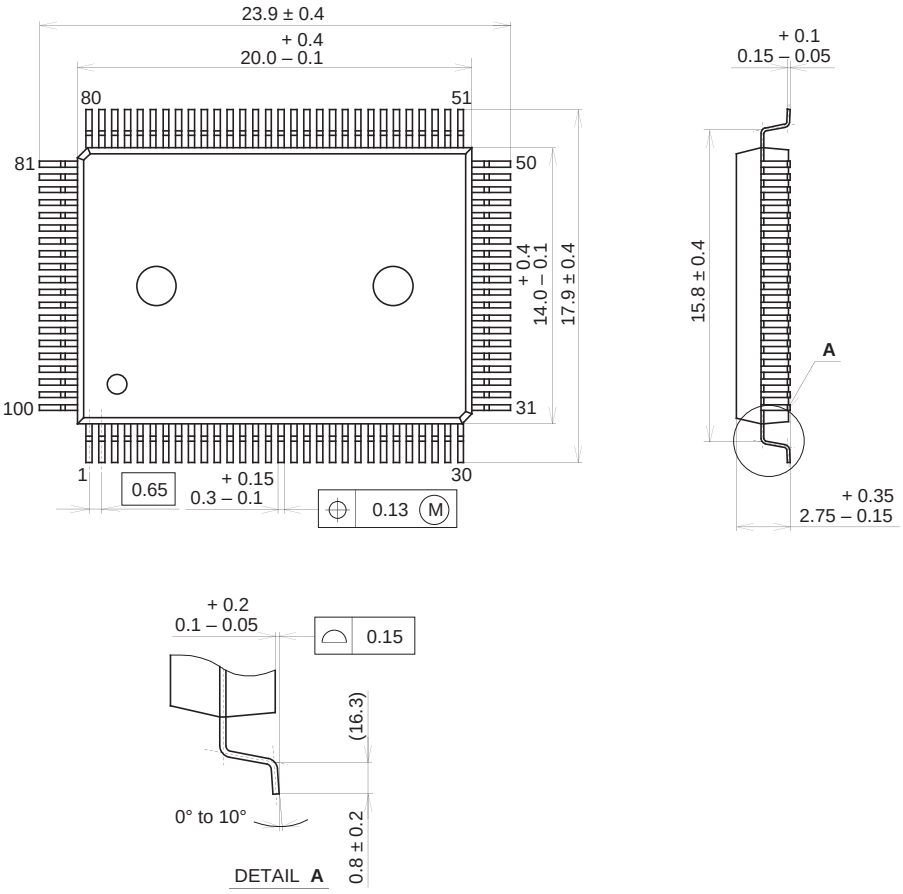


IDD vs. fc
(VDD = 5.0V, Ta = 25°C, Typical)



Package Outline Unit: mm

100PIN QFP (PLASTIC)



PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	————