16,384 word × 4-bit High Speed CMOS Static RAM

Description

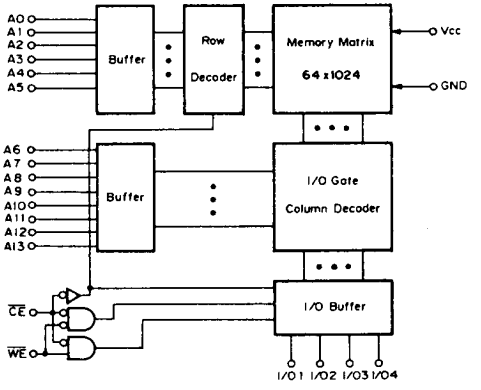
CXK5466P/J is a high speed CMOS static RAM with TTL compatible I/O organized as 16,384 words × 4 bits.

This IC operating on a single 5V supply turns to power down mode at no select time by means of chip enable signal.

Features

- Fast access time :
  CXK5466P/J-15 15ns (Max.)
  CXK5466P/J-20 20ns (Max.)
- Low power consumption : 150mW (Typ.)
  During operation
- Single +5V supply : +5V ± 10%
- Fully static memory
  ···No clock or timing strobe required
- Equal access and cycle time
- Common data input and output :
  three-state output
- Directly TTL compatible :
  All inputs and outputs
- Compatible with various types of packages
- High density : 300 mil 22 pin plastic DIP
  300 mil 24 pin plastic SOJ

Block Diagram



CXK5466P
22 pin DIP (Plastic)

CXK5466J
24 pin SOJ (Plastic)

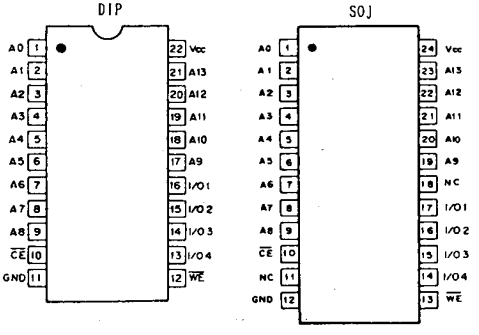
Functions

16,384 word × 4-bit static RAM

Structure

Silicon gate CMOS IC

Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A13	Address input
I/O1 to I/O4	Data input/output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
Vcc	+5V power supply
GND	Ground
NC	No connection

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Absolute Maximum Ratings (Ta = 25°C, GND = 0V)

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	− 0.5* to + 7.0	V
Input voltage	V_{IN}	− 0.5* to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$	− 0.5* to V_{CC} + 0.5	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	Topr	0 to + 70	°C
Storage temperature	Tstg	− 55 to + 150	°C
Soldering temperature • time	Tsolder	260 • 10	°C • sec

* V_{CC}, V_{IN}, $V_{I/O}$ Min. = − 3.5V for pulse width less than 20ns.

Truth Table

$\overline{CE}$	$\overline{WE}$	Mode	I/O1 to I/O4	V_{CC} current
H	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	Read	Data output	I_{CC1}, I_{CC2}
L	L	Write	Data input	I_{CC1}, I_{CC2}

× : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to + 70°C, GND = 0V)

Item	Symbol	Min.	Typ.*1	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	——	V_{CC} + 0.3	V
Input low voltage	V_{IL}	− 0.3*2	——	0.8	V

*1) V_{CC} = 5V, Ta = 25°C
*2) V_{IL} Min. = − 3.0V for pulse width less than 20ns.

5

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DC Electrical Characteristics

• DC and operating characteristics (Vcc = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test Conditions		Min.	Typ.*	Max.	Unit
Input leak current	I_{LI}	V_{IN} = GND to Vcc		−1	—	1	μA
Output leak current	I_{LO}	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to Vcc		−1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA, V_{IN} = V_{IH} or V_{IL}		—	30	55	mA
Average operating current	I_{CC2}	Cycle = Min., Duty = 100%, I_{OUT} = 0mA	−15	—	95	150	mA
			−20	—	90	140	mA
Standby current	I_{SB1}	$\overline{CE}$ ≧ Vcc − 0.2V, V_{IN} ≧ Vcc − 0.2V or V_{IN} ≦ 0.2V		—	—	1	mA
	I_{SB2}	$\overline{CE}$ = V_{IH}, V_{IN} = V_{IH}/V_{IL} Cycle = Min.		—	—	85	mA
Output high voltage	V_{OH}	I_{OH} = −4.0mA		2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0mA		—	—	0.4	V

* Vcc = 5.0V, Ta = 25°C

I/O capacitance (Ta = 25°C, f = 1MHz)

Item	Symbol	Test Conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

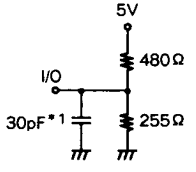
AC characteristics

• AC test conditions

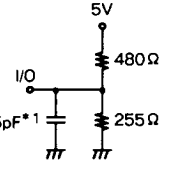
(Vcc = 5V ± 10%, Ta = 0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH} = 3.0V
Input pulse low level	V_{IL} = 0V
Input rise time	tr = 5ns
Input fall time	tf = 5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)*2



*1 including scope and jig capacitance
*2 for t_{LZ}, t_{HZ}, t_{OW}, t_{WHZ}

Fig. 1

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• **Read cycle**

Item	Symbol	−15		−20		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	15	—	20	—	ns
Address access time	t_{AA}	—	15	—	20	ns
Chip enable access time ($\overline{CE}$)	t_{CO}	—	15	—	20	ns
Output hold from address change	t_{OH}	3	—	3	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	2	—	3	—	ns
Chip disable to output in high Z	t_{HZ}*	0	6	0	8	ns
Chip enable to power up time	t_{PU}	0	—	0	—	ns
Chip disable to power down time	t_{PD}	—	15	—	20	ns

* Transition is tested by means of load conditions (2), from stationary condition at ±200mV (See Fig. 1)

• **Write cycle**

Item	Symbol	−15		−20		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	15	—	20	—	ns
Address valid to end of write	t_{AW}	13	—	18	—	ns
Chip enable to end of write	t_{CW}	13	—	18	—	ns
Data to write time overlap	t_{DW}	8	—	11	—	ns
Data hold from write time	t_{DH}	0	—	0	—	ns
Write pulse width	t_{WP}	13	—	18	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write recovery time	t_{WR}	0	—	0	—	ns
Output active from end of write	t_{OW}*	2	—	3	—	ns
Write to output in high Z	t_{WHZ}*	0	5	0	7	ns

* Transition is tested by means of load conditions (2), from stationary condition at ±200mV (See Fig. 1)

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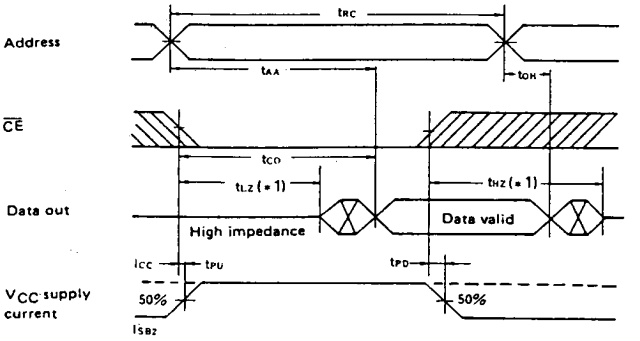
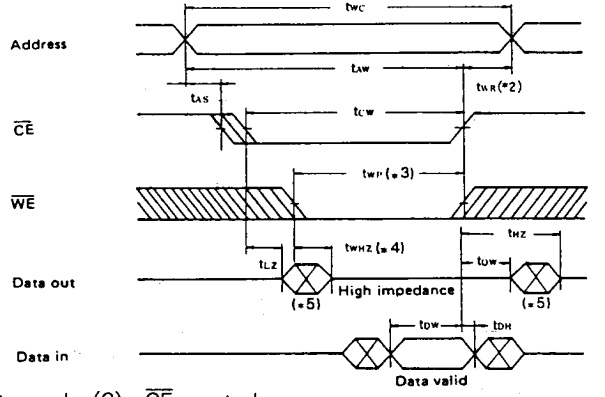
Timing Waveform

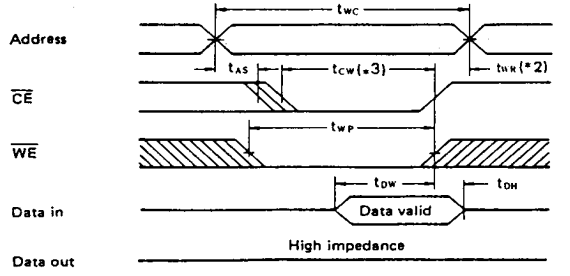
• Read cycle : $\overline{WE}$ = V_{IH}



• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE}$ control



*1) Whatever the conditions, t_{HZ} is smaller than t_{LZ}.

*2) t_{WR} is tested from either $\overline{CE}$ or $\overline{WE}$ rise, whichever comes earlier, until the end of write cycle.

*3) Write is performed when both $\overline{CE}$ and $\overline{WE}$ are in the low overlap.

*4) When $\overline{WE}$ fall is performed simultaneously with $\overline{CE}$ fall, or before, output is kept to high impedance.

*5) While I/O pins are in output state, do not apply data input signals with a phase opposite to that of the output.

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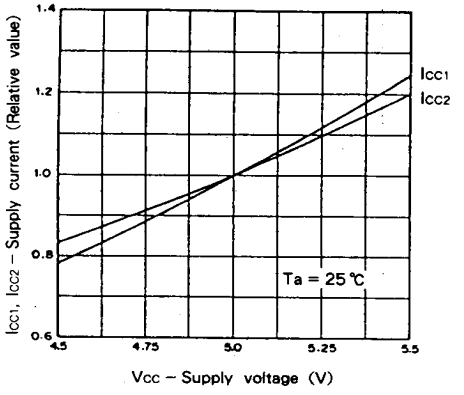
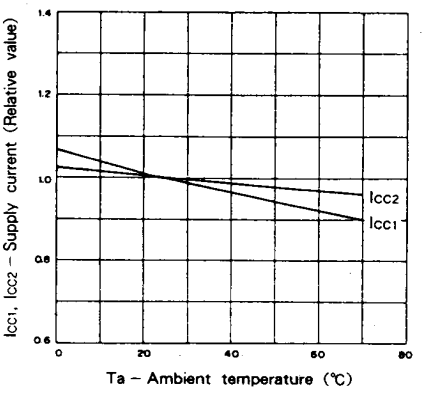
Example of Represeutative Characteristics

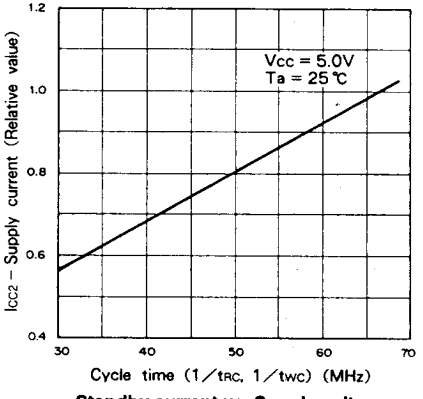
Supply current vs. Supply voltage



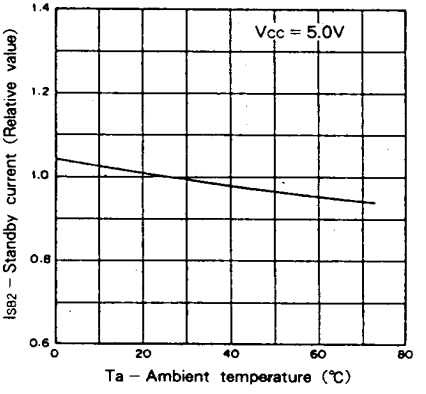
Supply current vs. Ambient temperature



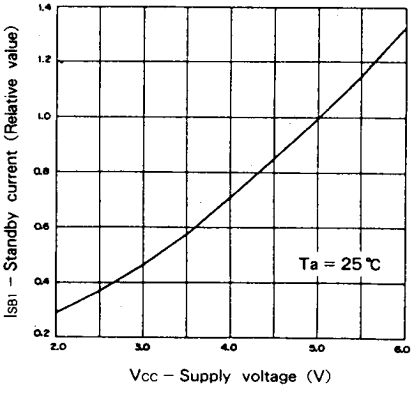
Supply current vs. Cycle time



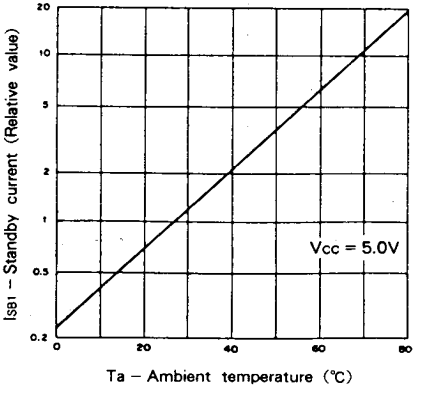
Standby current vs. Ambient temperature



Standby current vs. Supply voltage



Standby current vs. Ambient temperature



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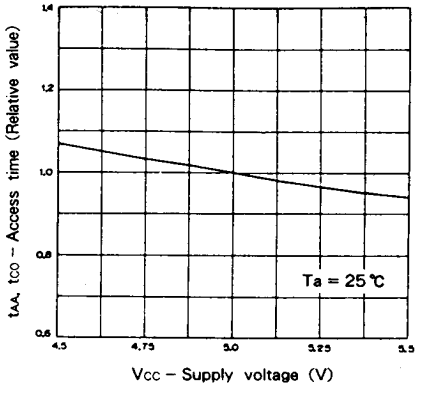
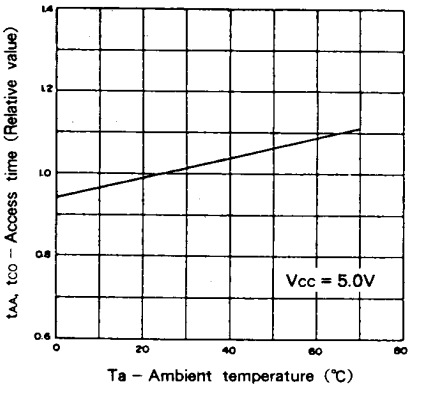
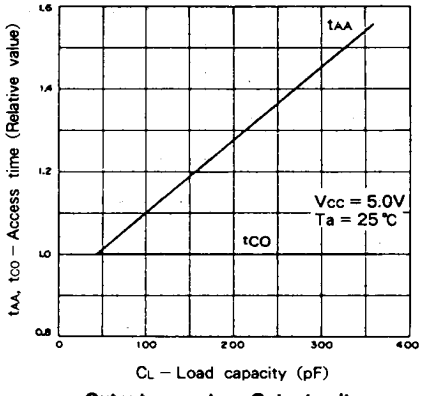
Access time vs. Supply voltage



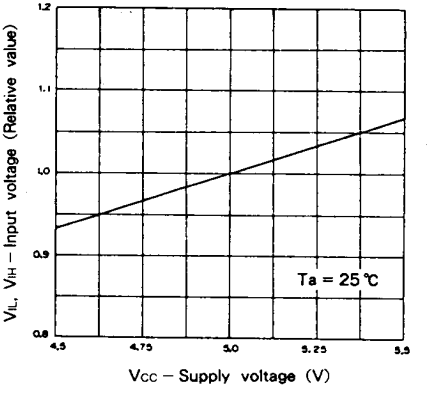
Access time vs. Ambient temperature



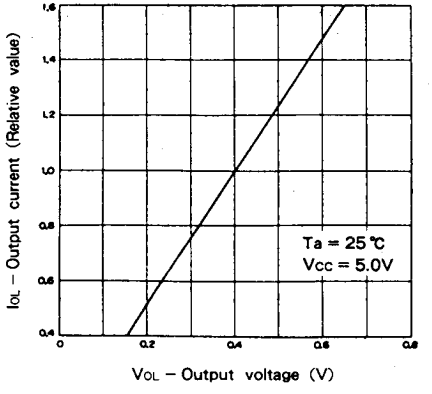
Access time vs. Load capacity



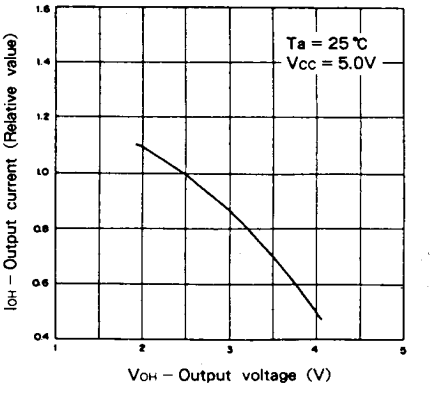
Input voltage vs. Supply voltage



Output current vs. Output voltage



Output current vs. Output voltage



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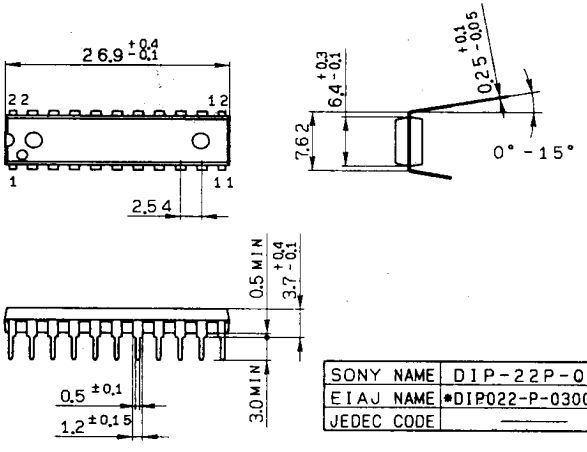
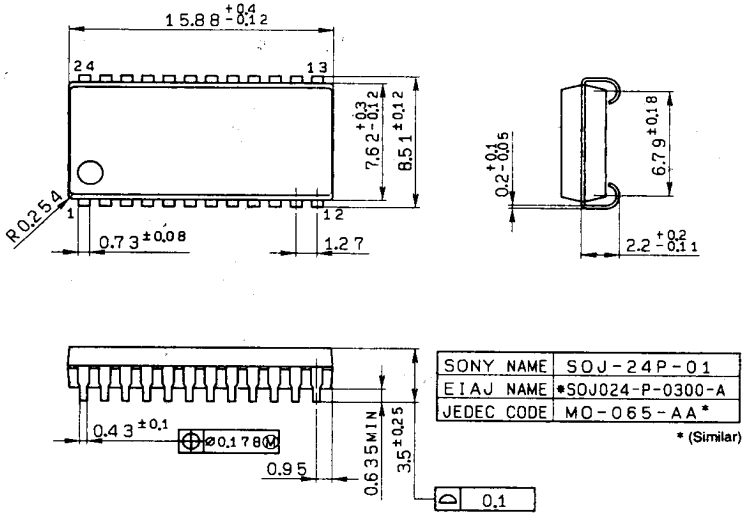
Package Outline Unit : mm

CXK5466P 22 pin DIP (Plastic) 300mil 1.3g



SONY NAME	DIP-22P-02
EIAJ NAME	*DIP022-P-0300-A
JEDEC CODE	———

CXK5466J 24 pin SOJ (Plastic) 300mil 0.7g



SONY NAME	SOJ-24P-01
EIAJ NAME	*SOJ024-P-0300-A
JEDEC CODE	MO-065-AA*

* (Similar)

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