# Very High Speed 14-Bit, 20 MHz Sampling A/D Converter

In a Space-saving 46-pin Hybrid Package

Introduction

The Analogic ADC3121 is a complete 14-bit, 20 MHz sampling A/D converter subsystem in a space-saving 46-pin hybrid package. It is designed for frequency domain applications requiring high speed and high resolution front ends such as ATE, medical imaging, radar, I/Q Quadrature demodulators and digital receivers. With sampling rates from 10 MHz to 20 MHz, the ADC3121 is capable of 81 dB SFDR and 72 dB SNR. Although fully characterized in the frequency domain, the ADC3121 works equally well in applications requiring low noise and fast front end settling times such as CCD detectors. The built-in sample-and-hold amplifier will settle to within one LSB in less than one conversion.

The ADC3121 utilizes the latest semiconductor technologies to produce a cost-effective, high performance part in a 46 pin hybrid package. It is designed around a pipelined subranging architecture that integrates a pair of low-distortion, sample-and-hold amplifiers, a 3-bit, 14-bit accurate flash/DAC, a high-speed, 12-bit sampling ADC, all necessary timing circuitry and ECL-compatible output lines for ease of system integration. The superior performance of the ADC3121 is due, in no small part, to the input sample-and-hold amplifier. It is a proprietary custom monolithic chip capable of settling to ±0.003% in just 25 ns! During the initial research, all the potential error sources were well defined and each was considered one at a time. A worst case analysis was performed and scrutinized closely. The result is a 10 MHz to 20 MHz sampling ADC with 81 dB SFDR and 72 dB SNR.
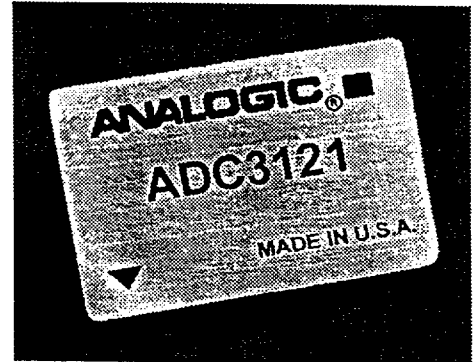
Features

❑ Built-in S/H Amplifier
❑ 14-Bit Resolution
❑ 20 MHz Sampling Rate
❑ 0.006% Integral Nonlinearity
❑ 81 dB SFDR
❑ 72 dB SNR
❑ ECL Compatibility
❑ 46 Pin Hybrid DIP

Applications

❑ Digital Signal Processing
❑ ATE
❑ Medical Imaging
❑ CCD Detectors
❑ IR Imaging
❑ Radar
❑ Digital Receivers
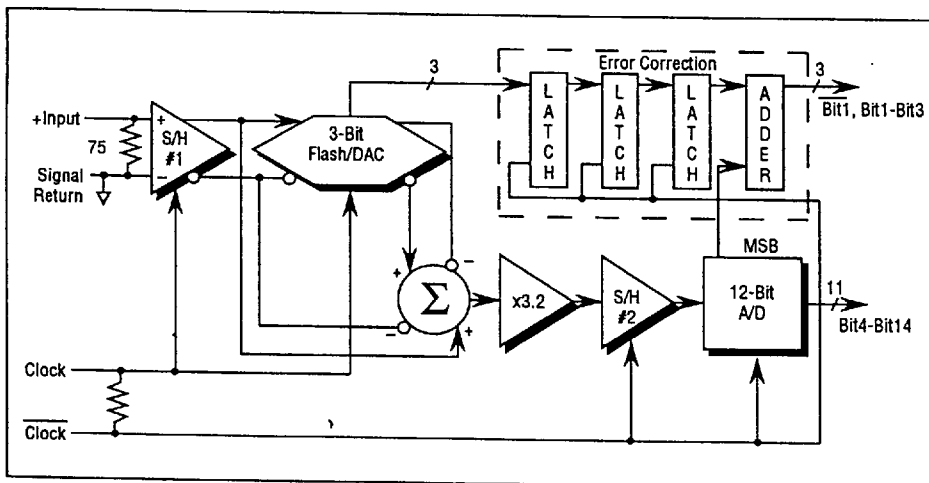❑ I/Q Quadrature Demodulators

Figure 1. ADC3121 Functional Block Diagram.

ANALOGIC.
**The World Resource
for Precision Signal Technology**

ANALOG INPUT

Input Voltage Range
Bipolar
±1.280V

Maximum Input Without Damage
+5.25V
−5.45V

Input Resistance
75Ω Typ.

Input Capacitance
5 pF Typ.

CLOCK INPUT

Compatibility
ECL

Logic "0"
−1.5V Max.

Logic "1"
−1.1V Min.

Loading
100Ω Typ.

CLOCK
(Complementary Inputs)
Positive Edge of CLOCK Puts S/H #1
into Hold

Duty Cycle
50% ±10%

DATA OUTPUTS

Fan-Out
1 ECL Load

Logic "0"
−1.5V Max.

Logic "1"
−1.1V Min.

Output Coding [2]
Offset binary, 2's Complement

TRANSFER CHARACTERISTICS

Resolution
14 bits

Integral Nonlinearity
±0.006% Max.

Differential Nonlinearity
±0.75 LSB Max.

Monotonicity
Guaranteed

No Missing Codes
Guaranteed over specified temperature range

Noise
205 µV RMS Typ.

Offset
TBD

Gain
TBD

DYNAMIC CHARACTERISTICS

	(10 MHz Sampling)	(20 MHz Sampling)
S/H Aperture Delay	5 ns Max.	5 ns Max.
S/H Aperture Uncertainty	1 ps RMS Max.	1 ps RMS Max.
S/H Feedthrough	−90 dB Max.	−90 dB Max.
Full Power Bandwidth	80 MHz Max.	80 MHz Max.
Small Signal Bandwidth	80 MHz Min.	80 MHz Min.
Signal to Noise Ratio DC to 10 MHz Input @ −1 dB	70 dB Min., 72.5 dB Typ.	70 dB Min., 72.5 dB Typ.
Spurious Free Dynamic Range 2 MHz Input @ −0.5 dB	81 dB Min., 85 dB Typ.	79 dB Min., 82 dB Typ.
Spurious Free Dynamic Range 4.8 MHz Input @ −0.5 dB	81 dB Min., 84 dB Typ.	73 dB Min., 75 dB Typ.
Total Harmonic Distortion 2 MHz Input @ −0.5 dB	−78 dB Max.	−74 dB Max.
Total Harmonic Distortion 4.8 MHz Input @ −0.5 dB	−78 dB Max.	−70 dB Max.

POWER REQUIREMENTS

±15V Supplies (±3%)
27 mA Typ.

−15V Supplies (±3%)
14 mA Typ.

+5V Supply (±5%)
285 mA Typ

−5.2V Supply
601 mA Typ

Total Power Consumption
5.2W Typ.

ENVIRONMENTAL & MECHANICAL

Specified Temperature Range [3]
0°C to +70°C

Storage Temperature Range
−40°C to 125°C

Dimensions
1.6" x 2.4" x 0.225"
(40,64 mm x 60.96 mm x
5.715 mm)

Thermal Impedance
θAC = 10°C/W Typ.

Heat Sink Recommendations
Aluminum Block, 2.35" x 1" x 0.14"
(59.7 mm x 25.4 mm x 3.56 mm), or
Gap Pad on Ground Plane
(1.5 to 2 oz copper clad ground plane)

NOTES
1. All specifications guaranteed at 50°C case temperature unless otherwise noted.
2. For 2's Complement operation, simply use $\overline{\text{BIT 1}}$ instead of BIT 1.
3. Specified temperature is guaranteed for case temperature.

Specifications subject to change without notice.

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The Analogic ADC3121 is a very high speed, very accurate sampling A/D converter. Achieving 20 MHz throughput rates with the 14-bit accuracy required maintaining very high bandwidths in most of the internal circuits. Preserving the accuracy of the ADC3121 under these conditions requires careful attention to design and layout considerations.

layout Information

The recommended grounding scheme for the ADC3121 is the use of a single low impedance ground plane on the component side of the printed circuit board. It becomes the common point for all analog, digital and signal returns. (See Figures 2a. and 2b.) All power supply returns should return separately to the respective supplies. All analog paths must be kept as short as possible and away from digital lines. The digital lines should also be kept short with differential lines equal in length to avoid propagation delay mismatching.
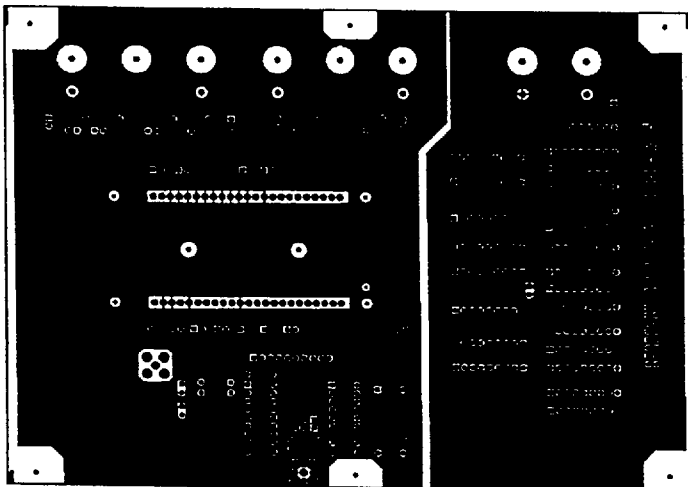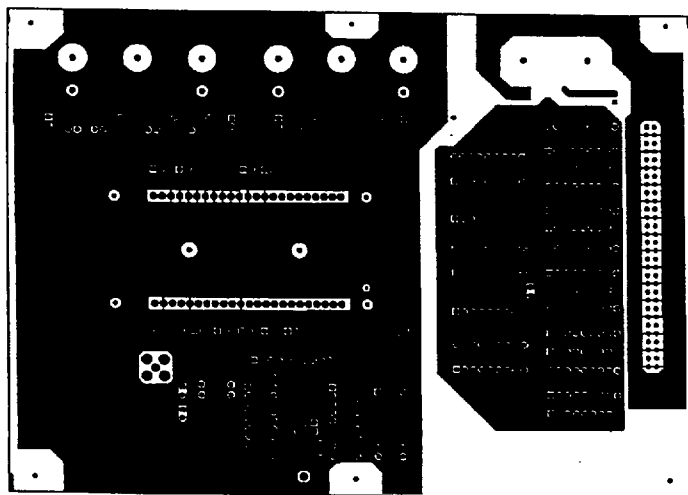

Figure 2a. ADC3120-EB1 Primary Side Layout.

Figure 2b. ADC3120-EB1 Secondary Side Layout.

Bypassing the ADC3121

All power supply inputs should be individually bypassed to ground with 10 µF, 35V tantalum capacitors at the input to the board, followed by 25 µH toroid inductors. Toroids are preferable over the axial type as they minimize radiation.
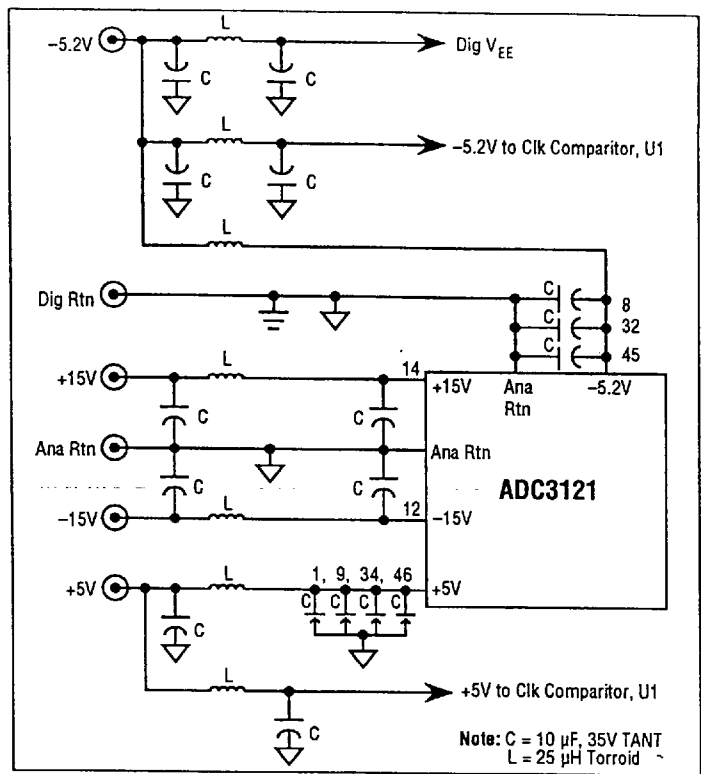

Figure 3. Bypassing the ADC3121.

To further reduce the effects of radiation, the toroid should be placed away from the ADC3121 and as near to the power supply inputs to the board as possible. Additionally, all power pins of the ADC3121 must be bypassed at the ADC input. (See Figure 3.)

Timing

The clock input to the ADC3121 is ECL compatible with conversion initiated on the rising edge of CLK. Data is available after a 3 1/2 clock pulse delay. (See Figure 4.) As the falling edge of CLK is also critical to the timing sequence, care must be taken to keep the duty cycle to 50%, ±10%, and it must be jitter free. As in any sampling ADC, the clock will act as a wide bandwidth analog input. With a 10 MHz input, a 1 pS jitter will cause an 80 µV error (1/2 LSB). The Circuitry shown in Figure 5 will help minimize the effects of jitter by cleaning the clock edges and will also allow the use of a TTL input.
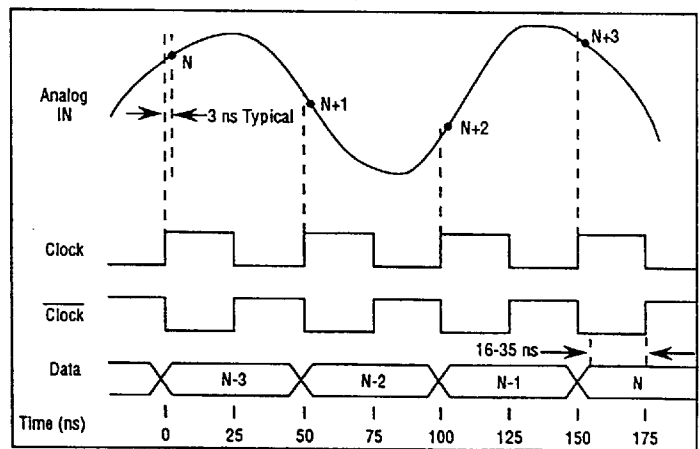

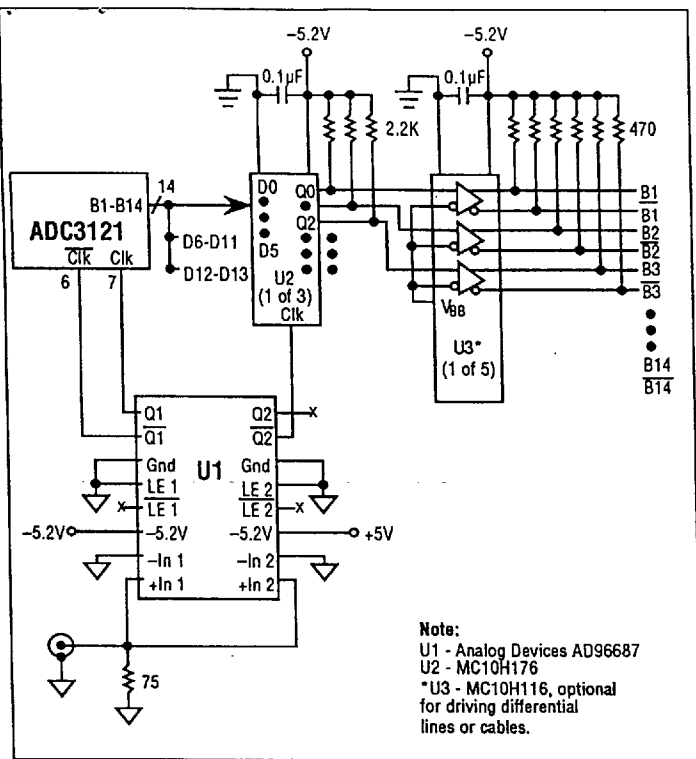
Figure 4. ADC3121 Timing Diagram.

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Figure 5. Suggested Clock and Data Interface Circuitry.

Note:
U1 - Analog Devices AD96687
U2 - MC10H176
*U3 - MC10H116, optional
for driving differential
lines or cables.

Figure 7. ADC3121 Mechanical Dimensions.

Analog Input

Taking full advantage of the dynamic range of the ADC3121 requires a ±1.280V full scale, analog input signal capable of driving 75Ω. The analog input to the ADC3121 has as a minimum, an 80 MHz bandwidth. For this reason, Analogic recommends the use of a low-pass or band-pass filter with 75Ω termination. If a 50Ω system is required, the use of an external 150Ω, ±1%, film resistor across the input is advised.

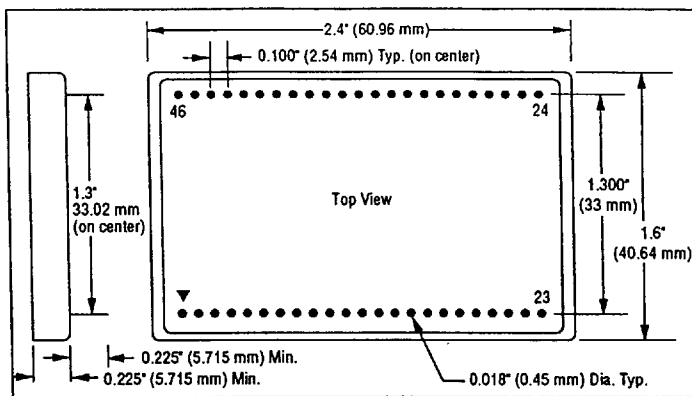| Pin #	Assignment	Pin #	Assignment
1	+5V	46	+5V
2	ANA RTN	45	–5.2V
3	SIG RTN	44	ANA RTN
4	SIG IN	43	ANA RTN
5	ANA RTN	42	ANA RTN
6	$\overline{CLK}$	41	ANA RTN
7	CLK	40	ANA RTN
8	–5.2V	39	ANA RTN
9	+5V	38	ANA RTN
10	N.C.	37	ANA RTN
11	ANA RTN	36	DIG RTN
12	–15V	35	DIG RTN
13	N.C.	34	+5V
14	+15V	33	ANA RTN
15	ANA RTN	32	–5.2V
16	ANA RTN	31	$\overline{BIT\ 1}$
17	BIT 14	30	BIT 1
18	BIT 13	29	BIT 2
19	BIT 12	28	BIT 3
20	BIT 11	27	BIT 4
21	BIT 10	26	BIT 5
22	BIT 9	25	BIT 6
23	BIT 8	24	BIT 7

Figure 6. ADC3121 Pin Assignment.

Data Interface

Isolating the ADC3121 from digital perturbations and excessive capacitance at the data output lines is important in maintaining dynamic performance. The ADC3121 ECL compatible data outputs have designed in 1KΩ series resistors, providing that required isolation. The lengths of the data output lines and the associated loading must therefore be minimized. An ECL to TTL translator or the Flip Flops seen in Figure 5 should be utilized. Figure 5 depicts suggested circuitry for driving most differential requirements or twisted pair ribbon cable.

PRINCIPLE OF OPERATION

The ADC3121 is a 14-bit sampling A/D converter that utilizes a two-pass, sub-ranging, pipelined architecture to achieve sampling rates from 10 MHz to 20 MHz. The analog input range is ±1.280V and is converted to an offset binary, or 2's complement data format.

To understand the operating principles of the ADC3121, refer to the Functional Block Diagram of Figure 1 and Timing Diagram of Figure 4. Analog input signals up to 10 MHz, are captured by a low-noise, low-distortion, S/H amplifier, S/H #1. S/H #1 drives both a three-bit flash DAC (14-bit linear) and the summing junction of a residue amplifier. The three MSBs of the flash/DAC are latched into the first of three registers within the error correction logic. The flash DAC will produce an analog voltage equal to the analog input of the ADC3121 to within three bits of resolution or an error voltage equal to 320 mV P-P. (It is critical that the flash DAC be at least 14-bit linear, as any error source will add directly to the 3-bit quantization error at the summing junction.) The flash DAC analog output result is summed with the S/H #1 analog output at the summing junction input of the residue amplifier. This completes the first pass.

The second pass starts with the residue amplifier. It amplifies the error voltage by 3.2 (0.32 x 3.2 = 1.024 Vp-p) to use 11 bits of the 12-bit ADC. S/H #2 is put into hold and the ADC is then clocked. The eleven LSBs are latched into the output logic (after two additional clocks) and the MSB is latched into the error correction logic to be summed with the three MSBs of the first pass creating a one bit overlap. This overlap corrects for any gain and linearity errors in the amplifying circuit. This completes the second pass.

Within the 12-bit ADC, there exists a 2 clock pipelined delay before the N data is available. To compensate for this delay, the three MSBs from the flash DAC must be de-

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layed by 3 clocks to be in phase with the second pass. This is accomplished with three data latches within the error correction logic followed by a 1/2 clock adder delay. Collectively, this creates a 3-1/2 clock pipelined delay from N clock to available N data (see Figure 4).

PERFORMANCE TESTING

To further instill confidence in our customers, Analogic supplies a test data sheet with each analog-to-digital (A/D) converter as proof of 100% testing performed on each device prior to shipping. Such data sheets reflect testing performed both in the "Frequency Domain" and in the "Amplitude Domain." The methods of testing A/D converters have developed significantly over the past decade to keep pace with the increased precision and speed of these converters. Not only have more of the testing methods become automated, but the demands on this automatic test equipment have increased significantly to test 14-bit performance fully in both the "Amplitude Domain" and the "Frequency Domain". In particular, testing A/D converters in the frequency domain has become a critical issue for many applications.

Analogic, one of the world leaders in data conversion technology, has developed automatic test systems for testing its family of 14-bit A/D converters in the amplitude and frequency domains. These testers were designed in conjunction with our engineering development effort on Analogic's family of high speed, high resolution A/D converters, since these converters perform beyond the testing capability of commercially available testers. Analogic's testers are used to perform a rigorous and exhaustive set of tests on each and every unit shipped by Analogic, assuring the customer that each unit meets or exceeds our published specifications.
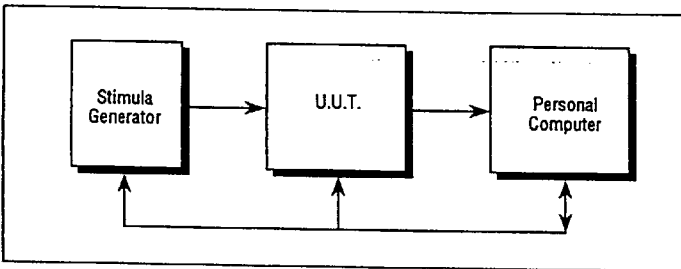

Figure 8. Amplitude Domain Test System.

Amplitude Domain Testing

Analogic's Amplitude Domain Test System, a simplified block diagram of which is shown in Figure 8, is controlled by a host computer and includes a 22-bit digital-to-analog converter, with accuracy and linearity far exceeding the requirements for testing 14-bit A/D converters. The reference for the D/A converter is traceable to the National Institute of Standards Technology. This degree of accuracy is essential for amplitude domain testing of A/D converters to the 18-bit level.

With this system, Analogic tests such parameters as integral linearity, dynamic differential linearity, A/D converter noise, conversion time, gain error, offset error, power supply current, and power supply rejection. The test system measures code transition voltages over the full range of the A/D converter and builds a histogram. Typical Amplitude Domain data sheet is shown in Figure 10.

Frequency Domain Testing

Many of the applications that use Analogic's high performance A/D converters, such as telecommunications, sonar and radar, require frequency domain test data.

A proprietary ADC spectral test station designed and manufactured by Analogic Corporation provides the frequency domain characterization for the sampling ADCs (see Figure 9). This test station consists of a pair of low noise, low jitter, synthesized generators. One generator uses a narrow bandpass filter to create a clean input signal. The second generator, in conjunction with signal conditioning and an ECL Comparator, produces an extremely low jitter trigger signal. The need for a "windowing" algorithm is eliminated with a precise, coherent relationship between the two generators. This is critical in determining spectral characterization without the windowing side effects.

The resulting FFT data (See Figure 11 for the Test Data Sheet) is a spectral representation of the raw data generated by the test station and the device under test. It has not been massaged by a window function.
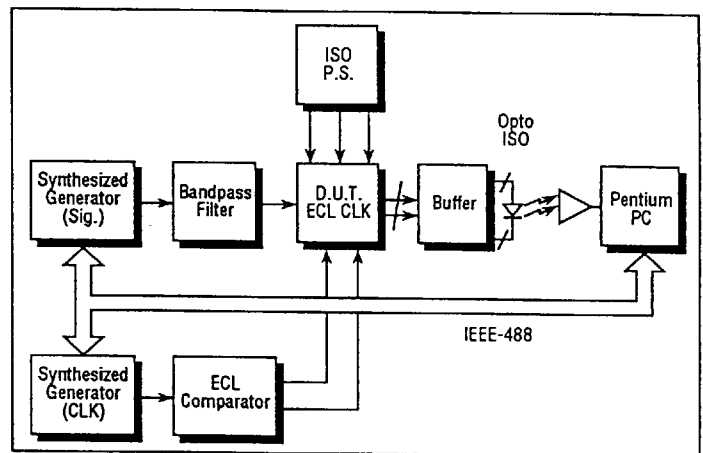

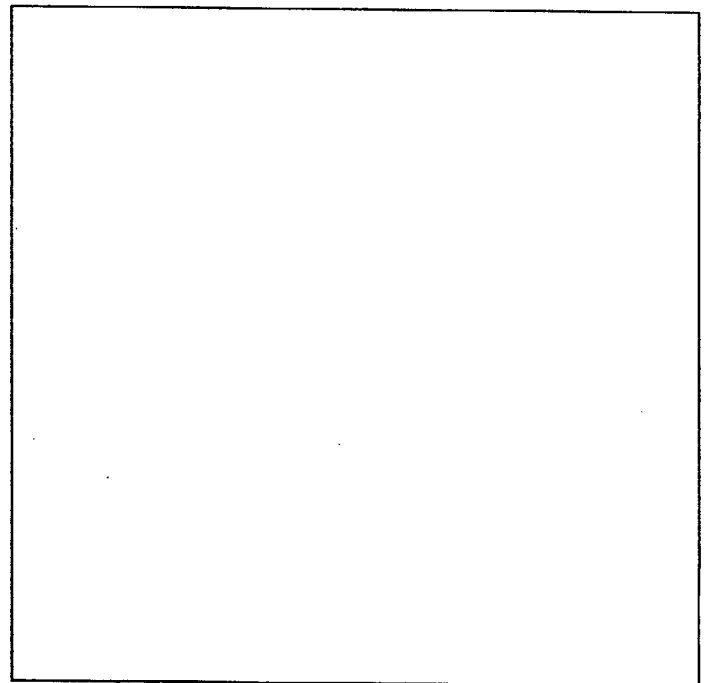**Figure 9. Frequency Domain Test System Block Diagram.**

Figure 10. Typical ADC3121 Amplitude Domain Data Sheet.

: ■ 0816970 0003137 T31 ■

Figure 11. Typical ADC3121 Frequency Domain Data Sheet.

ADC3121 EVALUATION BOARD

The ADC3121 evaluation board provides a convenient characterization method for the ADC. It is a double sided board that supplies the correct layout and contains all the capacitors and toroids required for proper power supply bypassing. Also provided is a high-speed ECL comparator circuit designed to help clean up clock edges and to pro-vide an input that is TTL/ECL compatible. (See Figure 5.) For your convenience, an optional crystal oscillator is also available. The ADC output data is latched into on-board ECL FLIP-FLOPS that drive MECL 10K-compatible differential line drivers. The data output connector is a 60-pin ribbon cable connector, 3M part number 3372-1302. Suggested interface is a twisted pair ribbon cable.

GLOSSARY OF TERMS

Spurious Free Dynamic Range

The ratio, expressed in dB, between the RMS value of the signal and the RMS value of the highest spurious spectral component below the Nyquist rate .

$$SFDR = 20 \log \frac{\text{RMS value of input signal}}{\text{RMS value max. spurious component}}$$

Signal to Noise Ratio

The ratio, expressed in dB, between the RMS value of the signal and the total RMS noise below the Nyquist rate. Note that all frequency bins that are correlated with the test frequency are removed and replaced with an average of the remaining bins.

Total Harmonic Distortion

The ratio, expressed in dB, between the RMS sum of all harmonics up to the 100th harmonic and the RMS value of the signal. The components of this specification include both Direct and Reflected Harmonics.

Direct Harmonic Distortion

The ratio, expressed in dB, between the RMS sum of all the components below the Nyquist rate that are harmonically related to the signal and the RMS value of the signal.

Reflected Harmonic Distortion

The ratio, expressed in dB, between the RMS sum of all aliased harmonics and the RMS value of the signal. Aliased harmonics are those that "fold back" below the Nyquist frequency.

Note that the estimated RMS noise, based on those frequency bins not correlated with the test signal, is first removed from the harmonic frequency bins before the above distortion values are calculated.

Ordering Guide

Simply Specify

A/D Converter   ADC3121

Evaluation Board   ADC3120-EB1

: ■ 081b970 0003138 978 ■

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