1.1 Scope.

This specification covers the detail requirements for a voltage-to-frequency converter with full scale range of up to 1MHz.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD650SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-14.

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

Supply Voltage $+V_S$ to $-V_S$	36V
Differential Input Voltage (Pins 2 & 3)	±10V
Maximum Input Voltage	$\pm V_S$
Open Collector Output Voltage Above Digital GND	+36V
Open Collector Output Current	50mA
Amplifier Short Circuit to Ground	Indefinite
Comparator Input Voltage (Pin 9)	$\pm V_S$
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 65°C/W
θ_{JA} = 150°C/W

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Table 1.

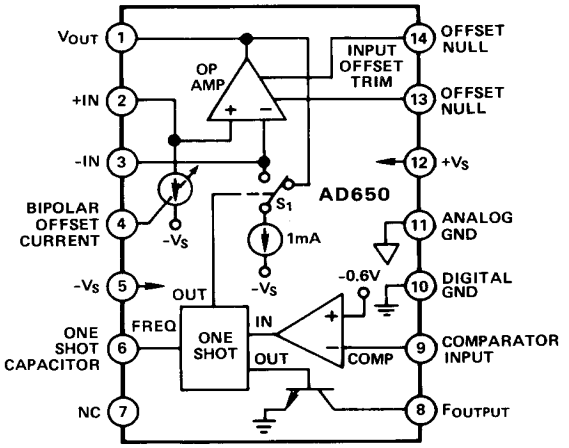
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1]	Units
Linearity Error[2]	LE	−1	0.02	0.02			V_{IN} = 10mV, 10V f = 100kHz	% of FS max
			0.1	0.1			V_{IN} = 10mV, 10V f = 1MHz	% of FS max
Gain Error[2]	A_E	−1	10	10			V_{IN} = 10V, f = 100kHz	± % of FS max
			15	15			V_{IN} = 10V, f = 1MHz	± % of FS max
Gain Error vs. Supply	P_{SS}	−1	0.015	0.015			12.5≤V_S≤17.5V f_{FS} = 100kHz	± % of FS/ % Supply max
Gain Error vs. Temperature	dA_E/dT	−1			75		V_{IN} = 10V f = 10kHz 25°C to 125°C	± ppm/°C max
					75		−55°C to 25°C	
					150		f = 100kHz 25°C to 125°C	
					150		−55°C to 25°C	
Input Offset Voltage[3]	V_{IO}	−1	4	4			V_{IN} = 20mV F = 100kHz	± mV max
Input Offset Voltage vs. Temperature	$\Delta V_{IO}/\Delta T$	−1			30		f = 10kHz 25°C to 125°C	± µV/°C max
					30		−55°C to 25°C	
Input Bias Current	$+I_{IB}$	−1	100	100			V_{IN} = 100mV	± nA max
	$-I_{IB}$	−1	20	20			V_{IN} = 100mV	± nA max
Differential Impedance	Z_{IND}	−1	2‖10					MΩ‖pF
Low Level Output Voltage	V_{OL}	−1	0.4	0.4			I_{SINK} = 8mA	V max
Leakage Current	I_{OH}	−1	100	100			V_{OUT} = 15V	nA max
Dynamic Response Settling Time (See Note 3 for Design Limits)	t_S	−1	See Note 3				Full Scale Step Input	
Overload Recovery Time (See Note 3 for Design Limits)	OR	−1	See Note 3					
Quiescent Current	$+I_S$	−1	8	8			V_S = ±15V, V_{IN} = 0V	mA max
	$-I_S$	−1	8	8			V_S = ±15V, V_{IN} = 0V	− mA min

NOTES
[1]V_S = ±15V, unless otherwise specified.
[2]Nonlinearity is defined as deviation from a straight line from zero to full scale, expressed as a fraction of full scale.
[3]1 pulse of new frequency plus 1µs.

3.2.1 Functional Block Diagram and Terminal Assignments.

Top View

D Package



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (57).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).