PCMCIA Flash Memory Card *1 MEGABYTE through 40 MEGABYTE (Intel/Sharp based)*

General Description

WEDC's FLV Series Flash memory cards offer high density linear Flash solid state storage solutions for code and data storage, high performance disk emulation and execute in place (XIP) applications in mobile PC and dedicated (embedded) equipment.

FLV series cards conform to the PCMCIA international standard

The card's control logic provides the system interface and controls the internal Flash memories. The card can be read/written in byte-wide or word-wide mode which allows for flexible integration into various systems. Combined with file management software, such as Flash Translation Layer (FTL), FLV Flash cards provide removable high-performance disk emulation.

The FLV series offers low power modes controlled by registers. Cards contain separate 2kB EEPROM memory for Card Information Structure (CIS) which can be used for easy identification of card characteristics.

The WEDC FLV series is based on Intel/Sharp Flash memories.

Note: Standard options include attribute memory.Cards without attribute memory are available. Cards are also available with or without a hardware write protect switch.

Features

- Low cost High Density Linear Flash Card
- Supports 3V or 5V only systems
- x8/ x16 Data Interface
- Based on Intel/Sharp FlashFile Components
- Fast Read Performance
  - 150ns @ 5V
  - 200ns @ 3.3V
- High Performance Random Writes
  - 8µs Typical Word Write Time @ 5V
  - 17µs Typical Word Write Time @ 3.3V
- Automated Write and Erase Algorithms
  - Command User Interface
- 100,000 Erase Cycles per Block
- 64K word symmetrical Block Architecture
- PC Card Standard Type I Form Factor

Architecture Overview

WEDC's FLV series is designed to support from 2 to 20 of 4Mb, 8Mb or 16MB components, providing a wide range of density options. Cards are based on the 28F004SC (4Mb), 28F008SC (8Mb) and 28F016SC (16Mb) devices for 3.3V or 5V only applications. Devices codes for the 28F004SC, 28F008SC and the 28F016SC are: A7H, A6H and AAH respectively. Systems should be able to recognize all three codes. Cards utilizing the 8Mb components provide densities ranging from 2MB to 20MB in 2MB increments, cards utilizing 16Mb components provide densities ranging from 4MB to 40MB in 4MB increments. 4 Mbit memory devices are used only for smallest capacity cards (1MB).

In support of the PC Card 95 standard for word wide access, devices are paired. Therefore, the Flash array is structured in 64K word (128kBytes) blocks. Write, read and block erase operations can be performed as either a word or byte wide operation . By multiplexing A0, CE1# and CE2#, 8-bit hosts can access all data on data lines DQ0 - DQ7.

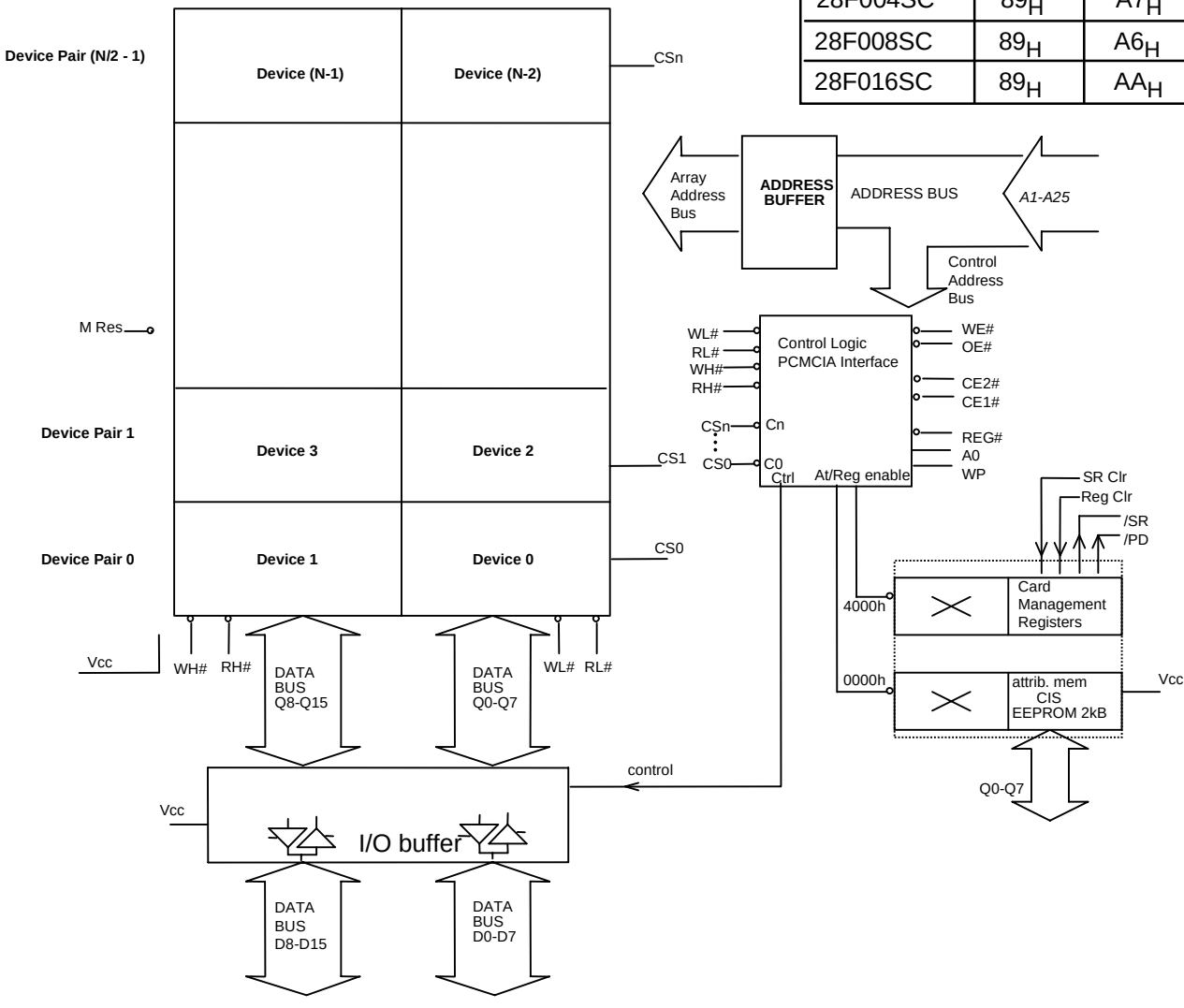
The FLA21-FLA28 series also supports the following PCMCIA compatible register functions: Soft Reset via the Configuration Option Register, Power Down (sleep mode) via the Configuration and Status Register and monitoring of Ready/Busy, Soft Reset and Power Down via the Card Status Register (cards without attribute memory do not have registers).

The FLV series cards conform to the PC Card (PCMCIA) and JEIDA standards, providing electrical and physical compatibility. The PC Card form factor offers an industry standard pinout and mechanical outline, allowing density upgrades without system design changes.

WEDC's standard cards are shipped with WEDC's Logo. Cards are also available with blank housings (no Logo). The blank housings are available in both a recessed (for label) and flat housing. Please contact your WEDC sales representative for further information on Custom artwork.

Block Diagram

Device type	Manuf ID	Device ID
28F004SC	89_H	$A7_H$
28F008SC	89_H	$A6_H$
28F016SC	89_H	AA_H



Registers in Attribute Memory Space

ADDRESS	Register NAME
4100h	Status Reg.
4002h	Config. and Status Reg.
4000h	Configuration Option Register

COR

Configuration Option Register: ADRS=4000h Write Only

SRES	LREQ	-Configuration Index-					
D7	*D6*	D5	D4	D3	D2	D1	D0

D7 Soft Reset, active High
1 = Reset State
0 = End Reset State
D6 LevelReq (not supported)
D5-D0 *Configuration index (not supported)*

CSR

Configuration Status Register: ADRS=4002h Write Only

not supported					PDwn	not supported	
D7	*D6*	*D5*	*D4*	*D3*	**D2**	*D1*	*D0*

D2 Power Down; active High
1=Place all memory devices in power down mode
0=normal operation Power On default=0

SR

Status Register: ADRS=4100h Read Only

not supported		SReset		PDwn	not supported		R/BSY
D7	*D6*	**D5**	D4	**D3**	*D2*	*D1*	**D0**

D5 Represents the state of SRESET bit in COR (4000h)
1=Reset
0=Normal operation
Power On default D5=0
D3 Represents the state of Power Down bit (D2) in CSR (4002h)
1=Power Down
D0 Reflects the card's Ready/Busy signal (pin 16) driven by memory components Ready/Busy outputs.This bit allows software polling of the card's Ready/Busy status.
1=Ready

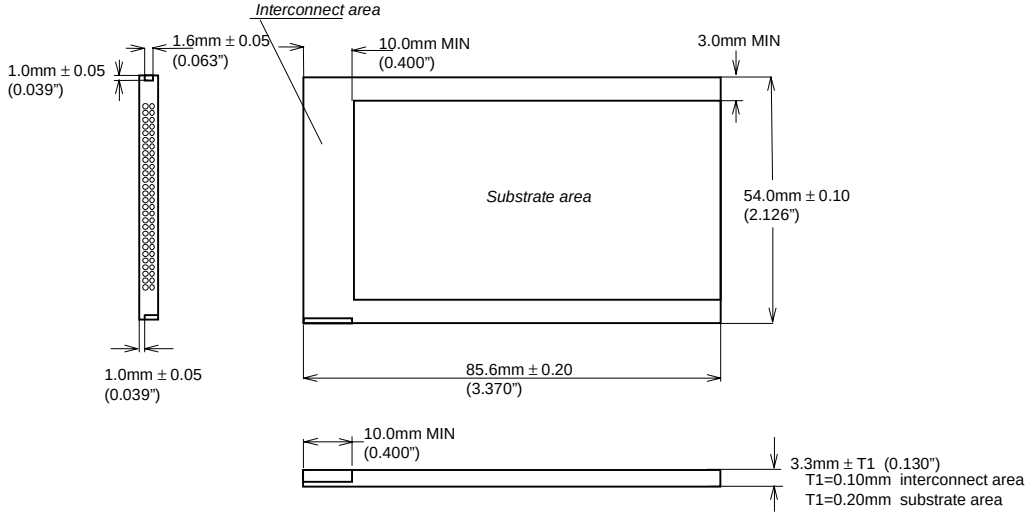
Pinout

Pin	Signal name	I/O	Function	Active
1	GND		Ground	
2	DQ3	I/O	Data bit 3	
3	DQ4	I/O	Data bit 4	
4	DQ5	I/O	Data bit 5	
5	DQ6	I/O	Data bit 6	
6	DQ7	I/O	Data bit 7	
7	CE1#	I	Card enable 1	LOW
8	A10	I	Address bit 10	
9	OE#	I	Output enable	LOW
10	A11	I	Address bit 11	
11	A9	I	Address bit 9	
12	A8	I	Address bit 8	
13	A13	I	Address bit 13	
14	A14	I	Address bit 14	
15	WE#	I	Write Enable	LOW
16	RDY/BSY#	O	Ready/Busy	LOW
17	Vcc		Supply Voltage	
18	Vpp1		Prog. Voltage	N.C.
19	A16	I	Address bit 16	
20	A15	I	Address bit 15	
21	A12	I	Address bit 12	
22	A7	I	Address bit 7	
23	A6	I	Address bit 6	
24	A5	I	Address bit 5	
25	A4	I	Address bit 4	
26	A3	I	Address bit 3	
27	A2	I	Address bit 2	
28	A1	I	Address bit 1	
29	A0	I	Address bit 0	
30	DQ0	I/O	Data bit 0	
31	DQ1	I/O	Data bit 1	
32	DQ2	I/O	Data bit 2	
33	WP	O	Write Potect	HIGH
34	GND		Ground	

Pin	Signal name	I/O	Function	Active
35	GND		Ground	
36	CD1#	O	Card Detect 1	LOW
37	DQ11	I/O	Data bit 11	
38	DQ12	I/O	Data bit 12	
39	DQ13	I/O	Data bit 13	
40	DQ14	I/O	Data bit 14	
41	DQ15	I	Data bit 15	
42	CE2#	I	Card Enable 2	LOW
43	VS1	O	Voltage Sense 1	LOW
44	RFU		Reserved	
45	RFU		Reserved	
46	A17	I	Address bit 17	
47	A18	I	Address bit 18	
48	A19	I	Address bit 19	
49	A20	I	Address bit 20	2MB(3)
50	A21	I	Address bit 21	4MB(3)
51	Vcc		Supply Voltage	
52	Vpp2		Prog. Voltage	N.C.
53	A22	I	Address bit 22	8MB(3)
54	A23	I	Address bit 23	16MB(3)
55	A24	I	Address bit 24	32MB(3)
56	A25	I	Address bit 25	64MB(3)
57	VS2	O	Voltage Sense 2	N.C.
58	RST	I	Card Reset	HIGH
59	Wait#	O	Extended Bus cycle	Low(2,)
60	RFU		Reserved	
61	REG#	I	Attrib Mem Select	
62	BVD2	O	Bat. Volt. Detect 2	(2)
63	BVD1	O	Bat. Volt. Detect 1	(2)
64	DQ8	I/O	Data bit 8	
65	DQ9	I/O	Data bit 9	
66	DQ10	O	Data bit 10	
67	CD2#	O	Card Detect 2	LOW
68	GND		Ground	

Notes:
1. RDY/BSY signal is an “Open drain” type output, pull-up resistor on host side is required.
2. Wait#, BVD1 and BVD2 are driven high for compatibility.
3. Shows density for which specified address bit is MSB. Higher order address bits are no connects (ie 4MB A21 is MSB A22 - A25 are NC).

Mechanical



Card Signal Description

Symbol	Type	Name and Function
A0 - A25	INPUT	**ADDRESS INPUTS:** A0 through A25 enable direct addressing of up to 64MB of memory on the card. Signal A0 is not used in word access mode. A25 is the most significant bit
DQ0 - DQ15	INPUT/OUTPUT	**DATA INPUT/OUTPUT:** DQ0 THROUGH DQ15 constitute the bi-directional databus. DQ15 is the MSB.
CE1#, CE2#	INPUT	**CARD ENABLE 1 AND 2:** CE1# enables even byte accesses, CE2# enables odd byte accesses. Multiplexing A0, CE1# and CE2# allows 8-bit hosts to access all data on DQ0 - DQ7.
OE#	INPUT	**OUTPUT ENABLE:** Active low signal gating read data from the memory card.
WE#	INPUT	**WRITE ENABLE:** Active low signal gating write data to the memory card.
RDY/BSY#	OUTPUT	**READY/BUSY OUTPUT:** Indicates status of internally timed erase or program algorithms. A high output indicates that the card is ready to accept accesses. A low output indicates that one or more devices in the memory card are busy with internally timed erase or write activities.
CD1#, CD2#	OUTPUT	**CARD DETECT 1 and 2:** Provide card insertion detection. These signals are internally connected to ground on the card. The host shall monitor these signals to detect card insertion (pulled-up on host side).
WP	OUTPUT	**WRITE PROTECT:** Write protect reflects the status of the Write Protect switch on the memory card. WP set to high = write protected, providing internal hardware write lockout to the Flash array. If card does not include optional write protect switch, this signal will be pulled low internally indicating write protect = "off".
VPP1, VPP2	N.C.	**PROGRAM/ERASE POWER SUPPLY:** Provides programming voltages for card . Not connected for 3.3V/5V only card.
VCC		**CARD POWER SUPPLY:** (3.3V or 5.0V nominal).
GND		**CARD GROUND**
REG#	INPUT	**ATTRIBUTE MEMORY SELECT :** Active low signal, enables access to Attribute Memory Plane, occupied by Card Information Structure and Card Registers.
RST	INPUT	**RESET:** Active high signal for placing card in Power-on default state. Reset can be used as a Power-Down signal for the memory array.
WAIT#	OUTPUT	**WAIT:** This signal is pulled high internally for compatibility. No wait states are generated.
BVD1, BVD2	OUTPUT	**BATTERY VOLTAGE DETECT:** These signals are pulled high to maintain SRAM card compatibility.
VS1, VS2	OUTPUT	**VOLTAGE SENSE:** Notifies the host socket of the card's VCC requirements. VS1 grounded and VS2 is open to indicate a 3.3V/5V card.
RFU		**RESERVED FOR FUTURE USE**
N.C.		**NO INTERNAL CONNECTION TO CARD:** pin may be driven or left floating

Functional Truth Table

READ function

Function Mode	/CE2	/CE1	A0	/OE	/WE	Common Memory /REG	Common Memory D15-D8	Common Memory D7-D0	Attribute Memory /REG	Attribute Memory D15-D8	Attribute Memory D7-D0
Standby Mode	H	H	X	X	X	X	High-Z	High-Z	X	High-Z	High-Z
Byte Access (8 bits)	H	L	L	L	H	H	High-Z	Even-Byte	L	High-Z	Even-Byte
	H	L	H	L	H	H	High-Z	Odd-Byte	L	High-Z	Not Valid
Word Access (16 bits)	L	L	X	L	H	H	Odd-Byte	Even-Byte	L	Not Valid	Even-Byte
Odd-Byte Only Access	L	H	X	L	H	H	Odd-Byte	High-Z	L	Not Valid	High-Z

WRITE function

Standby Mode	H	H	X	X	X	X	X	X	X	X	X
Byte Access (8 bits)	H	L	L	H	L	H	X	Even-Byte	L	X	Even-Byte
	H	L	H	H	L	H	X	Odd-Byte	L	X	X
Word Access (16 bits)	L	L	X	H	L	H	Odd-Byte	Even-Byte	L	X	Even-Byte
Odd-Byte Only Access	L	H	X	H	L	H	Odd-Byte	X	L	X	X

Absolute Maximum Ratings (1)

Operating Temperature TA (ambient)	
Commercial	0°C to +60 °C
Industrial	-40°C to +85 °C
Storage Temperature	
Commercial	-30°C to +80 °C
Industrial	-40°C to +85 °C
Voltage on any pin relative to VSS	-0.5V to VCC+0.5V
VCC supply Voltage relative to VSS	-0.5V to +7.0V

Note:
(1) Stress greater than those listed under "Absolute Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Characteristics (1)

Vcc = 3.3V / 5V

Symbol	Parameter	Density (Mbytes)	Notes	3.3V Vcc		5V Vcc		Units	Test Conditions
				Typ(3)	Max	Typ(3)	Max		
I_{CCR}	VCC Read Current	All		10	12	20	35	mA	VCC = VCCmax tcycle = 150ns,CMOS levels
I_{CCW}	VCC Program Current	All	28F008SC 28F016SC		60		75	mA	
I_{CCE}	VCC Erase Current	All			40		50	mA	
I_{CCS} (CMOS)	VCC Standby Current	2MB	2 28F008SC	50	200	60	230	µA	VCC = VCCmax Control Signals = VCC Reset = VSS, CMOS levels
		20MB		400		420			
		4MB	2 28F016SC	50	200	60	230		
		40MB		400		420			

CMOS Test Conditions: VCC = 5V ± 5%, VIL = VSS ± 0.2V, VIH = VCC ± 0.2V

Notes:
1. All currents are RMS values unless otherwise specified. ICCR, ICCW and ICCE are based on Byte wide operations. For 16 bit operation values are double.
2. Control Signals: CE_1#, CE_2#, OE#, WE#, REG#.
3. Typical: VCC = 5V, T = +25C.

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
I_{LI}	Input Leakage Current	1		±20	µA	VCC = VCCMAX Vin =VCC or VSS
I_{LO}	Output Leakage Current	1		±20	µA	VCC = VCCMAX Vout =VCC or VSS
V_{IL}	Input Low Voltage	1	0	0.8	V	
V_{IH}	Input High Voltage	1	0.7VCC	VCC+0.5	V	
V_{OL}	Output Low Voltage	1		0.4	V	IOL = 3.2mA
V_{OH}	Output High Voltage	1	VCC-0.4	VCC	V	IOH = -2.0mA
V_{LKO}	VCC Erase/Program Lock Voltage	1	2.0		V	

Notes:
1. Values are the same for byte and word wide modes for all card densities.
2. Exceptions: Leakage currents on CE1#, CE2#, OE#, REG# and WE# will be < 500 µA when VIN = GND due to internal pull-up resistors. Leakage currents on RST will be <150µA when VIN=VCC due to internal pull-down resistor.

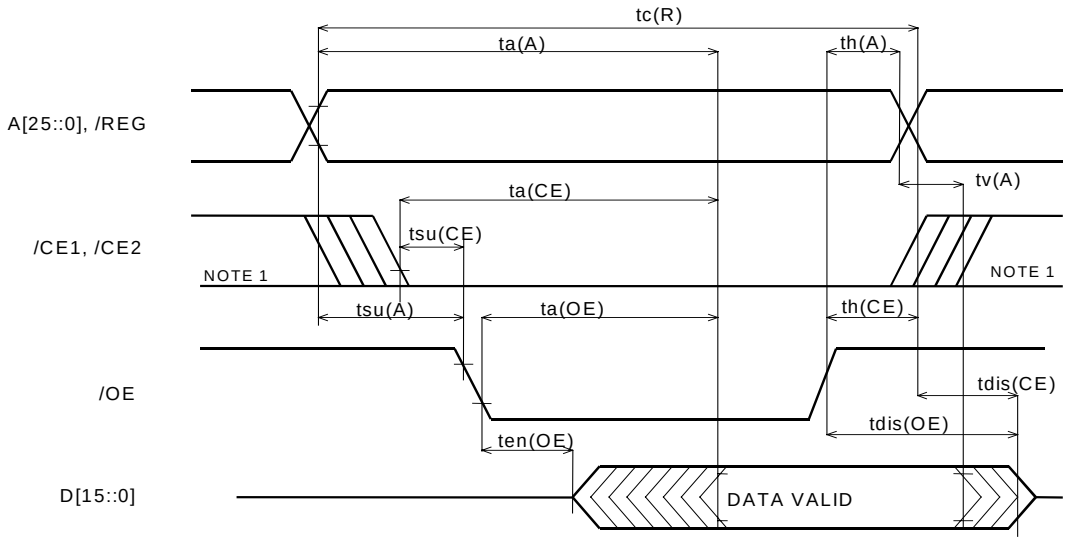
AC Characteristics

Read Timing Parameters

		150ns		250ns		
SYMBOL (PCMCIA)	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_C(R)	Read Cycle Time	150		250		ns
t_a(A)	Address Access Time		150		250	ns
t_a(CE)	Card Enable Access Time		150		250	ns
t_a(OE)	Output Enable Access Time		75		125	ns
t_{su}(A)	Address Setup Time		20		30	ns
t_{su}(CE)	Card Enable Setup Time		0		0	ns
t_h(A)	Address Hold Time		20		30	ns
t_h(CE)	Card Enable Hold Time		20		30	ns
t_v(A)	Output Hold from Address Change		0		0	ns
t_{dis}(CE)	Output Disable Time from CE#		75		100	ns
t_{dis}(OE)	Output Disable Time from OE#		75		100	ns
t_{en}(CE)	Output Enable Time from CE#	5		5		ns
t_{en}(OE)	Output Enable Time from OE#	5		5		ns
t_{rec}(RSR)	Power Down recovery to Output Delay. VCC = 5V		500		600	ns

Note: AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

Read Timing Diagram



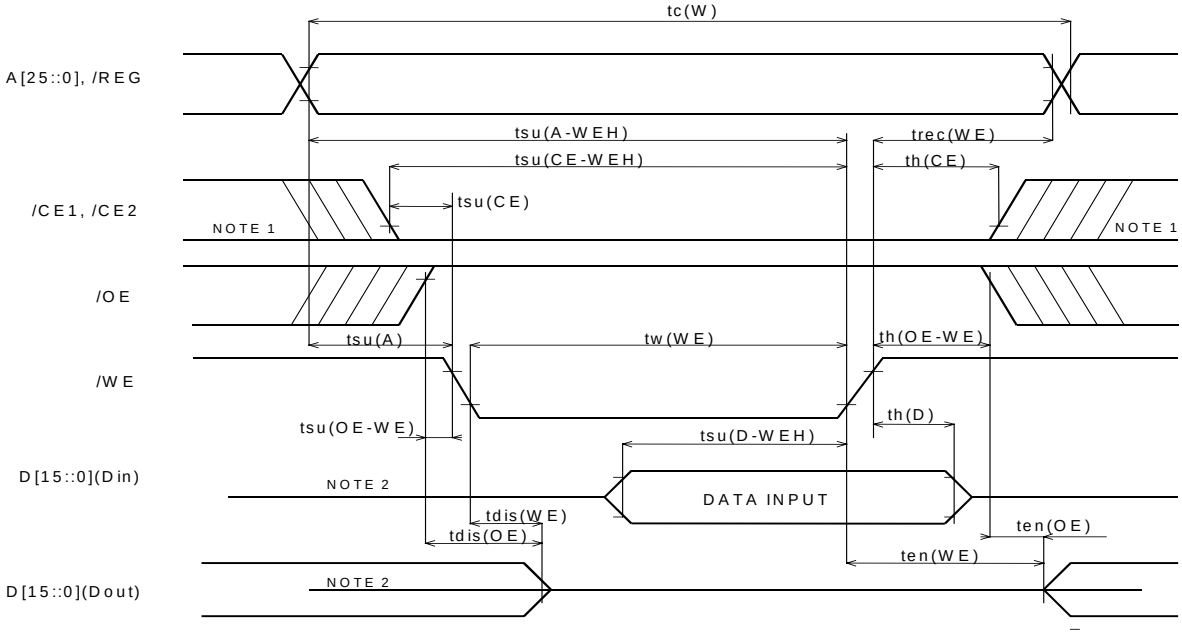
Note: Signal may be high or low in this area.

Write Timing Parameters

		150ns @ 5V		250ns @ 3.3V		
SYMBOL (PCMCIA)	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_CW	Write Cycle Time	150		250		ns
t_w(WE)	Write Pulse Width	80		150		ns
t_{su}(A)	Address Setup Time	20		30		ns
t_{su}(A-WEH)	Address Setup Time for WE#	100		180		ns
t_{su}(CE-WEH)	Card Enable Setup Time for WE#	100		180		ns
t_{su}(D-WEH)	Data Setup Time for WE#	50		80		ns
t_h(D)	Data Hold Time	20		30		ns
t_{rec}(WE)	Write Recover Time	20		30		ns
t_{dis}(WE)	Output Disable Time from WE#		75		100	ns
t_{dis}(OE)	Output Disable Time from OE#		75		100	ns
t_{en}(WE)	Output Enable Time from WE#	5		5		ns
t_{en}(OE)	Output Enable Time from OE#	5		5		ns
t_{su}(OE-WE)	Output Enable Setup from WE#	10		10		ns
t_h(OE-WE)	Output Enable Hold from WE#	10		10		ns
t_{su}(CE)	Card Enable Setup Time from OE#	0		0		ns
t_h(CE)	Card Enable Hold Time	20		20		ns

Note: AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

Write Timing Diagram



Notes:
1. Signal may be high or low in this area.
2. When the data I/O pins are in the output state, no signals shall be applied to the data pins (D15 - D0) by the host system.

Data Write and Erase Performance (1,3)

VCC = 5V ± 5%, T_A = 0C to + 70C

Symbol	Parameter	Notes	Min	Typ(1)	Max	Units
t_{WHQV1} t_{EHQV1}	Word/Byte Program time	4		8		µs
t_{WHQV2} t_{EHQV2}	Block Program Time	device SC	0.4	0.5		sec
	Block Erase Time	device SC	0.9	1.1		sec

VCC = 3.3V ± 0.3V, T_A = 0C to + 70C

Symbol	Parameter	Notes	Min	Typ(1)	Max	Units
t_{WHQV1} t_{EHQV1}	Word/Byte Program time	4		17		µs
t_{WHQV2} t_{EHQV2}	Block Program Time	device SC		1.1		sec
	Block Erase Time	device SC		1.8		sec

Notes:
1. Typical: Nominal voltages and T_A = 25C.
2. Excludes system overhead.
3. Valid for all speed options.
4. To maximize system performance RDY/BSY# signal should be polled.

PRODUCT MARKING

WED 7P016FLV2600C15 C995 9915

EDI

Date code

Lot code / trace number

Part number

Company Name

Note:
Some products are currently marked with our pre-merger company name/acronym (EDI). During our transition period, some products will also be marked with our new company name/acronym (WED). Starting October 2000 all PCMCIA products will be marked only with the WED prefix.

PART NUMBERING

7 P 016 FLV26 00 C 15

Card access time

15	150ns
25	250ns

Temperature range

C	Commercial	0°C to +70°C
I	Industrial	-40°C to +85°C

Packaging option

00	Standard, type 1

Card family and version

- See Card Family and Version Info. for details (next page)

Card capacity

016 16MB

PC card

P	Standard PCMCIA
R	Ruggedized PCMCIA

Card technology

7	FLASH
8	SRAM

Card Family and Version Information

FLV 21-FLV24 Based on **28F008SC** for 3.3V / 5V application

FLV 21	No Attribute Memory, No Write Protect switch
FLV 22	With Attribute Memory, No Write Protect switch
FLV 23	No Attribute Memory,with Write Protect switch
FLV 24	With Attribute Memory, with Write Protect switch

Example P/N **7P XXX FLV 22 SS T ZZ**

FLV 25-FLV28 Based on **28F016SC** for 3.3V / 5V application

FLV 25	No Attribute Memory, No Write Protect switch
FLV 26	With Attribute Memory, No Write Protect switch
FLV 27	No Attribute Memory,with Write Protect switch
FLV 28	With Attribute Memory, with Write Protect switch

Example P/N **7P XXX FLV 26 SS T ZZ**

Ordering Information

7P XXX FLVYY SS T ZZ

where

XXX:	**002** [1]	**2MB**
	004	**4MB**
	006 [1]	**6MB**
	008	**8MB**
	010 [1]	**10MB**
	012	**12MB**
	014 [1]	**14MB**
	016	**16MB**
	018 [1]	**18MB**
	020	**20MB**
	024 [2]	**24MB**
	028 [2]	**28MB**
	032 [2]	**32MB**
	036 [2]	**36MB**
	040 [2]	**40MB**

[1] available only for FLV21 - FLV24
[2] available only for FLV25 - FLV28

FLVYY: **Card Version (See Card Family and Version Information)**

SS:	**00**	**WEDC Silkscreen**
	01	**Blank Housing, Type I**
	02	**Blank Housing, Type I Recessed**
T:	**C**	**Commercial**
	I**	**Industrial**
ZZ:	**15**	**150ns**

Note: Options without attribute memory and with hardware write protect switch are available.
** Denotes advanced information.

CIS Information for FLV Series Cards

Example for FLV26 family, built with 28F016SC.

Address	Value	Description
00H	**01H**	**CISTPL_DEVICE**
02H	**03H**	TPL_LINK
04H	**53H**	FLASH = 150ns (device writable)
06H	**0EH**	CARD SIZE: 4MB
	1EH	8MB
	2EH	12MB
	3EH	16MB
	4EH	20MB
	5EH	24MB
	6EH	28MB
	7EH	32MB
	8EH	36MB
	9EH	40MB
08H	**FFH**	END OF DEVICE
0AH	**1CH**	**CISTPL_DEVICE_OC**
0CH	**04H**	TPL_LINK
0EH	**02H**	3 VOLT OPERATION
10H	**51H**	FLASH = 250ns (device writable)
12H	**0EH**	CARD SIZE: 4MB
	1EH	4MB
	2EH	12MB
	3EH	16MB
	4EH	20MB
	5EH	24MB
	6EH	28MB
	7EH	32MB
	8EH	36MB
	9EH	40MB
14H	**FFH**	END OF DEVICE
16H	**18H**	**CISTPL_JEDEC_C**
18H	**03H**	TPL_LINK
1AH	**89H**	INTEL - ID
1CH	**AAH**	INTEL 28F016SC – ID(4-40MB)
1EH	**FFH**	END OF DEVICE
20H	**17H**	**CISTPL_DEVICE_A**
22H	**03H**	TPL_LINK
24H	**42H**	EEPROM - 200ns
26H	**01H**	Device Size = 2KBytes
28H	**FFH**	END OF TUPLE

Address	Value	Description
2AH	**1DH**	**CISTPL_DEVICE_OA**
2CH	**03H**	TPL_LINK
2EH	**02H**	3 VOLT OPERATION
30H	**11H**	ROM - 250ns
32H	**FFH**	END OF DEVICE
34H	**1AH**	**CISTPL_CONF**
36H	**06H**	TPL_LINK
38H	**01H**	TPCC_SZ
3AH	**00H**	TPCC_LAST
3CH	**00H**	TPCC_RADR
3EH	**40H**	TPCC_RADR
40H	**03H**	TPCC_RMSK
42H	**FFH**	**CISTPL_END**
44H	**1EH**	**CISTPL_DEVICEGEO**
46H	**06H**	TPL_LINK
48H	**02H**	DGTPL_BUS
4AH	**11H**	DGTPL_EBS
4CH	**01H**	DGTPL_RBS
4EH	**01H**	DGTPL_WBS
50H	**01H**	DGTPL_PART
52H	**01H**	FLASH DEVICE NON-INTERLEAVED
54H	**20H**	**CISTPL_MANFID**
56H	**04H**	TPL_LINK(04H)
58H	**F6H**	**EDI** TPLMID_MANF: LSB
5AH	**01H**	**EDI** TPLMID_MANF: MSB
5CH	**00H**	*LSB: Number Not Assigned*
5EH	**00H**	*MSB: Number Not Assigned*
60H	**15H**	**CISTPL_VERS1**
62H	**47H**	TPL_LINK
64H	**05H**	TPLLV1_MAJOR
66H	**00H**	TPLLV1_MINOR
68H	**45H**	***E***
6AH	**44H**	***D***
6CH	**49H**	***I***
6EH	**37H**	***7***
70H	**50H**	***P***
72H	**30H**	***0***

CIS Information for FLV Series Cards (Cont.)

Address	Value	Description
74H	**34H**	***4***
76H	**30H**	***0***
78H	**46H**	***F***
7AH	**4CH**	***L***
7CH	**56H**	***V***
7EH	**32H**	***2***
80H	**36H**	***6***
82H	**2DH**	***-***
84H	**2DH**	***-***
86H	**2DH**	***-***
88H	**31H**	***1***
8AH	**35H**	***5***
8CH	**20H**	SPACE
8EH	**00H**	END TEXT
90H	**43H**	***C***
92H	**4FH**	***O***
94H	**50H**	***P***
96H	**59H**	***Y***
98H	**52H**	***R***
9AH	**49H**	***I***
9CH	**47H**	***G***
9EH	**48H**	***H***
A0H	**54H**	***T***
A2H	**20H**	SPACE
A4H	**45H**	***E***
A6H	**4CH**	***L***
A8H	**45H**	***E***
AAH	**43H**	***C***
ACH	**54H**	***T***
AEH	**52H**	***R***
B0H	**4FH**	***O***
B2H	**4EH**	***N***
B4H	**49H**	***I***
B6H	**43H**	***C***
B8H	**20H**	SPACE
BAH	**44H**	***D***
BCH	**45H**	***E***
BEH	**53H**	***S***
C0H	**49H**	***I***
C2H	**47H**	***G***
C4H	**4EH**	***N***
C6H	**53H**	***S***

Address	Value	Description
C8H	**20H**	SPACE
CAH	**49H**	***I***
CCH	**4EH**	***N***
CEH	**43H**	***C***
D0H	**4FH**	***O***
D2H	**52H**	***R***
D4H	**50H**	***P***
D6H	**4FH**	***O***
D8H	**52H**	***R***
DAH	**41H**	***A***
DCH	**54H**	***T***
DEH	**45H**	***E***
E0H	**44H**	***D***
E2H	**20H**	SPACE
E4H	**00H**	END TEXT
E6H	**31H**	***1***
E8H	**39H**	***9***
EAH	**39H**	***9***
ECH	**37H**	***7***
EEH	**00H**	END TEXT
F0H	**FFH**	END OF LIST

Revision History

revision	rev date	descrpt
00	Sep-98	initial release
01	02-Dec-98	CIS, value in line 0CH
02	7-Jun-99	Logo change
03	30-May-00	Added Page 9, Revised Page
		10, Changed Page Header
04	1-Aug-00	Corrected Timing Error pg. 6

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