PIC16F688

PIC16F688 Memory Programming Specification

This document includes the programming specifications for the following device:

- PIC16F688

1.0 PROGRAMMING THE PIC16F688

The PIC16F688 is programmed using a serial method. The Serial mode will allow the PIC16F688 to be programmed while in the user's system. This allows for increased design flexibility. This programming specification applies to the PIC16F688 device in all packages.

1.1 Hardware Requirements

The PIC16F688 requires one power supply for VDD (5.0V) and one for VPP (12V).

1.2 Program/Verify Mode

The Program/Verify mode for the PIC16F688 allows programming of user program memory, data memory, user ID locations, calibration word and the configuration word.

FIGURE 1-1: 14-PIN DIAGRAM FOR PIC16F688

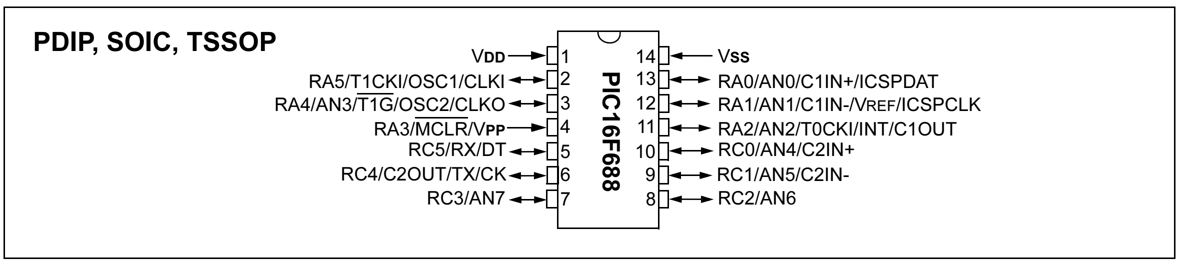


TABLE 1-1: PIN DESCRIPTIONS IN PROGRAM/VERIFY MODE: PIC16F688

Pin Name	During Programming		
	Function	**Pin Type**	**Pin Description**
RA1	ICSPCLK	I	Clock input – Schmitt Trigger input
RA0	ICSPDAT	I/O	Data input/output – Schmitt Trigger input
$\overline{MCLR}$	Program/Verify mode	P(1)	Program Mode Select
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = Input, O = Output, P = Power

Note 1: In the PIC16F688, the programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to $\overline{MCLR}$ input. Since the $\overline{MCLR}$ is used for a level source, $\overline{MCLR}$ does not draw any significant current.

2.0 MEMORY DESCRIPTION

2.1 Program Memory Map

The user memory space extends from 0x0000 to 0x1FFF. In Program/Verify mode, the program memory space extends from 0x0000 to 0x3FFF, with the first half (0x0000-0x1FFF) being user program memory and the second half (0x2000-0x3FFF) being configuration memory. The PC will increment from 0x0000 to 0x1FFF and wrap to 0x000, 0x2000 to 0x3FFF and wrap around to 0x2000 (not to 0x0000). Once in configuration memory, the highest bit of the PC stays a '1', thus always pointing to the configuration memory. The only way to point to user program memory is to reset the part and re-enter Program/Verify mode as described in **Section 3.0 "Program/Verify Mode"**.

In the configuration memory space, 0x2000-0x2008 are physically implemented. However, only locations 0x2000 through 0x2003, 0x2007 and 0x2008 are available. Other locations are reserved.

2.2 User ID Locations

A user may store identification information (user ID) in four designated locations. The user ID locations are mapped in [0x2000: 0x2003]. It is recommended that the user use only the seven Least Significant bits (LSb) of each user ID location. The user ID locations read out normally, even after code protection is enabled. It is recommended that ID locations are written as "`xx xxxx xbbb bbbb`" where '`bbb bbbb`' is user ID information.

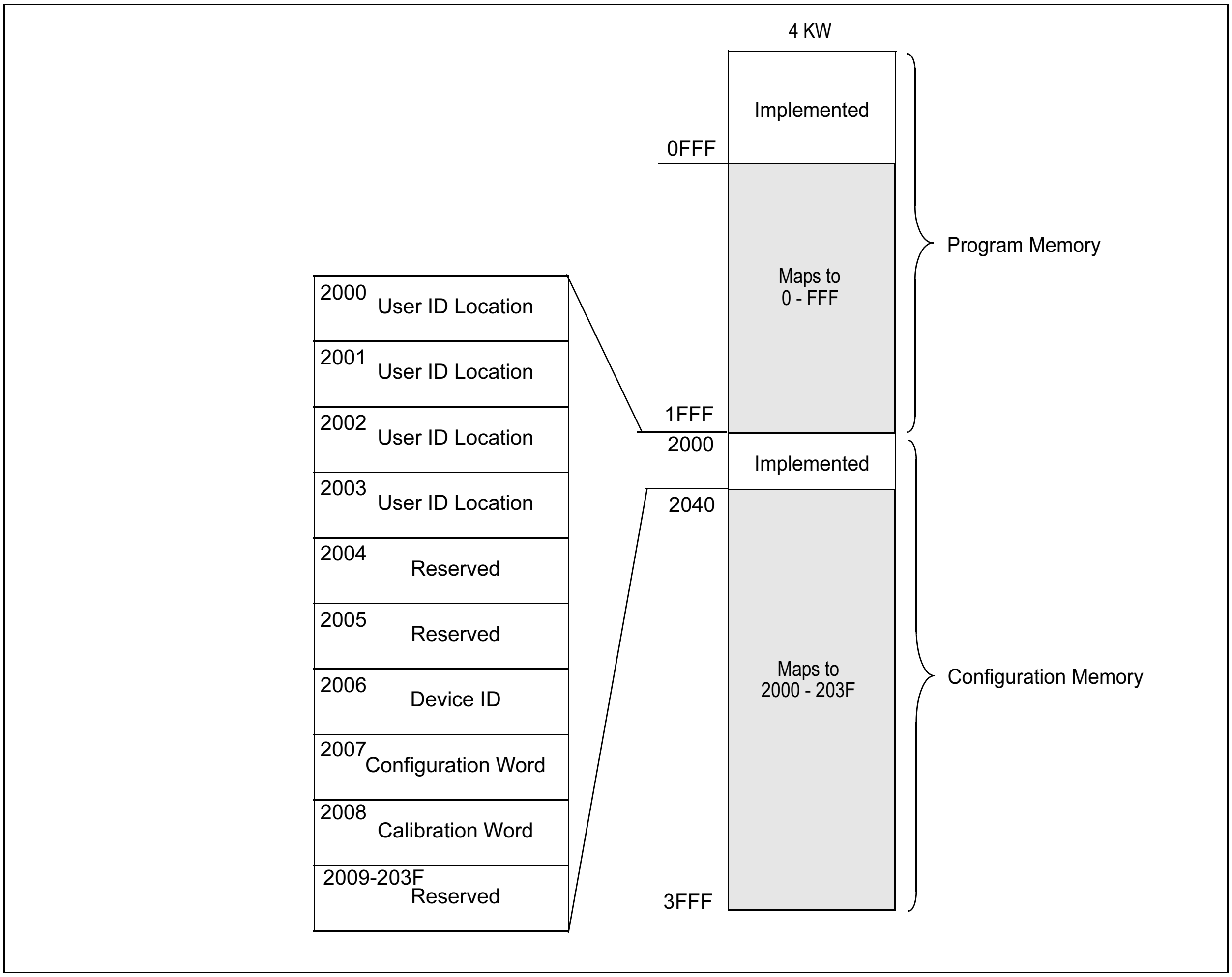
The 14 bits may be programmed, but only the 7 LSb's are displayed by MPLAB® IDE. The `xxxx`'s are "don't care" bits and are not read by MPLAB® IDE.

2.3 Calibration Word

The 8 MHz internal oscillator (INTOSC), the Power-on Reset (POR) and the Brown-out Detect (BOD) modules are factory calibrated. These values are stored in the calibration word (0x2008). See the PIC16F688 data sheet for more information.

The calibration word does not necessarily participate in erase operation unless a specific procedure is executed. Therefore, the device can be erased without affecting the calibration word. This simplifies the erase procedure, for these values do not need to be read and restored after the device is erased. See **Section 3.1.5.12 "Row Erase Program Memory"** for more information on the various erase sequences.

FIGURE 2-1: PROGRAM MEMORY MAPPING



3.0 PROGRAM/VERIFY MODE

Two methods are available to enter Program/Verify mode. The "VPP-first" is entered by holding ICSPDAT and ICSPCLK low while raising MCLR pin from VIL to VIHH (high voltage), then applying VDD and data. This method can be used for any configuration word selection and **must** be used if the INTOSC and internal MCLR options are selected (FOSC<2:0> = 100 or 101 and MCLRE = 0). The VPP-first entry prevents the device from executing code prior to entering Program/Verify mode. See the timing diagram in Figure 3-1.

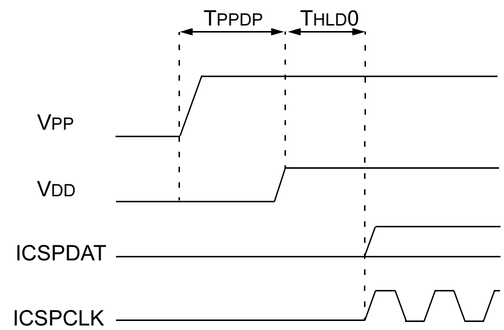
The second entry method, "VDD-first", is entered by applying VDD, holding ICSPDAT and ICSPCLK low, then raising MCLR pin from VIL to VIHH (high voltage), followed by data. This method can be used for any configuration word selection **except** when INTOSC and internal MCLR options are selected (FOSC<2:0> = 100 or 101 and MCLRE = 0). This technique is useful when programming the device when VDD is already applied, for it is not necessary to disconnect VDD to enter Program/Verify mode. See the timing diagram in Figure 3-2.

Once in this mode, the program memory, data memory, and configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are Schmitt Trigger inputs in this mode. RA4 is tristate, regardless of fuse setting.

The sequence that enters the device into the Programming/Verify mode places all other logic into the Reset state (the MCLR pin was initially at VIL). Therefore, all I/O's are in the Reset state (hi-impedance inputs) and the Program Counter (PC) is cleared.

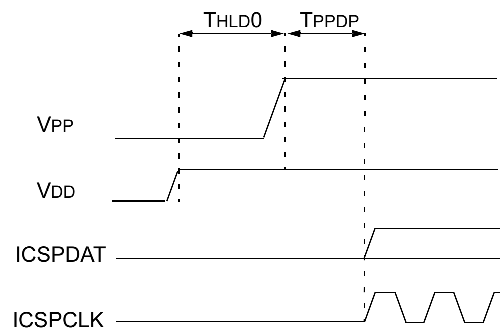
To prevent a device configured with INTOSC and internal MCLR from executing after exiting Program/Verify mode; VDD needs to power-down before VPP. See Figure 3-3 for the timing.

FIGURE 3-1: VPP-FIRST PROGRAM/VERIFY MODE ENTRY



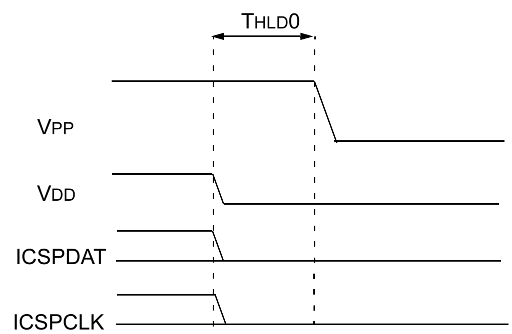
Note: This method of entry is valid, regardless of configuration word selected.

FIGURE 3-2: VDD-FIRST PROGRAM/VERIFY MODE ENTRY



Note: This method of entry is valid if INTOSC and internal MCLR are not selected.

FIGURE 3-3: PROGRAM/VERIFY MODE EXIT



3.1 Program/Erase Algorithms

The PIC16F688 program memory may be written in two ways. The fastest method writes four words at a time. However, one-word writes are also supported for backward compatibility with previous 8-pin and 14-pin FLASH devices. The four-word algorithm is used to program the program memory only. The one-word algorithm can write any available memory location (i.e., program memory, configuration memory and data memory).

After writing the array, the PC may be reset and read back to verify the write. It is not possible to verify immediately following the write because the PC can only increment, not decrement.

A device Reset will clear the PC and set the address to '0'. The Increment Address command will increment the PC. The Load Configuration command will set the PC to 0x2000. The available commands are shown in Table 3-1.

3.1.1 FOUR-WORD PROGRAMMING

Only the program memory can be written using this algorithm. Data and configuration memory (>0x2000) must use the One-word Programming Algorithm (**Section 3.1.2 "One-Word Programming"**).

This algorithm writes four sequential addresses in program memory. The four addresses must point to a four-word block with addresses modulo 4 of 0, 1, 2 and 3. For example, programming address 4 though 7 can be programmed together. Programming addresses 2 through 5 will create an unexpected result.

The sequence for programming four words of program memory at a time is as follows:

1. Load a word at the current program memory address using Load Data For Program Memory command.
2. Issue an Increment Address command.
3. Load a word at the current program memory address using Load Data For Program Memory command.
4. Repeat Step 2 and Step 3 two times.
5. Issue a Begin Programming command either internally or externally timed.
6. Wait TPROG1 (internally timed) or TPROG2 (externally timed).
7. Issue End Programming if externally timed.
8. Issue an Increment Address command.
9. Repeat this sequence as required to write program memory.

See Figure 3-17 for more information.

3.1.2 ONE-WORD PROGRAMMING

The program memory may also be written one word at a time to allow compatibility with other 8-pin and 14-pin FLASH PICmicro® devices. Configuration memory (>0x2000) and data memory must be written one word (or byte) at a time.

Note:	The four write latches must be reset after programming the Device ID (0x2006), configuration word (0x2007) or calibration word (0x2008). See **Section 3.1.3 "Resetting Write Latches"**

The sequence for programming one word of program memory at a time is as follows:

1. Load a word at the current program memory address using Load Data For Program Memory command.
2. Issue a Begin Programming command either internally or externally timed.
3. Wait TPROG1 (internally timed) or TPROG2 (externally timed).
4. Issue End Programming if externally timed.
5. Issue an Increment Address command.
6. Repeat this sequence as required to write program, data or configuration memory.

See Figure 3-16 for more information.

3.1.3 RESETTING WRITE LATCHES

The device ID (0x2006), configuration word (0x2007) and calibration word (0x2008) are mapped into the configuration memory but do not physically reside in it. As a result, the write latches are not reset when programming these locations and must be reset by the programmer. This can be done in two ways, either loading all four latches with '1's or by exiting Program/Verify mode.

The sequence for manually resetting the write latches is as follows:

1. Load a word using Load Data For Program Memory or Load Data For Configuration Memory command with a data word of all '1's.
2. Issue an Increment Address command.
3. Repeat this sequence three times to reset all four write latches.

3.1.4 ERASE ALGORITHMS

The PIC16F688 will erase different memory locations depending on the Program Counter (PC), $\overline{CP}$ and $\overline{CPD}$ values and which erase command executed. The following sequences can be used to erase noted memory locations. In each sequence, the data memory will be erased if the $\overline{CPD}$ bit in the configuration word is programmed (clear).

To erase the program memory and configuration word (0x2007), the following sequence must be performed. Note the calibration word (0x2008) and user ID (0x2000:0x2003) **will not** be erased.

1. Do a Bulk Erase Program Memory command.
2. Wait TERA to complete erase.

To erase the user ID (0x2000:0x2003), configuration word (0x2007) and program memory, use the following sequence. Note that the calibration word (0x2008) **will not** be erased.

1. Perform Load Configuration with dummy data to point the Program Counter (PC) to 0x2000
2. Perform a Bulk Erase Program Memory command.
3. Wait TERA to complete erase.

To erase the user ID (0x2000:0x2003), configuration word (0x2007), calibration word (0x2008) and program memory, use the following sequence. Note that the calibration word (0x2008) **will** be erased.

1. Perform Load Configuration with dummy data to point the Program Counter (PC) to 0x2000
2. Perform 8 Increment Address commands to point the PC to the calibration word at 0x2008.
3. Do a Bulk Erase Program Memory command.
4. Wait TERA to complete erase.

3.1.5 SERIAL PROGRAM/VERIFY OPERATION

The ICSPCLK pin is used as a clock input and the ICSPDAT pin is used for entering command bits and data input/output during serial operation. To input a command, ICSPCLK is cycled six times. Each command bit is latched on the falling edge of the clock with the LSb of the command being input first. The data input onto the ICSPDAT pin is required to have a minimum setup and hold time (see Table 6-1), with respect to the falling edge of the clock. Commands that have data associated with them (Read and Load) are specified to have a minimum delay of 1 µs between the command and the data. After this delay, the clock pin is cycled 16 times with the first cycle being a Start bit and the last cycle being a Stop bit.

During a read operation, the LSb will be transmitted onto ICSPDAT pin on the rising edge of the second cycle. For a load operation, the LSb will be latched on the falling edge of the second cycle. A minimum 1 µs delay is also specified between consecutive commands, except for the End Programming command, which requires a 100 µs TDIS.

All commands and data words are transmitted LSb first. Data is transmitted on the rising edge and latched on the falling edge of the ICSPCLK. To allow for decoding of commands and reversal of data pin configuration, a time separation of at least 1 µs is required between a command and a data word.

The commands that are available are described in Table 3-1.

TABLE 3-1: COMMAND MAPPING FOR PIC16F688

Command	Mapping (MSb … LSb)						Data
Load Configuration	x	x	0	0	0	0	0, data (14), 0
Load Data For Program Memory	x	x	0	0	1	0	0, data (14), 0
Load Data For Data Memory	x	x	0	0	1	1	0, data (8), zero (6), 0
Read Data From Program Memory	x	x	0	1	0	0	0, data (14), 0
Read Data From Data Memory	x	x	0	1	0	1	0, data (8), zero (6), 0
Increment Address	x	x	0	1	1	0	
Begin Programming	x	0	1	0	0	0	Internally Timed
Begin Programming	x	1	1	0	0	0	Externally Timed
End Programming	x	0	1	0	1	0	
Bulk Erase Program Memory	x	x	1	0	0	1	Internally Timed
Bulk Erase Data Memory	x	x	1	0	1	1	Internally Timed
Row Erase Program Memory	x	1	0	0	0	1	Internally Timed

3.1.5.1 LOAD CONFIGURATION

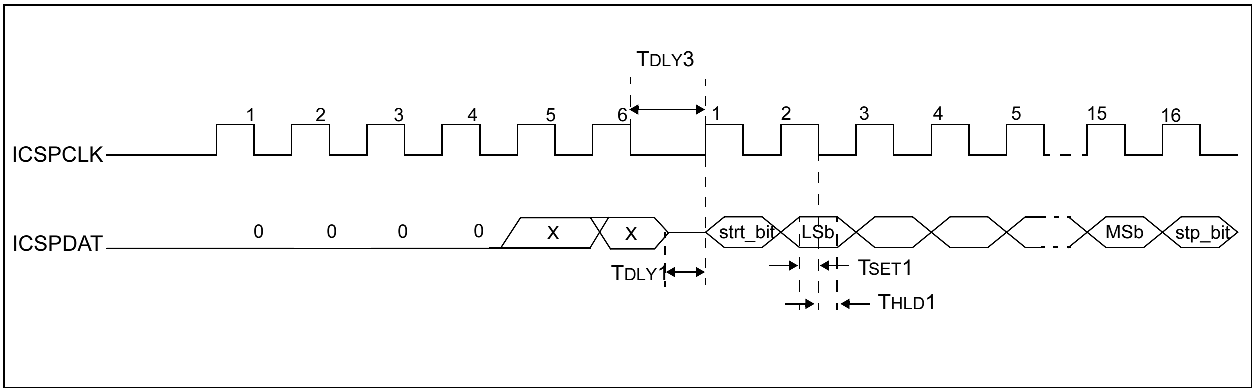
The Load Configuration command is used to access the configuration word (0x2007), user ID (0x2000:0x2003) and calibration word (0x2008). This command sets the Program Counter (PC) to address 0x2000 and loads the data latches with one word of data.

After receiving a Load Configuration command, the configuration word is accessed by performing an Increment Address command 7 times to point the PC to the configuration word. It can then be programmed with the loaded data using a Begin Programming command either internally or externally timed.

After the 6-bit command is input, ICSPCLK pin is cycled an additional 16 times for the Start bit, 14 bits of data and a Stop bit. See Figure 3-4.

After the configuration memory is entered, the only way to get back to the program memory is to exit the Program/Verify mode by taking $\overline{\text{MCLR}}$ low (V_{IL}).

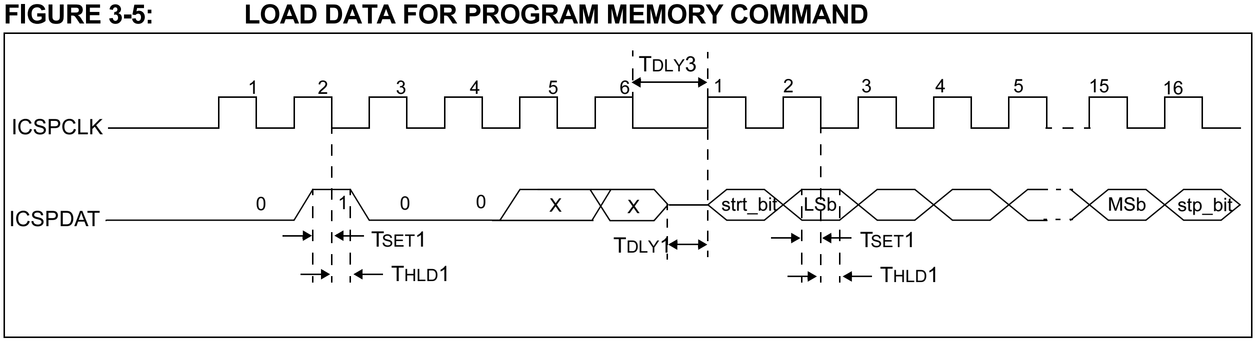
FIGURE 3-4: LOAD CONFIGURATION COMMAND



3.1.5.2 LOAD DATA FOR PROGRAM MEMORY

After receiving this command, the chip will load in a 14-bit "data word" when 16 cycles are applied, as described previously. A timing diagram for the Load Data For Program Memory command is shown in Figure 3-5.

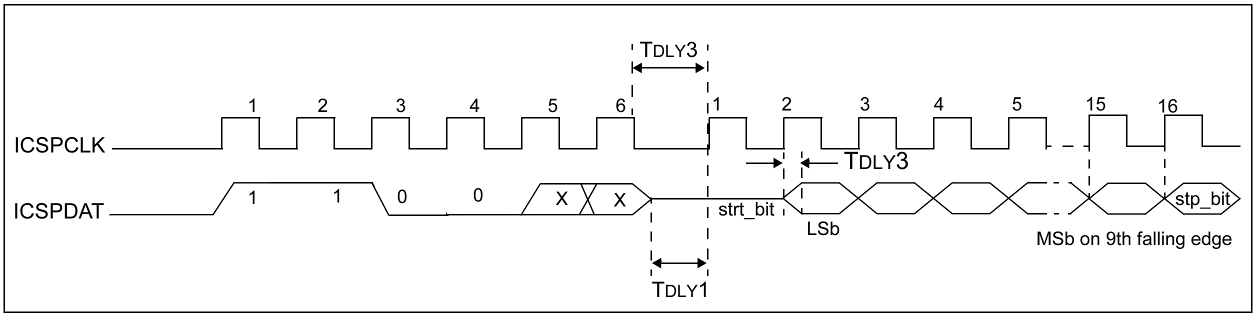
FIGURE 3-5: LOAD DATA FOR PROGRAM MEMORY COMMAND



3.1.5.3 LOAD DATA FOR DATA MEMORY

After receiving this command, the chip will load in a 14-bit "data word" when 16 cycles are applied. However, the data memory is only 8-bits wide and thus, only the first 8 bits of data after the Start bit will be programmed into the data memory. It is still necessary to cycle the clock the full 16 cycles in order to allow the internal circuitry to reset properly. The data memory contains 256 bytes.

FIGURE 3-6: LOAD DATA FOR DATA MEMORY COMMAND

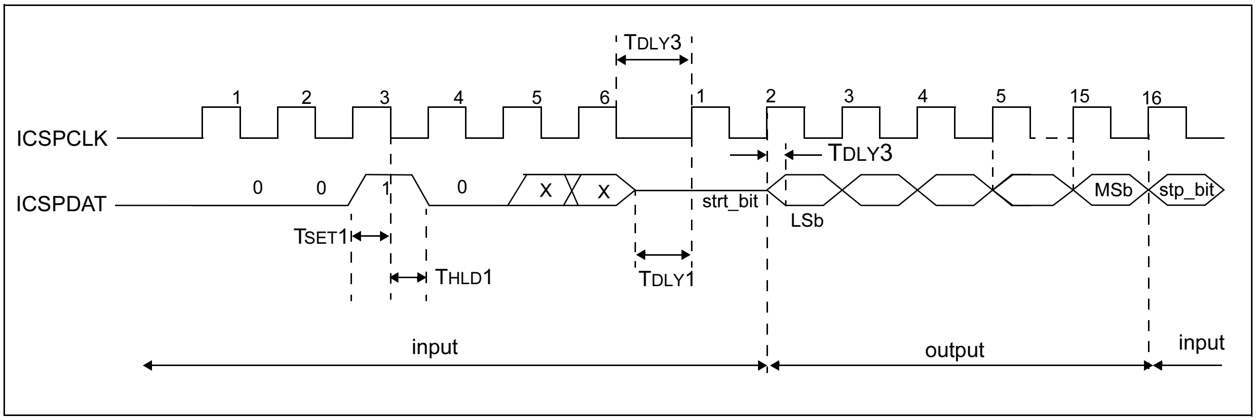


3.1.5.4 READ DATA FROM PROGRAM MEMORY

After receiving this command, the chip will transmit data bits out of the program memory (user or configuration) currently accessed, starting with the second rising edge of the clock input. The data pin will go into Output mode on the second rising clock edge, and it will revert to Input mode (hi-impedance) after the 16th rising edge.

If the program memory is code protected ($\overline{CP}$ = `0`), the data is read as zeros.

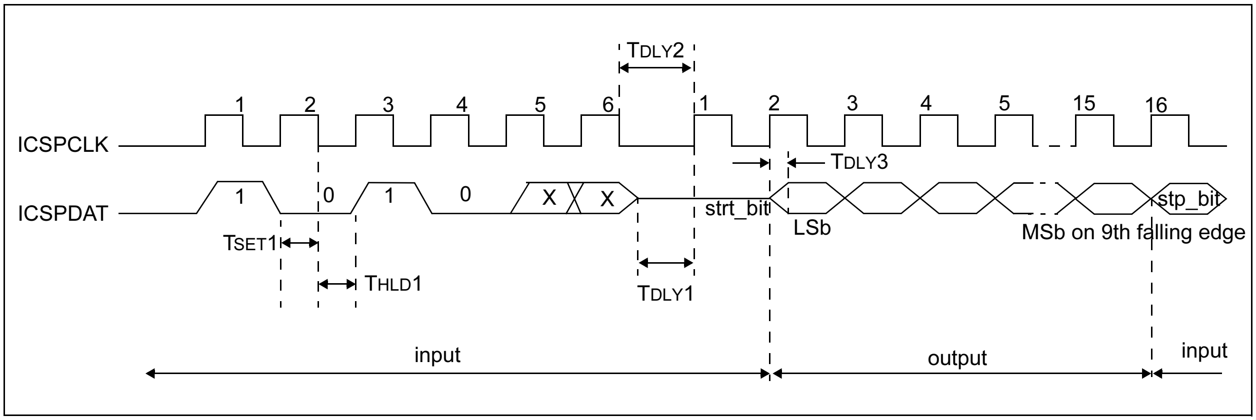
FIGURE 3-7: READ DATA FROM PROGRAM MEMORY COMMAND



3.1.5.5 READ DATA FROM PROGRAM MEMORY

After receiving this command, the chip will transmit data bits out of the data memory starting with the second rising edge of the clock input. The ICSPDAT pin will go into Output mode on the second rising edge, and it will revert to Input mode (hi-impedance) after the 16th rising edge. As previously stated, the data memory is 8-bits wide, and therefore, only the first 8 bits that are output are actual data. If the data memory is code protected, the data is read as all zeros. A timing diagram of this command is shown in Figure 3-8.

FIGURE 3-8: READ DATA FROM PROGRAM MEMORY COMMAND

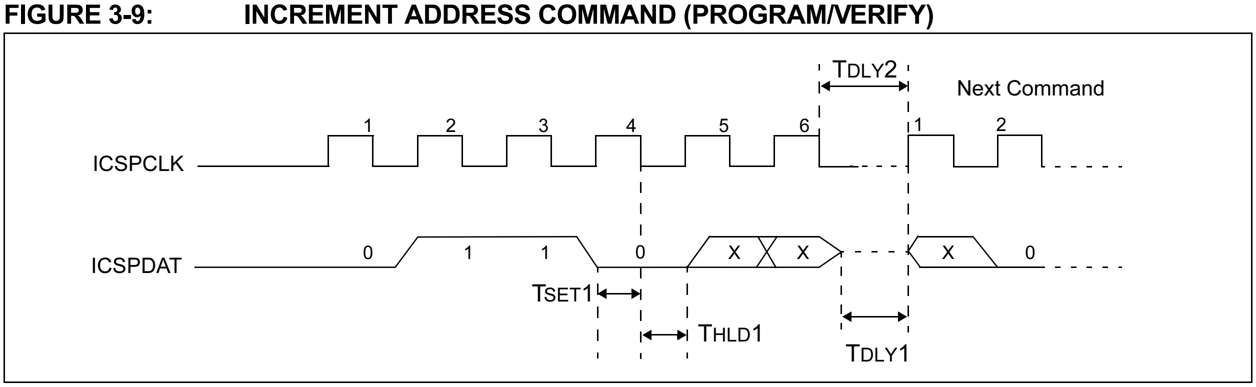


3.1.5.6 INCREMENT ADDRESS

The PC is incremented when this command is received. A timing diagram of this command is shown in Figure 3-9.

It is not possible to decrement the address counter. To reset this counter, the user should exit and re-enter Program/Verify mode.

FIGURE 3-9: INCREMENT ADDRESS COMMAND (PROGRAM/VERIFY)

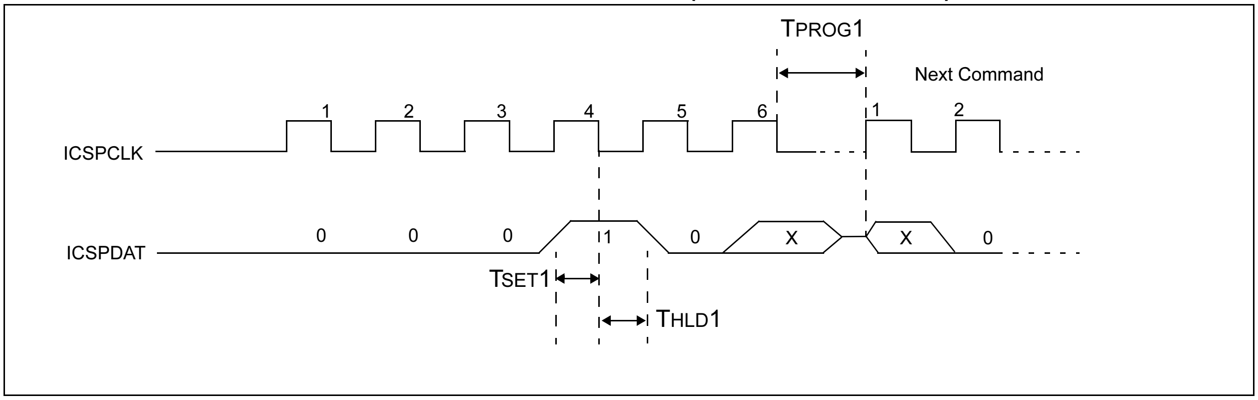


3.1.5.7 BEGIN PROGRAMMING (Internally Timed)

A load command must be given before every Begin Programming command. Programming of the appropriate memory (user program memory, configuration memory or data memory) will begin after this command is received and decoded. An internal timing mechanism executes a write. The user must allow for program cycle time for programming to complete. No End Programming command is required.

The addressed location is not erased before programming.

FIGURE 3-10: BEGIN PROGRAMMING COMMAND (INTERNALLY TIMED)

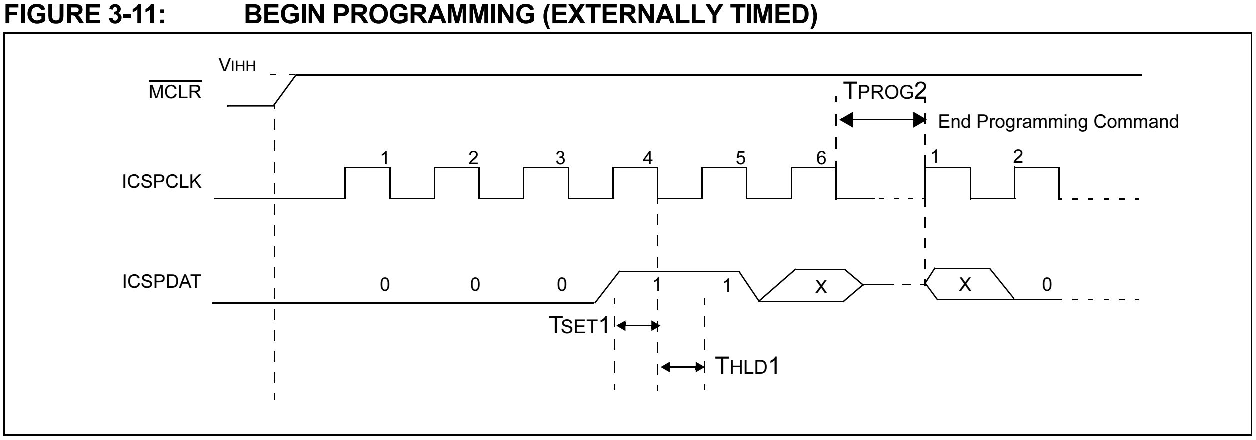


3.1.5.8 BEGIN PROGRAMMING (Externally Timed)

A load command must be given before every Begin Programming command. Programming of the appropriate memory (program memory, configuration or data memory) will begin after this command is received and decoded. Programming requires (TPROG2) time and is terminated using an End Programming command.

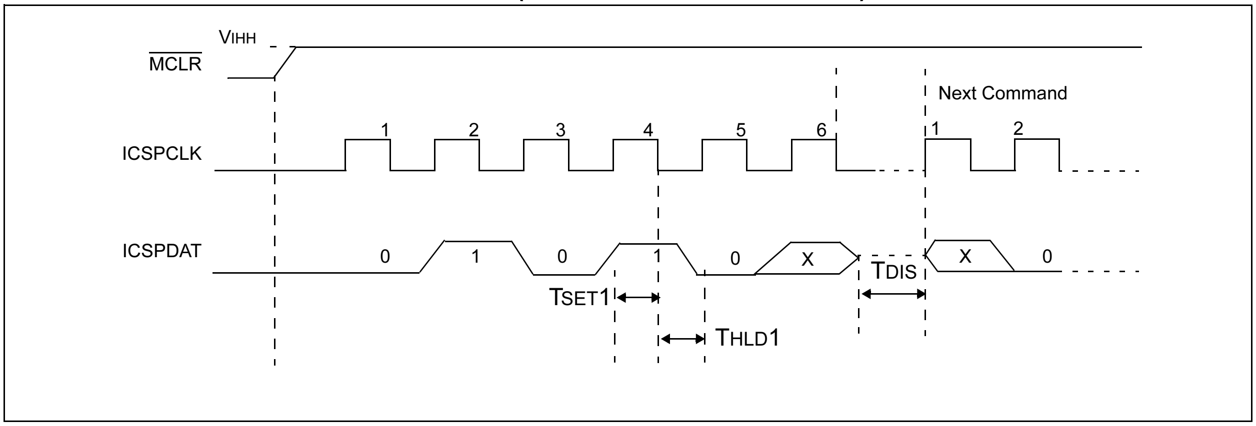
The addressed location is not erased before programming.

FIGURE 3-11: BEGIN PROGRAMMING (EXTERNALLY TIMED)



3.1.5.9 END PROGRAMMING

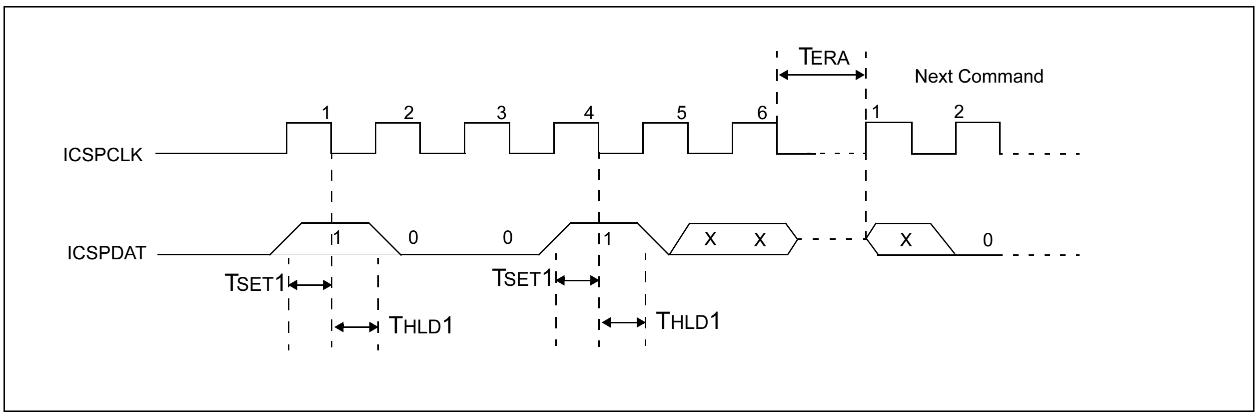
FIGURE 3-12: END PROGRAMMING (SERIAL PROGRAM/VERIFY)



3.1.5.10 BULK ERASE PROGRAM MEMORY

After this command is performed, the entire program memory and configuration word (0x2007) is erased. Data memory will also be erased if the $\overline{\text{CPD}}$ bit in the configuration word is programmed (clear). See **Section 3.1.4 "Erase Algorithms"** for erase sequences.

FIGURE 3-13: BULK ERASE PROGRAM MEMORY COMMAND



3.1.5.11 BULK ERASE DATA MEMORY

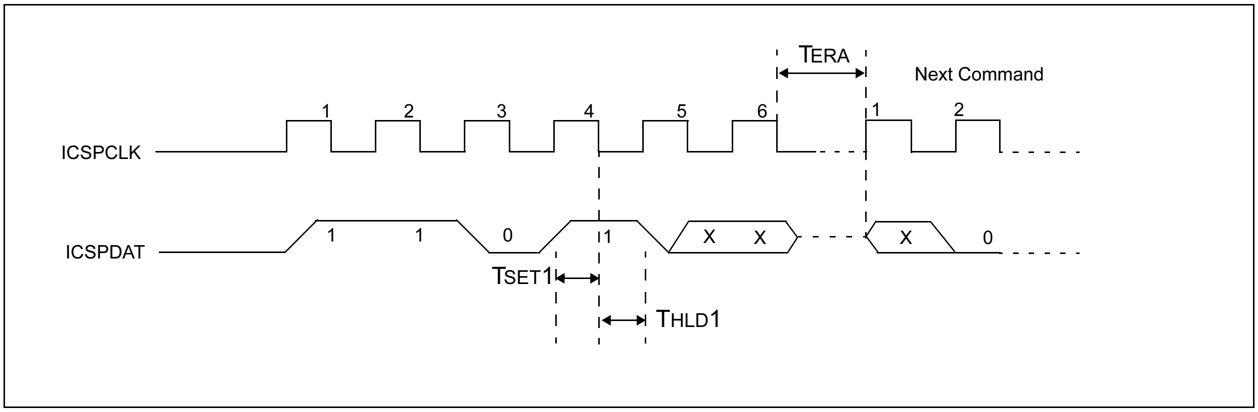
To perform an erase of the data memory, the following sequence must be performed.

1. Perform a Bulk Erase Data Memory command.
2. Wait TERA to complete bulk erase.

Data memory won't erase if code protected ($\overline{CPD}$ = 0).

Note:	All bulk erase operations must take place between 4.5V and 5.5V VDD for PIC16F688 and 2.0V to 5.5V VDD for PIC16F688-ICD.

FIGURE 3-14: BULK ERASE DATA MEMORY COMMAND



3.1.5.12 ROW ERASE PROGRAM MEMORY

This command erases the 16-word row of program memory pointed to by PC<11:4>. If the program memory array is protected ($\overline{CP}$ = 0) or the PC points to configuration memory (>0x2000), the command is ignored.

To perform a Row Erase Program Memory, the following sequence must be performed.

1. Execute a Row Erase Program Memory command.
2. Wait TERA to complete a Row Erase.

FIGURE 3-15: ROW ERASE PROGRAM MEMORY COMMAND

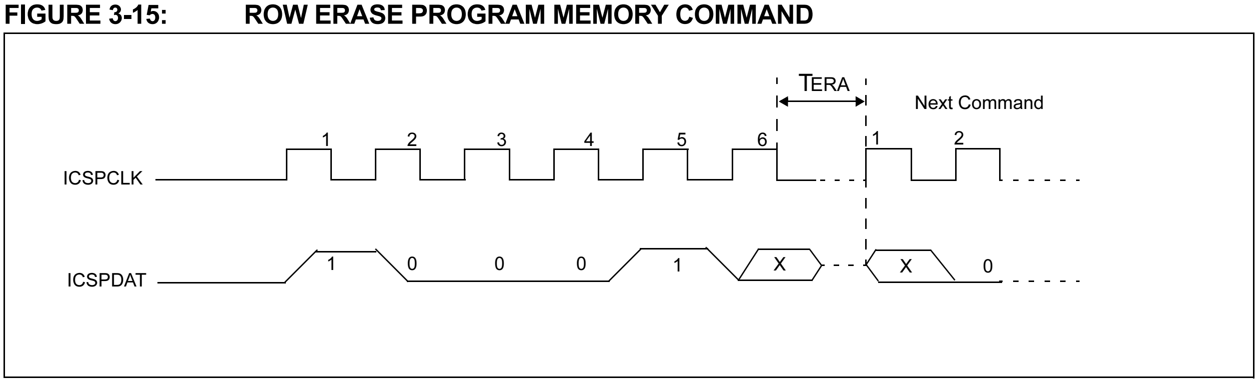
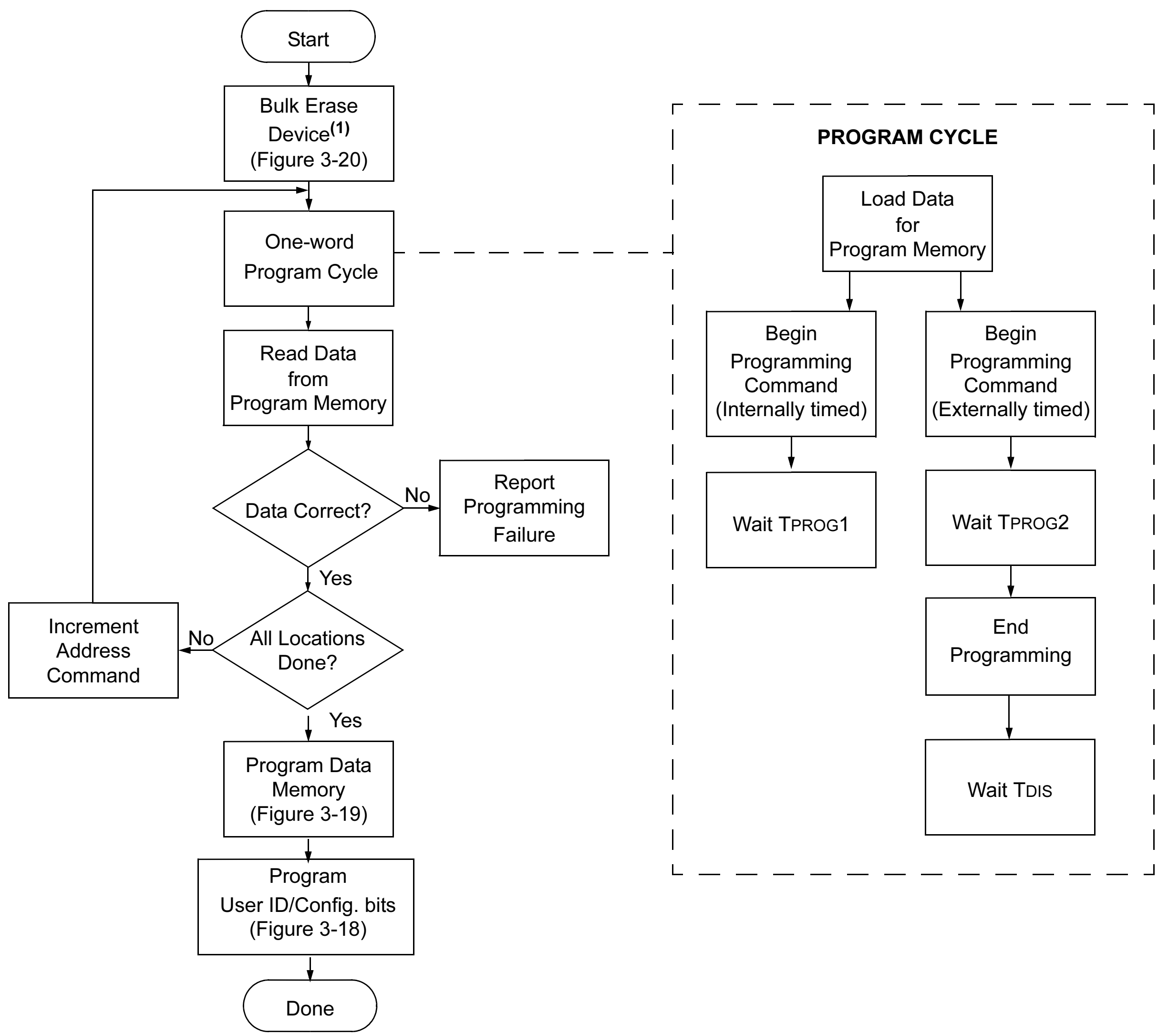
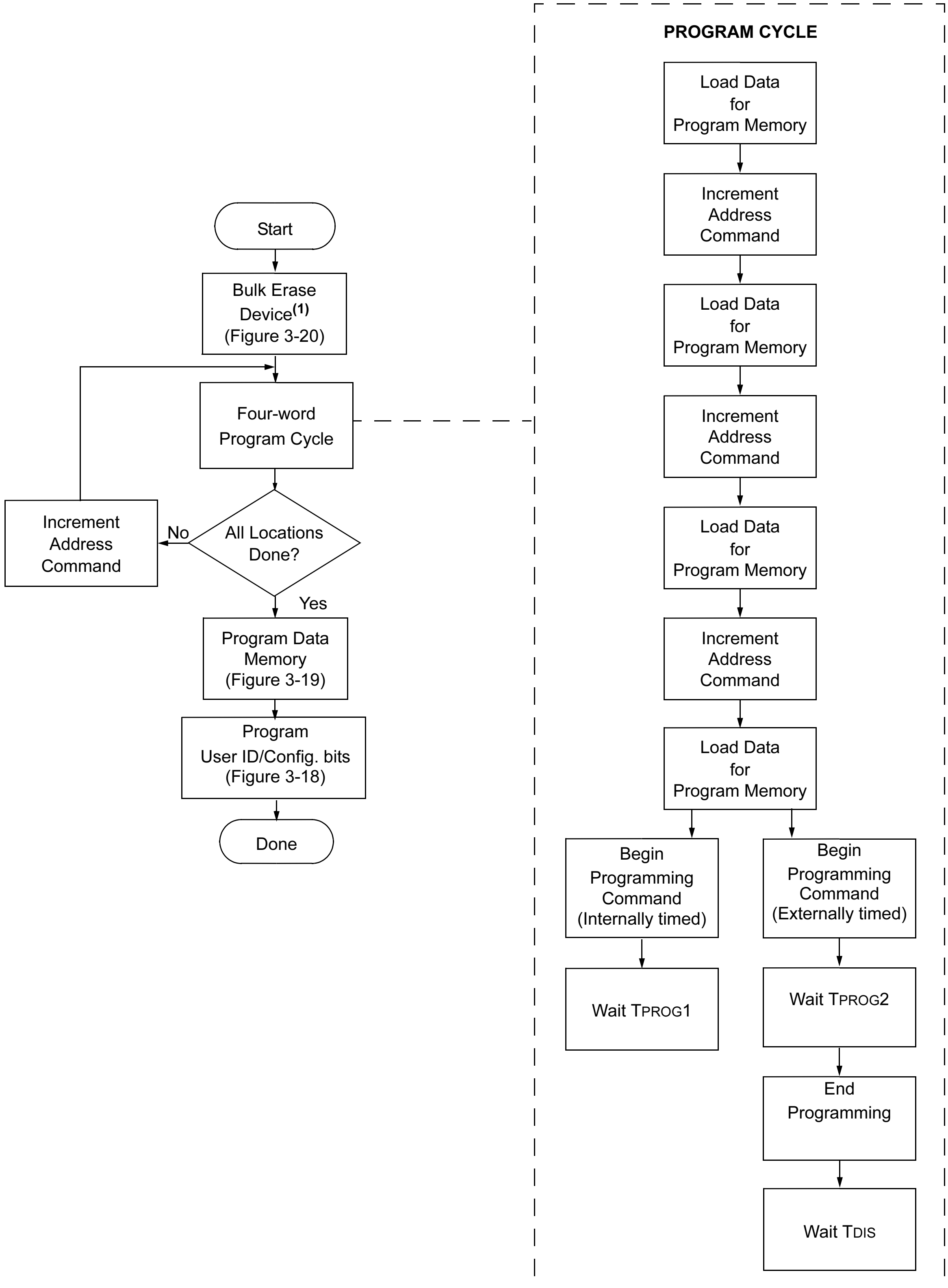


FIGURE 3-16: ONE-WORD PROGRAMMING FLOW CHART



Note 1: This step is optional if device has already been erased or has not been previously programmed.

FIGURE 3-17: FOUR-WORD PROGRAMMING FLOW CHART



Note 1: This step is optional if device is erased or not previously programmed.

2: Verification in four-word mode is accomplished after programming by reading back the entire memory.

 Preliminary

FIGURE 3-18: PROGRAM FLOW CHART - PIC16F688 CONFIGURATION MEMORY

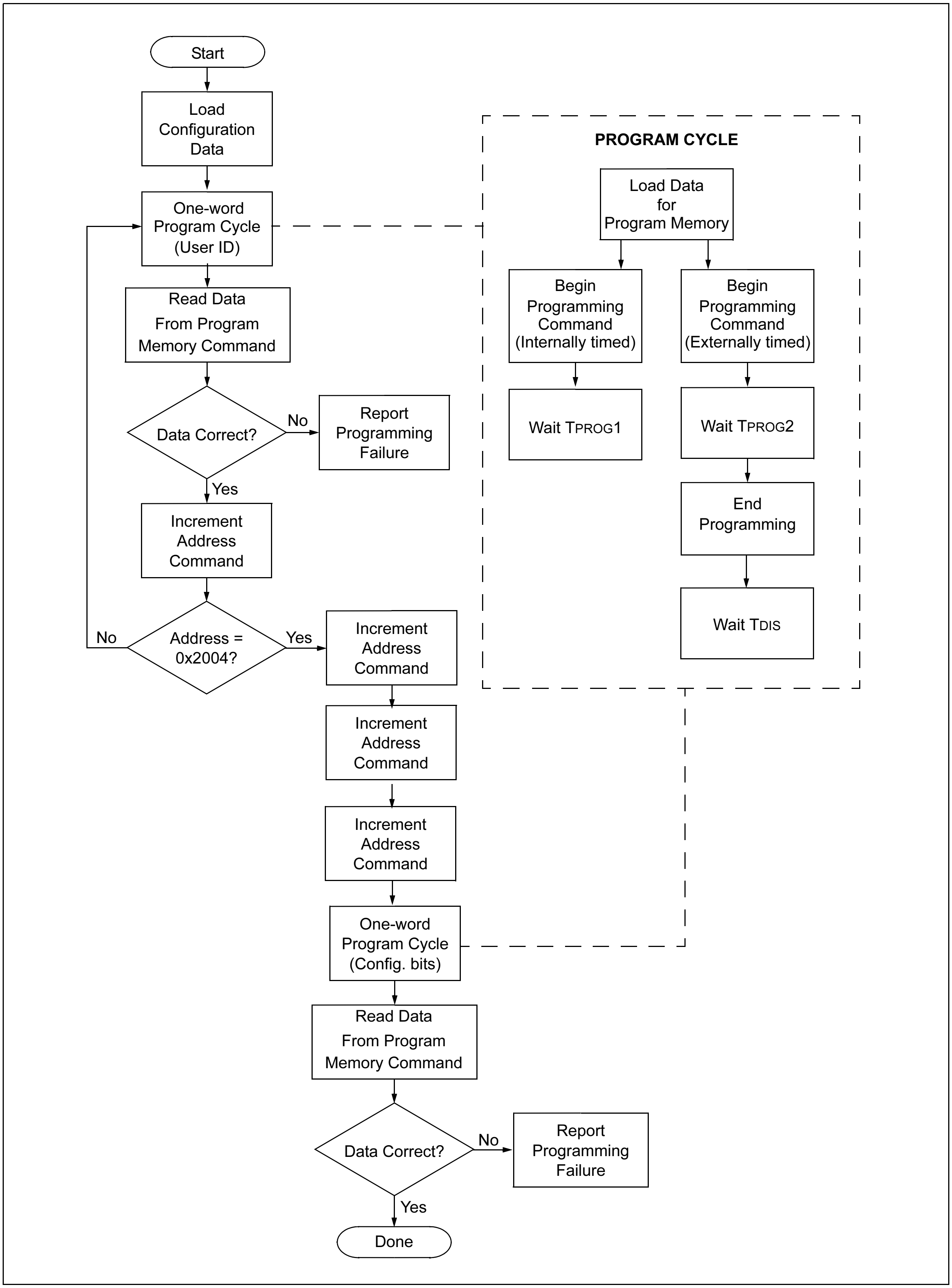


FIGURE 3-19: PROGRAM FLOW CHART - PIC16F688 DATA MEMORY

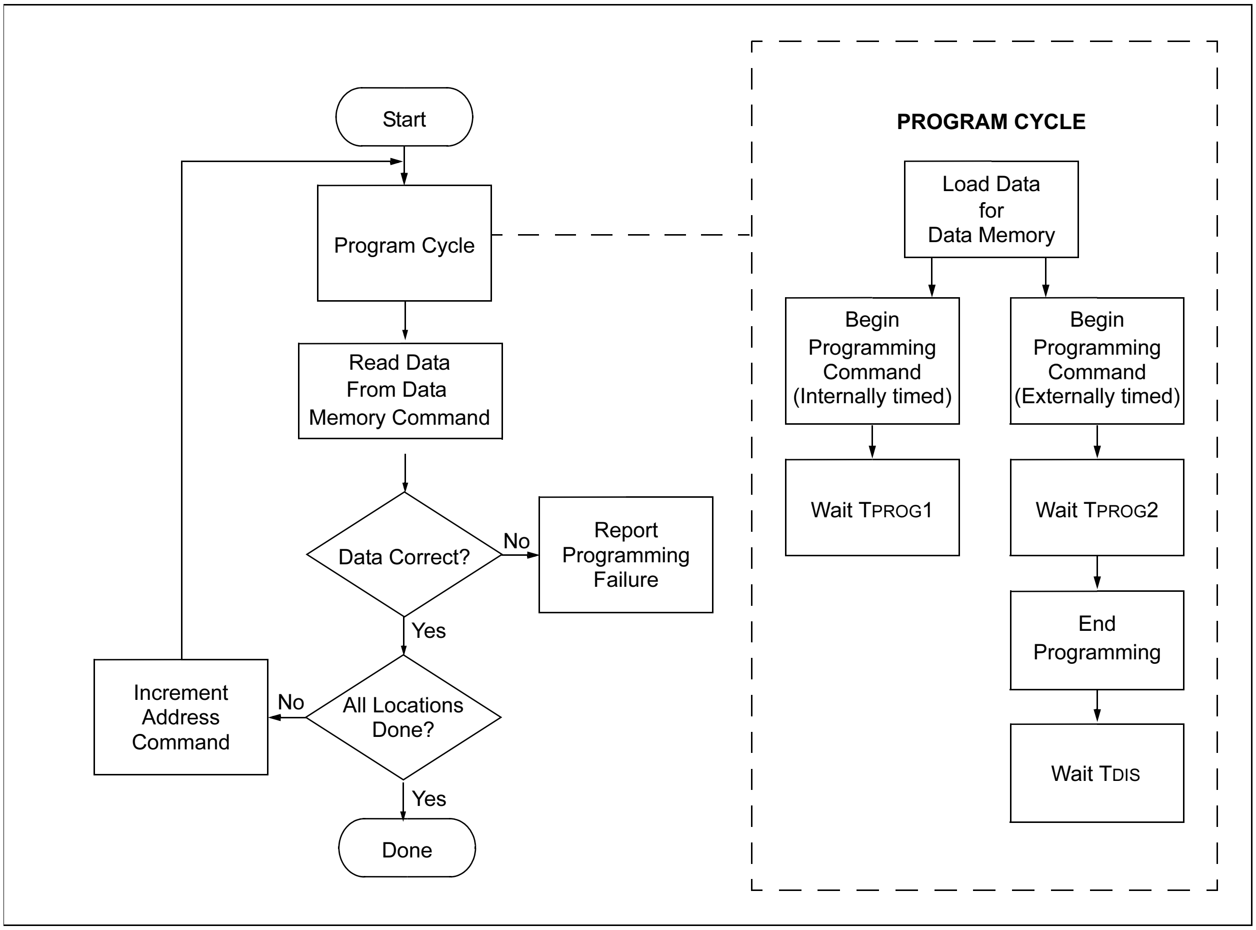
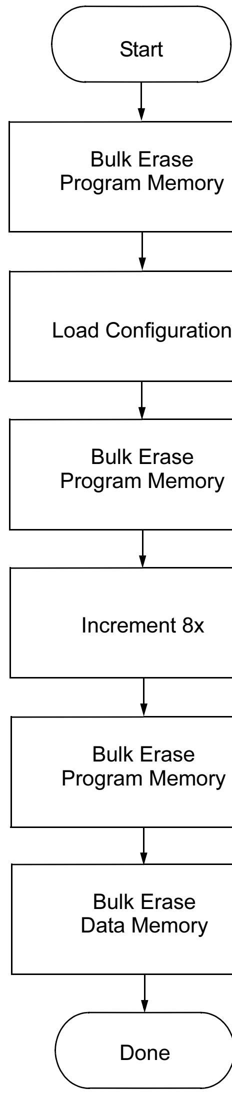


FIGURE 3-20: PROGRAM FLOW CHART - ERASE FLASH DEVICE



Note: This sequence does not erase the calibration word at address 2008h.

4.0 CONFIGURATION WORD

The PIC16F688 has several configuration bits. These bits can be programmed (reads ‘0’), or left unchanged (reads ‘1’), to select various device configurations.

REGISTER 4-1: CONFIG — CONFIGURATION WORD (ADDRESS: 2007h)

—	—	FCMEN	IESO	BODEN1	BODEN0	CPD	CP	MCLRE	$\overline{\text{PWRTE}}$	WDTE	FOSC2	F0SC1	F0SC0

bit 13 bit 0

bit 13-12 **Unimplemented**: Read as ‘1’

bit 11 **FCMEN:** Fail Clock Monitor Enabled bit
1 = Fail-Safe Clock Monitor is enabled
0 = Fail-Safe Clock Monitor is disabled

bit 10 **IESO:** Internal External Switch Over bit
1 = Internal External Switch Over mode is enabled
0 = Internal External Switch Over mode is disabled

bit 9-8 **BODEN1:BODEN0**: Brown-out Detect Selection bits(3)
11 = BOD enabled
10 = BOD enabled during operation and disabled in SLEEP
01 = BOD controlled by SBODEN bit (PCON<4>)
00 = BOD disabled

bit 7 **CPD:** Data Code Protection bit(1)
1 = Data Memory code protection is disabled
0 = Data Memory code protection is enabled

bit 6 **CP**: Code Protection bit(2)
1 = Program Memory code protection is disabled
0 = Program Memory code protection is enabled

bit 5 **MCLRE**: RA3/$\overline{\text{MCLR}}$ pin function select(4) bit
1 = RA3/$\overline{\text{MCLR}}$ pin function is $\overline{\text{MCLR}}$
0 = RA3/$\overline{\text{MCLR}}$ pin function is digital input, $\overline{\text{MCLR}}$ internally tied to V_{DD}

bit 4 **PWRTE**: Power-up Timer Enable bit
1 = PWRT disabled
0 = PWRT enabled

bit 3 **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled and can be enabled by SWDTEN bit (WDTCON<0>)

bit 2-0 **FOSC2:FOSC0**: Oscillator Selection bits
111 = RC oscillator: CLKOUT function on RA4/OSC2/CLKOUT pin, RC on RA5/OSC1/CLKIN
110 = RC oscillator: I/O function on RA4/OSC2/CLKOUT pin, RC on RA5/OSC1/CLKIN
101 = INTOSC oscillator: CLKOUT function on RA4/OSC2/CLKOUT pin, I/O function on RA5/OSC1/CLKIN
100 = INTOSC oscillator: I/O function on RA4/OSC2/CLKOUT pin, I/O function on RA5/OSC1/CLKIN
011 = EC: I/O function on RA4/OSC2/CLKOUT pin, CLKIN on RA5/OSC1/CLKIN
010 = HS oscillator: High speed crystal/resonator on RA4/OSC2/CLKOUT and RA5/OSC1/CLKIN
001 = XT oscillator: Crystal/resonator on RA4/OSC2/CLKOUT and RA5/OSC1/CLKIN
000 = LP oscillator: Low power crystal on RA4/OSC2/CLKOUT and RA5/OSC1/CLKIN

Note 1: The entire data memory will be erased when the code protection is turned off.
2: The entire program memory will be erased when the code protection is turned off.
3: Enabling Brown-out Detect does not automatically enable Power-up Timer.
4: When $\overline{\text{MCLR}}$ is asserted in INTOSC or RC mode, the internal clock oscillator is disabled.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

REGISTER 4-2: CALIB — CALIBRATION WORD (ADDRESS: 2008h)

	FCAL6	FCAL5	FCAL4	FCAL3	FCAL2	FCAL1	FCAL0		POR1	POR0	BOD2	BOD1	BOD0

bit 13 ... bit 0

bit 13 **Unimplemented**

bit 12-6 **FCAL<6:0>:** Internal oscillator calibration bits
0111111 = Maximum frequency
.
.
0000001
0000000 = Center frequency
1111111
.
.
1000000 = Minimum frequency

bit 5 **Unimplemented**

bit 4-3 **POR<1:0>:** POR Calibration bits
00= Lowest POR voltage
11= Highest POR voltage

bit 2-0 **BOD<2:0>:** BOD Calibration bits
000= Reserved
001= Lowest BOD voltage
111= Highest BOD voltage

Note 1: This location does not participate in bulk erase operations if the procedure in Figure 3-20 is used.

2: Calibration bits are reserved for factory calibration. These values can and will change across the entire range, therefore, specific values and available adjustment range can not be specified.

4.1 Device ID Word

The device ID word for the PIC16F688 is located at 2006h. This location can not be erased.

TABLE 4-1: DEVICE ID VALUES

Device	Device ID Values	
	Dev	Rev
PIC16F688	01 0001 100	x xxxx

5.0 CODE PROTECTION

For PIC16F688, once the $\overline{CP}$ bit is programmed to '0', all program memory locations read all '0's. The user ID locations and the configuration word read out in an unprotected fashion. Further programming is disabled for the entire program memory.

Data memory is protected with its own code protect bit ($\overline{CPD}$). When enabled, the data memory can still be programmed and read using the EECON1 Register (See the PIC16F688 data sheet for more information).

The user ID locations and the configuration word can be programmed regardless of the state of the $\overline{CP}$ and $\overline{CPD}$ bits.

5.1 Disabling Code Protection

It is recommended to use the procedure in Figure 3-20 to disable code protection of the device. This sequence will erase the program memory, data memory, configuration word (0x2007) and user ID locations (0x2000-0x2003). The calibration word (0x2008) **will not** be erased.

Note:	To ensure system security, if $\overline{CPD}$ bit = 0, Bulk Erase Program Memory command will also erase data memory.

5.2 Embedding Configuration Word and User ID Information in the HEX File

To allow portability of code, the programmer is required to read the configuration word and user ID locations from the hex file when loading the hex file. If configuration word information was not present in the hex file, a simple warning message may be issued. Similarly, while saving a hex file, configuration word and user ID information must be included. An option to not include this information may be provided.

Specifically for the PIC16F688, the data memory should also be embedded in the hex file (see **Section 5.3.2 "Embedding Data Memory Contents in HEX File"**).

Microchip Technology Incorporated feels strongly that this feature is important for the benefit of the end customer.

5.3 Checksum Computation

5.3.1 CHECKSUM

Checksum is calculated by reading the contents of the PIC16F688 memory locations and adding up the op codes up to the maximum user addressable location, (e.g., 0x0FFF for the PIC16F688). Any carry bits exceeding 16 bits are neglected. Finally, the configuration word (appropriately masked) is added to the checksum. Checksum computation for the PIC16F688 devices is shown in Table 5-1.

The checksum is calculated by summing the following:

- The contents of all program memory locations
- The configuration word, appropriately masked
- Masked user ID locations (when applicable)

The Least Significant 16 bits of this sum is the checksum.

The following table describes how to calculate the checksum for each device. Note that the checksum calculation differs depending on the code protect setting. Since the program memory locations read out zeroes when code protected, the table describes how to manipulate the actual program memory values to simulate values that would be read from a protected device. When calculating a checksum by reading a device, the entire program memory can simply be read and summed. The configuration word and user ID locations can always be read regardless of code protect setting.

Note:	Some older devices have an additional value added in the checksum. This is to maintain compatibility with older device programmer checksums.

TABLE 5-1: CHECKSUM COMPUTATIONS

Device	Code Protect	Checksum*	Blank Value	0x25E6 at 0 and Max Address
PIC16F688	OFF	SUM[0x0000:0x0FFF] + (CFGW & 0FFF)	0xFFFF	D3CD
	ALL	(CFGW & 0x0FFF) + SUM_ID	17BE	E38C

Legend: CFGW = Configuration Word. Example calculations assume configuration word is erased (all '1's).
SUM[a:b] = [Sum of locations a to b inclusive]
SUM_ID = User ID locations masked by 0xF then made into a 16-bit value with ID0 as the Most Significant nibble.
For example, ID0 = 0x1, ID1 = 0x2, ID3 = 0x3, ID4 = 0x4, then SUM_ID = 0x1234.
The 4 LSb's of the unprotection checksum is used for the example calculations.
*Checksum = [Sum of all the individual expressions] MODULO [0xFFFF]
+ = Addition
& = Bitwise AND

5.3.2 EMBEDDING DATA MEMORY CONTENTS IN HEX FILE

The programmer should be able to read data memory information from a hex file and conversely (as an option), write data memory contents to a hex file along with program memory information and configuration word (0x2007) and user ID (0x2000-0x2003) information.

The 256 data memory locations are logically mapped starting at address 0x2100. The format for data memory storage is one data byte per address location, LSb aligned.

6.0 PROGRAM/VERIFY MODE ELECTRICAL CHARACTERISTICS

TABLE 6-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

AC/DC Characteristics		Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +85°C Operating Voltage 4.5V ≤ VDD ≤ 5.5V				
Sym	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Conditions/Comments**
	General					
VDD	VDD level for read/write operations, program and data memory	2.0	—	5.5	V	
	VDD level for bulk erase operations, program and data memory	2.0 4.5	—	5.5 5.5	V V	PIC16F688-ICD PIC16F688
VIHH	High voltage on $\overline{\text{MCLR}}$ for Program/Verify mode entry	10	—	12	V	
TVHHR	$\overline{\text{MCLR}}$ rise time (VSS to VHH) for Program/Verify mode entry	—	—	1.0	μs	
TPPDP	Hold time after VPP changes	5	—	—	μs	
VIH1	(ICSPCLK, ICSPDAT) input high level	0.8 VDD	—	—	V	
VIL1	(ICSPCLK, ICSPDAT) input low level	0.2 VDD	—	—	V	
TSET0	ICSPCLK, ICSPDAT setup time before $\overline{\text{MCLR}}$↑ (Program/Verify mode selection pattern setup time)	100	—	—	ns	
THLD0	Hold time after VDD changes	5	—	—	μs	
	Serial Program/Verify					
TSET1	Data in setup time before clock↓	100	—	—	ns	
THLD1	Data in hold time after clock↓	100	—	—	ns	
TDLY1	Data input not driven to next clock input (delay required between command/data or command/command)	1.0	—	—	μs	
TDLY2	Delay between clock↓ to clock↑ of next command or data	1.0	—	—	μs	
TDLY3	Clock↑ to data out valid (during a Read Data command)		—	80	ns	
TERA	Erase cycle time	—	5	6	ms	
TPROG1	Programming cycle time (internally timed)	2 5	—	2.5 6	ms	Program memory Data memory
TPROG2	Programming cycle time (externally timed)	2	—	2.5	ms	10°C ≤ TA ≤ +40°C Program memory
TDIS	Time delay from program to compare (HV discharge time)	100	—	—	μs	

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