

MN3113F

Vertical Driver LSI for Video Camera CCD Area Image Sensor

■ Overview

The MN3113F is a vertical driver LSI for a two-dimensional interline CCD image sensor. It features a built-in power supply circuit that, in conjunction with such external components as six booster capacitors and two voltage stabilization capacitors, produces stabilized +15.0V and -10.0V power supplies from a +5.0V input and HD pulses.

The MN3113F makes it possible to drive a CCD image sensor on a single 5 volt power supply.

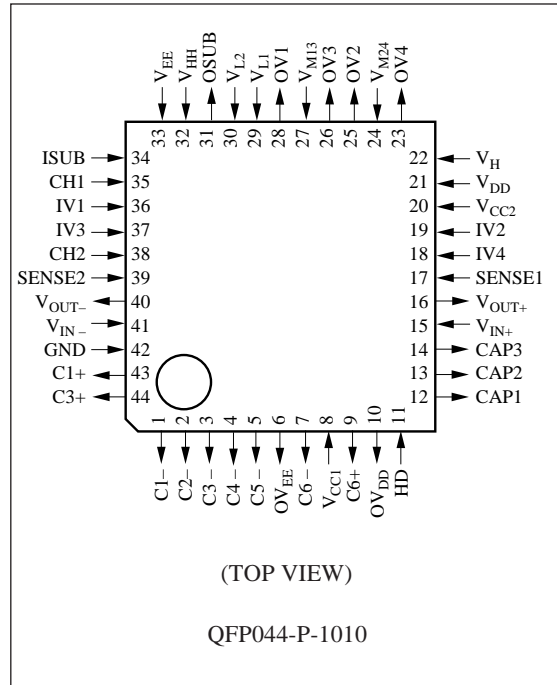
■ Features

- Single 5 volt power supply
- Adjustable output voltage for regulated voltage circuit

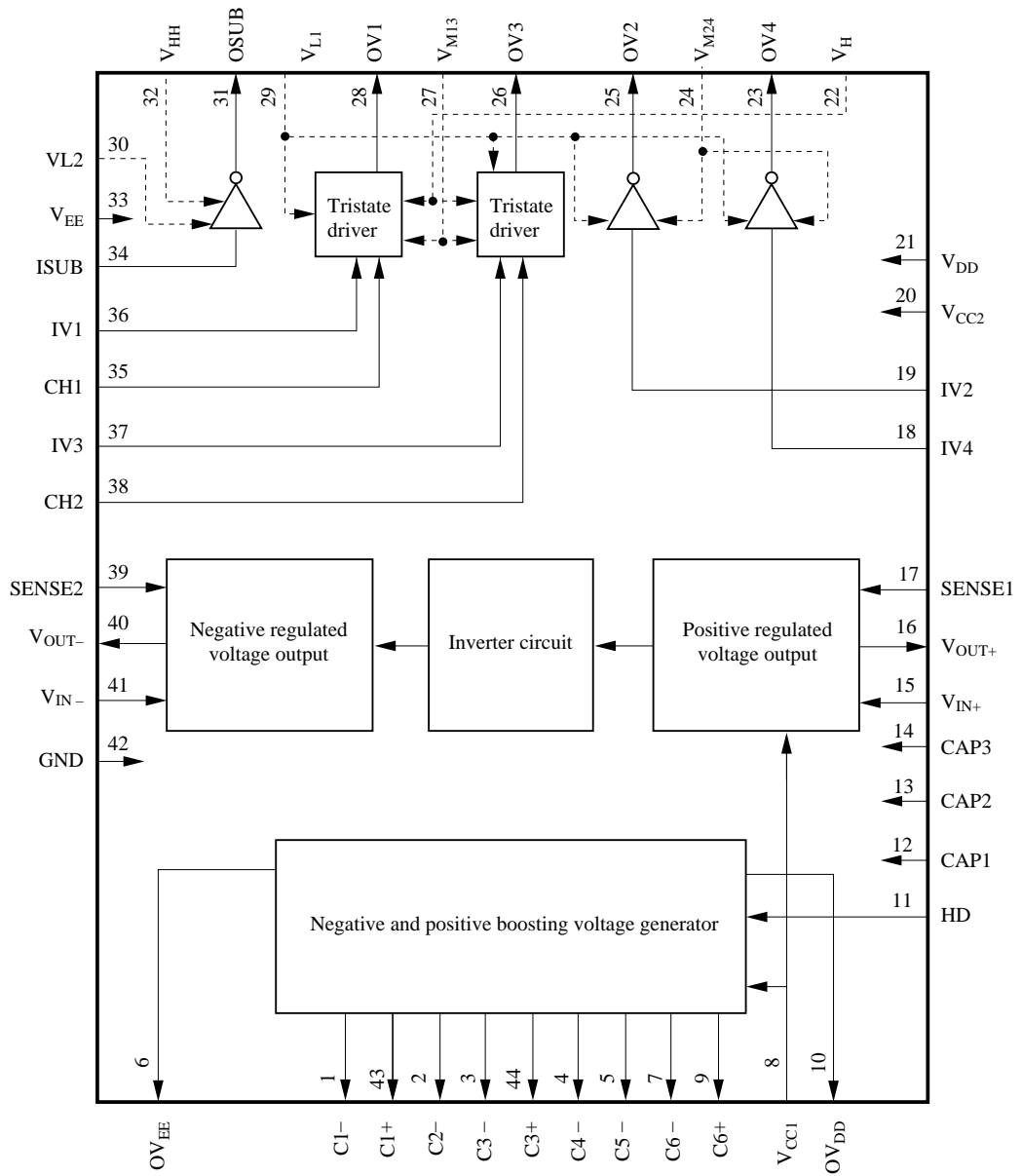
■ Applications

- Video cameras

■ Pin Assignment



■ Block Diagram



■ Pin Descriptions

| Pin No. | Symbol | Pin Name | I/O | Function Description |
|---------|------------------|----------------------------|-----|---|
| 8 | V _{CC1} | "H" level power supply | I | "H" level input for 5 volt circuits |
| 20 | V _{CC2} | for input block | | |
| 42 | GND | "L" level power supply | I | "L" level input for 5 volt circuits |
| | | for input block | | |
| 22 | V _H | "H" level power supply | I | "H" level input for high-voltage circuits |
| | | for vertical driver | | |
| 32 | V _{HH} | "H" level power supply | I | "H" level input for high-voltage circuits |
| | | for SUB driver | | |
| 27 | V _{M13} | "M" level power supply | I | "M" level input for high-voltage circuits |
| 24 | V _{M24} | for vertical driver | | |
| 29 | V _{L1} | "L" level power supply | I | "L" level input for high-voltage circuits |
| | | for vertical driver | | |
| 30 | V _{L2} | "L" level input | I | "L" level input for high-voltage circuits |
| | | for SUB driver | | |
| 21 | V _{DD} | Power supply 1 for driver | I | "H" level for high-voltage circuits |
| 33 | V _{EE} | Power supply 2 for driver | I | "L" level for high-voltage circuits |
| 15 | V _{IN+} | Positive regulated voltage | I | Positive regulated voltage block |
| | | block voltage input | | voltage input pin |
| 41 | V _{IN-} | Negative regulated voltage | I | Negative regulated voltage block |
| | | block voltage input | | voltage input pin |
| 11 | HD | HD pulse input | I | HD pulse input pin |
| 19 | IV2 | Transfer pulse input | I | Charge transfer pulse input pin |
| 18 | IV4 | Transfer pulse input | I | Charge transfer pulse input pin |
| 36 | IV1 | Transfer pulse input | I | Charge transfer pulse input pin |
| 37 | IV3 | Transfer pulse input | I | Charge transfer pulse input pin |
| 35 | CH1 | Charge pulse input | I | Charge readout pulse input pin |
| 38 | CH2 | Charge pulse input | I | Charge readout pulse input pin |
| 34 | ISUB | SUB pulse input | I | Unwanted charge rejection pulse input pin |
| 17 | SENSE1 | Positive voltage sensing | I | Positive voltage control sensing pin |
| | | input | | |
| 39 | SENSE2 | Negative voltage sensing | I | Negative voltage control sensing pin |
| | | input | | |
| 43 | C1+ | C1 connection | O | Booster block voltage charging capacitor |
| 1 | C1- | | | connection pins |
| 2 | C2+ | C2 connection | O | Booster block voltage charging capacitor |
| | C2- | | | connection pins |
| 44 | C3+ | C3 connection | O | Booster block voltage charging capacitor |
| 3 | C3- | | | connection pins |
| 4 | C4- | C4 connection | O | Booster block voltage charging capacitor |
| | | | | connection pins |
| 5 | C5- | C5 connection | O | Booster block voltage charging capacitor |
| | | | | connection pins |

■ Pin Descriptions (continued)

| Pin No. | Symbol | Pin Name | I/O | Function Description |
|---------|-------------------|---------------------------------------|-----|--|
| 7 | C6 – | C6 connection pins | O | Booster block voltage charging capacitor connection pins |
| 9 | C6+ | | | |
| 10 | OV _{DD} | Booster block positive voltage output | O | Booster block positive voltage output pin |
| 6 | OV _{EE} | Booster block negative voltage output | O | Booster block negative voltage output pin |
| 16 | V _{OUT+} | Positive regulated voltage output | O | Positive regulated voltage output pin |
| 40 | V _{OUT-} | Negative regulated voltage output | O | Negative regulated voltage output pin |
| 23 | OV4 | Binary transfer pulse output | O | Binary (V_{M24} , V_{L1}) transfer pulse output pin |
| 25 | OV2 | Binary transfer pulse output | O | Binary (V_{M24} , V_{L1}) transfer pulse output pin |
| 26 | OV3 | Tristate transfer pulse output | O | Tristate (V_H , V_{M13} , V_{L1}) transfer pulse output pin |
| 28 | OV1 | Tristate transfer pulse output | O | Tristate (V_H , V_{M13} , V_{L1}) transfer pulse output pin |
| 31 | OSUB | SUB pulse output | O | Unwanted charge (V_{HH} , V_{L2}) rejection pulse input pin |
| 12 | CAP1 | Stabilizing capacitor connection | O | Pins for connecting capacitors for internal voltage stabilization circuits |
| 13 | CAP2 | | | |
| 14 | CAP3 | | | |

■ Functional Description

Binary transfer pulses (vertical driver block)

| | |
|-----|-----|
| IV2 | OV2 |
| IV4 | OV4 |
| H | L |
| L | M |

Tristate transfer pulses (vertical driver block)

| | | |
|-----|-----|-----|
| CH1 | IV1 | OV1 |
| CH2 | IV3 | OV3 |
| H | H | L |
| | L | M |
| L | H | L |
| | L | H |

*1 IV1, IV2, IV3, IV4, CH1, CH2

H: V_{CC}

L: GND

OV1, OV2, OV3, OV4

H: V_H

M: V_{M13} , or V_{M24}

L: V_{L1}

Unwanted charge rejection pulses (SUB driver block)

| | |
|------|------|
| ISUB | OSUB |
| H | L |
| L | H |

*1 ISUB

H: V_{CC}

L: GND

OSUB

H: V_{HH}

L: V_{L2}

■ Electrical Characteristics

(1) DC characteristics

$V_{HH}=V_H=15.0V$, $V_{M13}=V_{M24}=1.0V$, $GND=0.0V$,

$V_{CC1}=V_{CC2}=5.0V (=V_{CC})$, $V_{L1}=-7.0V$, $V_{L2}=-10.0V$, $T_a=+25^\circ C$

| Parameter | Symbol | Test conditions | min | typ | max | Unit |
|---|-------------|--|----------|-------|-----------|----------|
| Quiescent supply current | I_{DDST} | $V_I=GND, V_{CC}$ | | 2 | 4 | mA |
| Operating supply current | I_{DDYN} | $V_I=GND, V_{CC}$ | | 45 | 90 | mA |
| Power supply output pins | | OV_{DD}, OV_{EE} | | | | |
| Positive voltage stabilization circuit output voltage | V_{OUT+} | $V_I=GND, V_{CC}, I_O=7mA$ $f_{INH D}=15.7kHz$ | 14.5 | 15.0 | 15.5 | V |
| Negative voltage stabilization circuit output voltage | V_{OUT-} | $V_I=GND, V_{CC}, I_O=-2mA$ $f_{INH D}=15.7kHz$ | -10.5 | -10.0 | -9.5 | V |
| Input pins | | IV1, IV2, IV3, IV4, CH1, CH2, ISUB, HD | | | | |
| "H" level voltage | V_{IH} | | 3.5 | | V_{CC} | V |
| "L" level voltage | V_{IL} | | GND | | 1.5 | V |
| Input leak current | I_{LI} | $V_I=0$ to 5V | | | ± 1 | μA |
| Output pins 1 (Binary output) | | OV2, OV4 | | | | |
| Output voltage "M" level | V_{OM1} | $V_I=GND, V_{CC}, I_{OM1}=-1mA$ | 0.9 | | V_{M24} | V |
| Output voltage "L" level | V_{OL1} | $V_I=GND, V_{CC}, I_{OL1}=1mA$ | V_{L1} | | -6.9 | V |
| Output on resistance "M" level | R_{ONM1} | $I_{OM1}=-50mA$ | | | 40 | Ω |
| Output on resistance "L" level | R_{ONL1} | $I_{OL1}=50mA$ | | | 40 | Ω |
| Output pins 2 (Tristate output) | | OV1, OV3 | | | | |
| Output voltage "H" level | V_{OH2} | $V_I=GND, V_{CC}, I_{OH2}=-1mA$ | 14.9 | | V_H | V |
| Output voltage "M" level | V_{OM2} | $V_I=GND, V_{CC}, I_{OM2}=-1mA$ | 0.9 | | V_{M13} | V |
| Output voltage "L" level | V_{OL2} | $V_I=GND, V_{CC}, I_{OL2}=1mA$ | V_{L1} | | -6.9 | V |
| Output on resistance "H" level | R_{ONH2} | $I_{OH2}=-50mA$ | | | 50 | Ω |
| Output on resistance "M" level | R_{ONM2} | $I_{OM2}=\pm 50mA$ | | | 40 | Ω |
| Output on resistance "L" level | R_{ONL2} | $I_{OL2}=50mA$ | | | 40 | Ω |
| Output pin 3 (SUB output) | | OSUB | | | | |
| Output voltage "H" level | V_{OHH3} | $V_I=GND, V_{CC}, I_{OHH3}=-1mA$ | 14.9 | | V_{HH} | V |
| Output voltage "L" level | V_{OL3} | $V_I=GND, V_{CC}, I_{OL3}=1mA$ | V_{L2} | | -9.9 | V |
| Output on resistance "H" level | R_{ONHH3} | $I_{ONHH3}=-50mA$ | | | 50 | Ω |
| Output on resistance "L" level | R_{ONL3} | $I_{ONL3}=50mA$ | | | 40 | Ω |

(2) AC characteristics

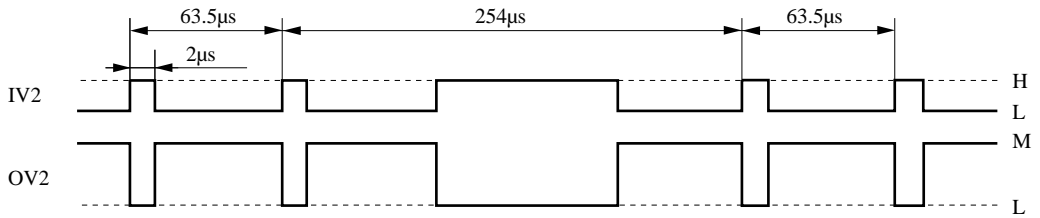
 $V_{HH}=V_H=15.0V$, $V_{M13}=V_{M24}=1.0V$, $GND=0.0V$,

 $V_{CC1}=V_{CC2}=5.0V (=V_{CC})$, $V_{L1}=-7.0V$, $V_{L2}=-10.0V$, $T_a=+25^{\circ}C$

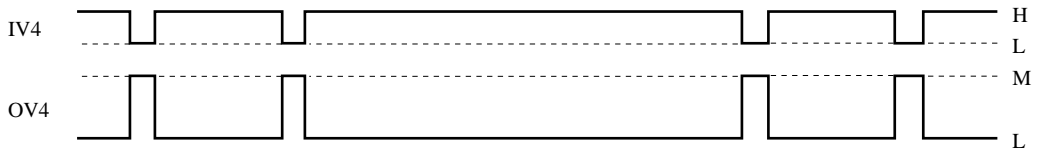
| Parameter | Symbol | Test Conditions | min | typ | max | Unit |
|--|------------|-----------------------------|-----|-----|-----|------|
| Output pins 1 (Binary output) OV2 , OV4 | | | | | | |
| Transmission delay time | t_{PLM} | No load | | 100 | 200 | ns |
| | t_{PML} | From "L" level to "M" level | | | | |
| Rise time | t_{TLM} | | | 200 | 300 | ns |
| Fall time | t_{TML} | | | | | |
| Output pins 2 (Tristate output) OV1 , OV3 | | | | | | |
| Transmission delay time | t_{PLM} | No load | | 100 | 200 | ns |
| | t_{PML} | From "L" level to "M" level | | | | |
| Transmission delay time | t_{PMH} | No load | | 200 | 400 | ns |
| | t_{PHM} | From "M" level to "H" level | | | | |
| Rise time | t_{TLM} | | | 200 | 300 | ns |
| Fall time | t_{TML} | | | | | |
| Rise time | t_{TMH} | | | 200 | 300 | ns |
| Fall time | t_{THM} | | | | | |
| Output pin 3 (SUB output) OSUB | | | | | | |
| Transmission delay time | t_{PLHH} | No load | | 100 | 200 | ns |
| | t_{PHHL} | From "L" level to "H" level | | | | |
| Rise time | t_{TLHH} | | | 200 | 300 | ns |
| Fall time | t_{THHL} | | | | | |

■ Timing Chart

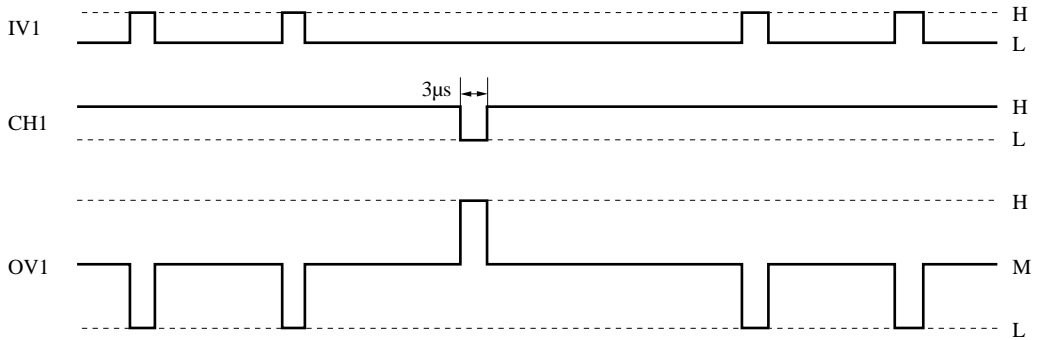
1. Binary transfer pulses



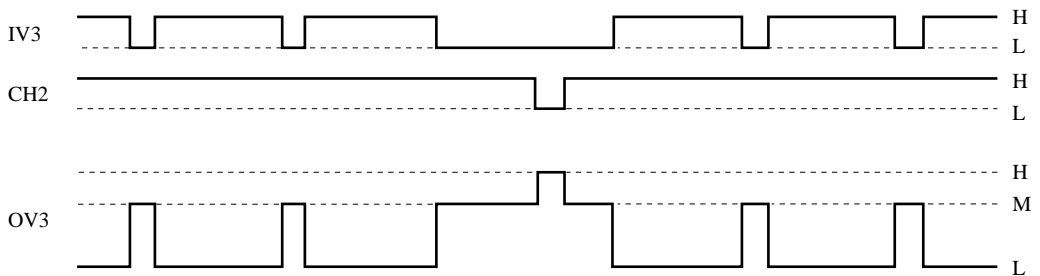
2. Binary transfer pulses



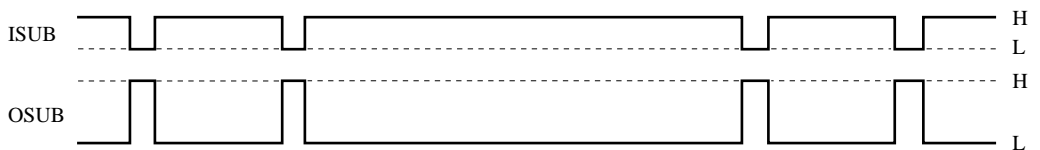
3. Tristate transfer pulses



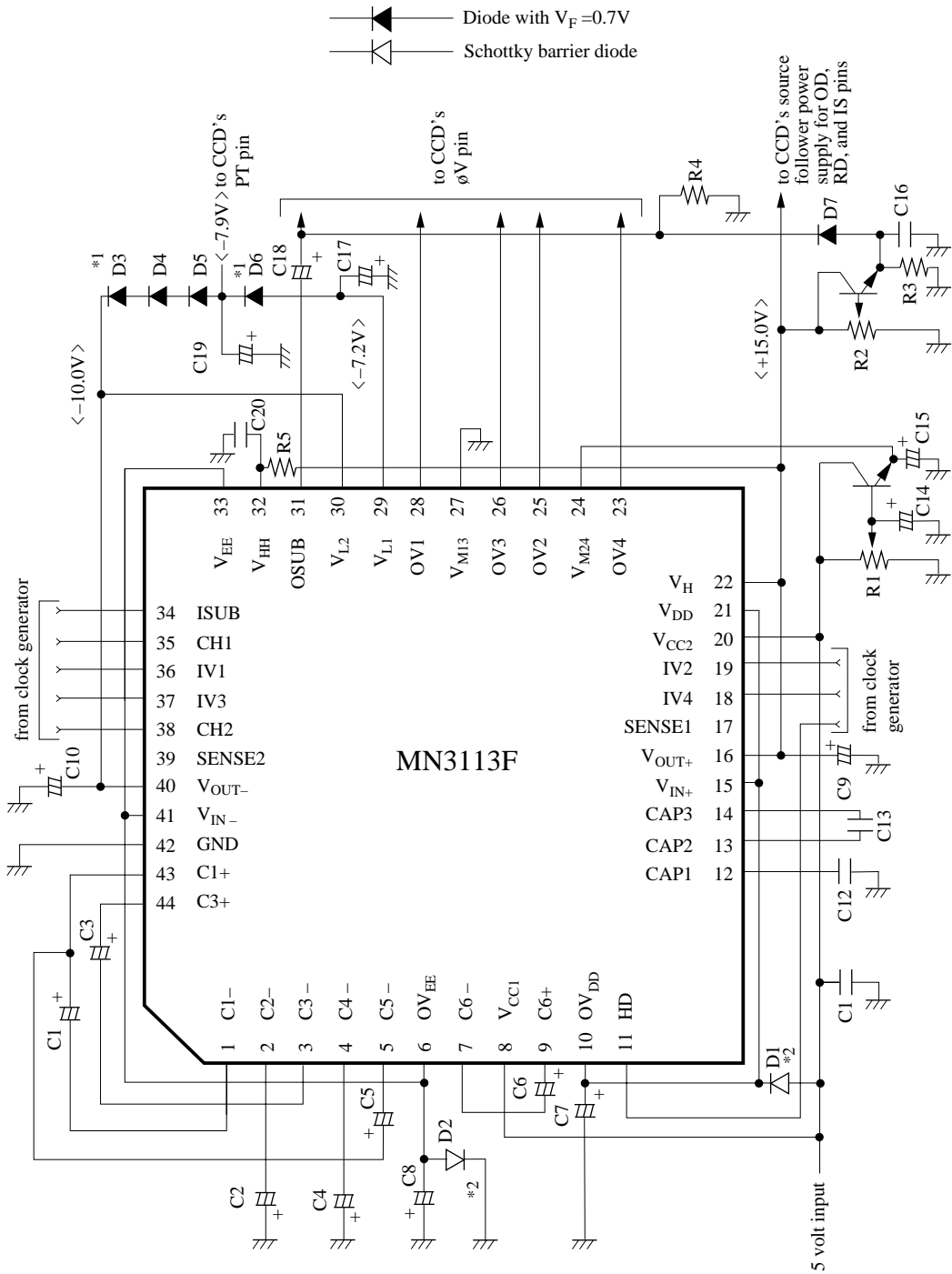
4. Tristate transfer pulses



5. SUB pulses



■ Application Circuit Example

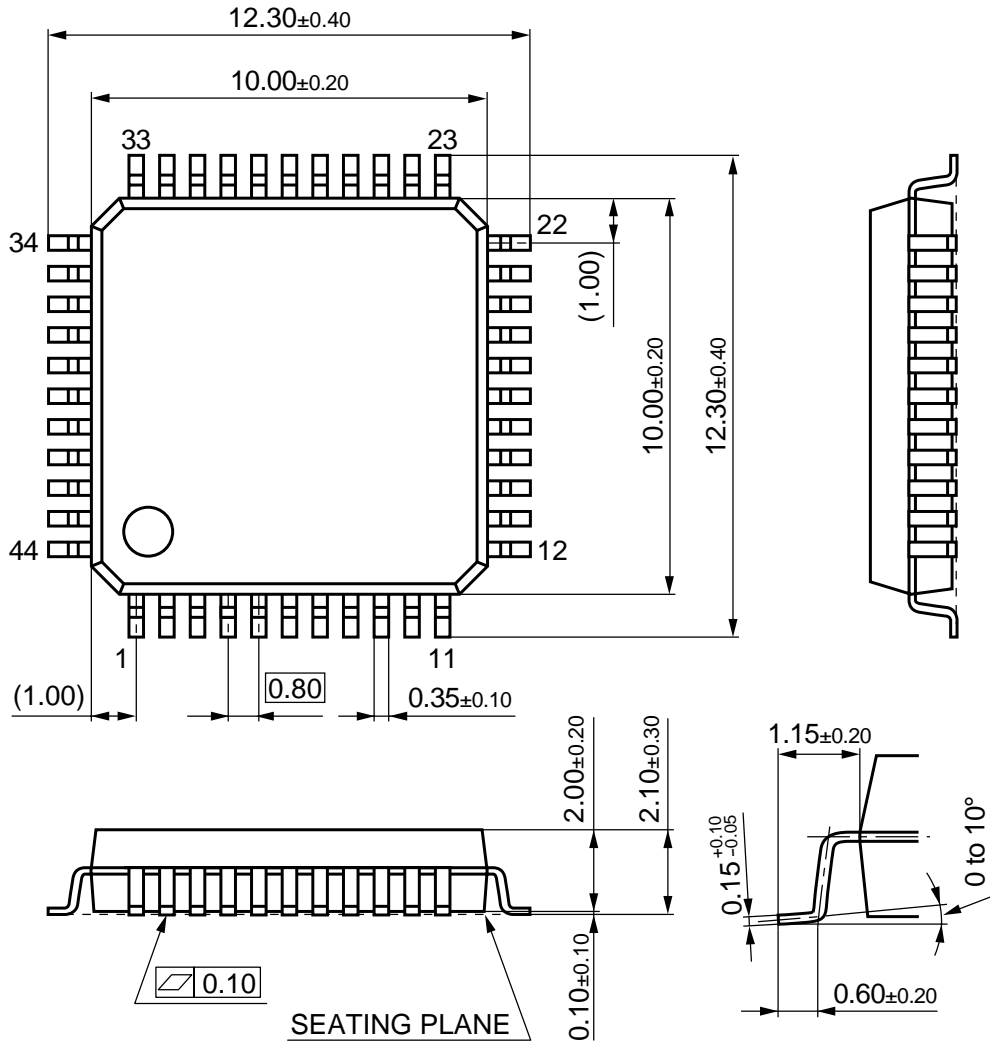


Notes

- *1: These diodes must have a V_F of 0.7V.
- *2: These diodes must be Schottky barrier diodes (MA723).
- *3: The booster circuit's electrolytic capacitors (C1 to C8) and voltage stabilization capacitors (C9 and C10) must have little impedance fluctuation at low temperatures.

■ Package Dimensions (Unit: mm)

QFP044-P-1010



■ Usage Notes

External components

1. This product requires two Schottky barrier diodes.

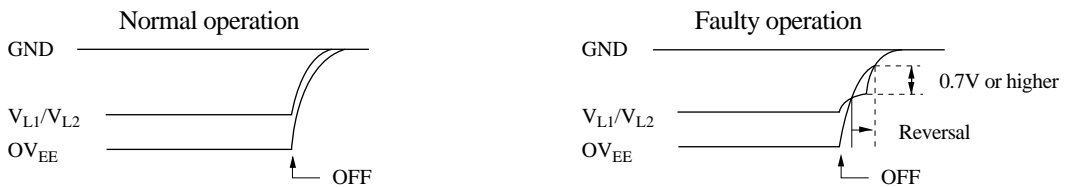
We recommend the following components.

Schottky barrier diodes: MA723 or equivalents

Ta=25°C

| Component | Model number | Typical characteristics | Notes |
|-------------------------|--------------|--|-------|
| Schottky barrier diodes | MA723 | $I_F = 200\text{mA}$, $V_F \leq 0.55\text{V}$ | |

The MN3113F will not operate properly if the components do not satisfy the above specifications.



2. Always use the specified components for peripheral circuits so as to ensure that OV_{EE} and V_L do not reverse potentials when the power is turned off.

As the above sketch illustrates, allowing OV_{EE} to exceed V_{L1} and V_{L2} by more than 0.7 V produces the risk of applying a forward bias to the PN junction, turning on the parasitic transistor, and generating an overcurrent that produces latch-up.

If this phenomenon arises, increase the size of capacitor C8 or decrease the size of capacitor C10 to increase the OV_{EE} time constant.

(See the sample application circuit for the locations of C8 and C10.)

3. Adjusting boost voltages with SENSE pins

The MN3113F provides the SENSE pins, SENSE1 and SENSE2, for adjusting the boost voltages (V_{OUT+} and V_{OUT-}) with the following procedures.

Adjusting the positive boosted voltage

(1) Making $V_{OUT+} < 15V$

Insert a resistor, R, between the SENSE1 pin (pin 17) and the V_{OUT+} pin (pin 16). The theoretical output voltage at the V_{OUT+} pin is then given by the following formula.

$$V_{OUT+'} = V_{CC} \times \frac{50k\Omega + 100k\Omega/R}{50k\Omega}$$

(where $100\text{ k}\Omega/R$ is the effective resistance of the $100\text{ k}\Omega$ resistor and R connected in parallel.)

For example, if R is $50\text{ k}\Omega$,

$$V_{OUT+'} = 5 \times \frac{50k\Omega + 33.3k\Omega}{50k\Omega} = 8.3V$$

(2) Making $V_{OUT+} > 15V$

Insert a resistor, R, between the SENSE1 pin (pin 17) and the GND pin (pin 42).

$$V_{OUT+'} = V_{CC} \times \frac{50k\Omega/R + 100k\Omega}{50k\Omega/R}$$

Adjusting the negative boosted voltage

(1) Making $V_{OUT-} < -10V$

Insert a resistor, R, between the SENSE2 pin (pin 39) and the GND pin (pin 42).

$$V_{OUT-'} = V_{CC} \times \frac{50k\Omega/R + 50k\Omega}{50k\Omega/R}$$

(2) Making $V_{OUT-} > -10V$

Insert a resistor, R, between the SENSE2 pin (pin 39) and the V_{OUT-} pin (pin 40).

$$V_{OUT-'} = -V_{CC} \times \frac{50k\Omega + 50k\Omega/R}{50k\Omega}$$

For example, if R is $50\text{ k}\Omega$,

$$V_{OUT-'} = -5 \times \frac{50k\Omega + 25k\Omega}{50k\Omega} = -7.5V$$

Note, however, that the above formulas are mere guidelines, that the internal resistances vary between samples, and that therefore each sample will have to be adjusted.

Note also that booster circuit capacity and output load current impose limits on adjustments for boosting V_{OUT+} above $15V$ and V_{OUT-} below $-10V$.

(The maximum possible adjustments are $20V$ for V_{OUT+} and $-15V$ for V_{OUT-} .)