PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

M66272FP

LCD CONTROLLER with VRAM

DESCRIPTION

The M66272FP is a graphic display-only controller for dot matrix type STN-LCD which is used widely for OA equipment, PDA, amusement equipment, etc.
It is capable of displaying six types of LCD by combining the panel configuration(single or dual scan), LCD display function(binary or gray scale), LCD display data bus width(4 or 8 bit).

Panel configuration	Binary/ gray scale	LCD display data	Displayable LCD size
Single scan	Binary	4bit	Equivalent to 640 x 240
		8bit	
	Gray scale	4bit	Equivalent to 320 x 240
		8bit	
Dual scan	Binary	4bit	Equivalent to 320 x 240 x 2 screens
	Gray scale	4bit	Equivalent to 320 x 120 x 2 screens

The M66272FP can support the reflective color type LCD (ECB : Electrically Controlled Birefringence).
The IC has a built-in 19200-byte VRAM as a display data memory. All of the VRAM addresses are externally opened. Direct addressing of display data can be performed from MPU, thus display data processing such as drawing can be efficiently carried out.
The built-in arbiter circuit(cycle steal system) which gives priority to display access allows timing-free access from MPU to VRAM, preventing display screen distortion.
The IC provides has a function for LCD module built-in system by lessening connect pins between the MPU and the IC.

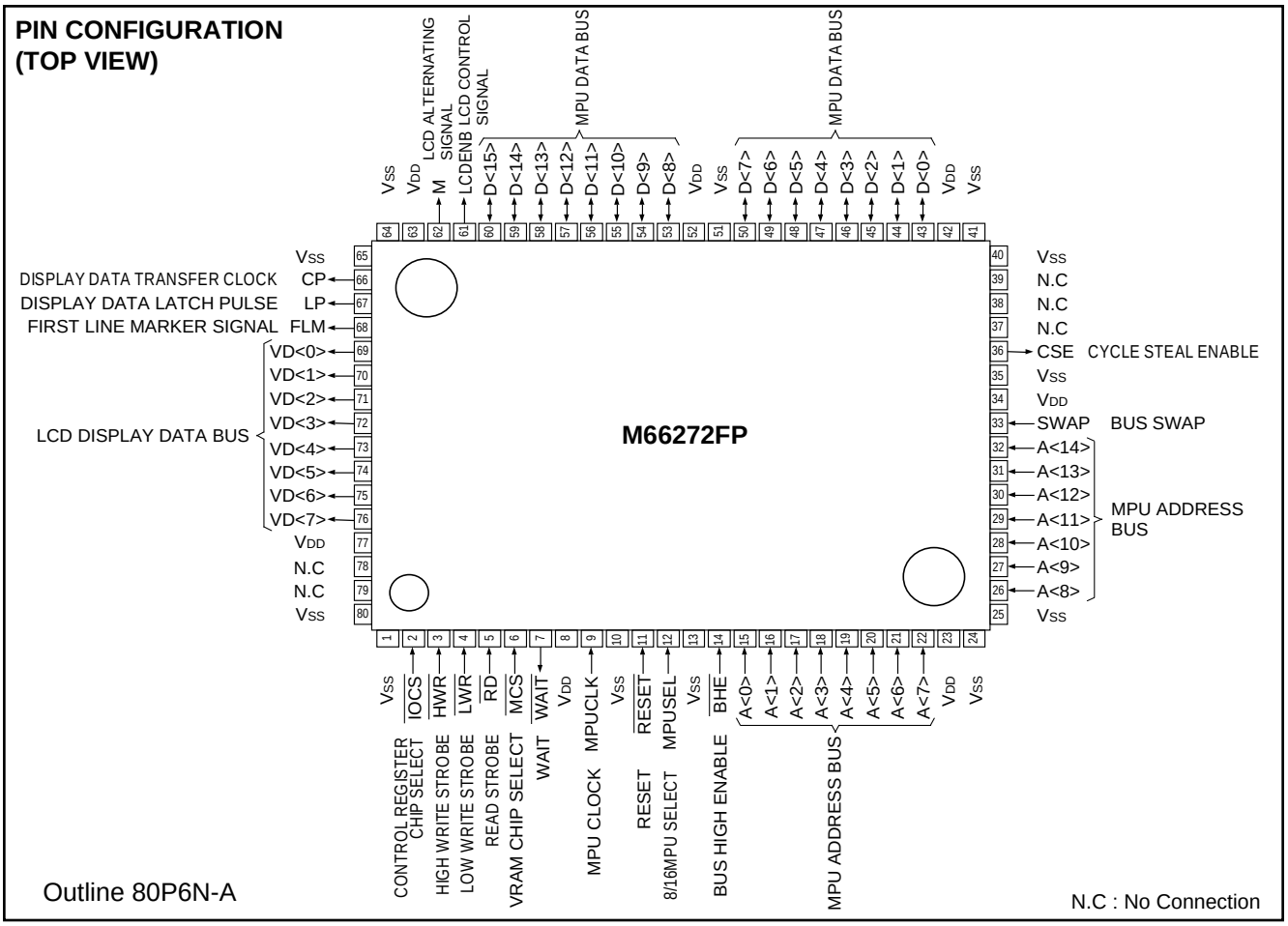
FEATURES

- Display memory
  - Built-in 19200-byte(153.6-Kbit) VRAM(Equivalent to 320 x 240 dots x 2 screens)
  - All addresses of built-in VRAM are externally opened.
- Displayable LCD
  - Binary display
    Monochrome STN-LCD of up to 153600 dots(equivalent to 1/2 VGA)
  - 4 gray scale display
    Monochrome STN-LCD of up to 76800 dots(equivalent to 1/4 VGA)
    Reflective color STN-LCD of up to 76800 dots (equivalent to 1/4 VGA)
- Interface with MPU
  - Capability of switching the interface with two-way 8/16-bit MPU
  - Provides WAIT output pin(WAIT output when access from MPU to VRAM is gained)
  - Capability of controlling BHE or LWR/HWR at the interface with a 16-bit MPU
- Interface with LCD
  - LCD display data bus is a 4-bit or 8-bit parallel output.
  - 4 kinds of control signals: CP, LP, FLM and M
- Display functions
  - Graphic display only
  - Binary or 4 gray scale display(gray scale palette is used to set pseudo medium 2 gray scale.)
  - Reflective color(ECB) uses a gray scale function.
  - Vertical scrolling is allowed within memory range.
- Additional function for LCD module built-in system
  - Capability of interfacing with two-way 8/16-bit MPU(16-bit MPU byte access is not allowed.)
  - Access from MPU to VRAM is gained via the I/O register.
- 5V or 3V single power supply

APPLICATION

- PPC/FAX operation panel, display/operation panel of other OA equipment, multifunction/public telephone
- PDA/electronic notebook/information terminal, portable terminal
- Game, Amusements, kid's computer etc.

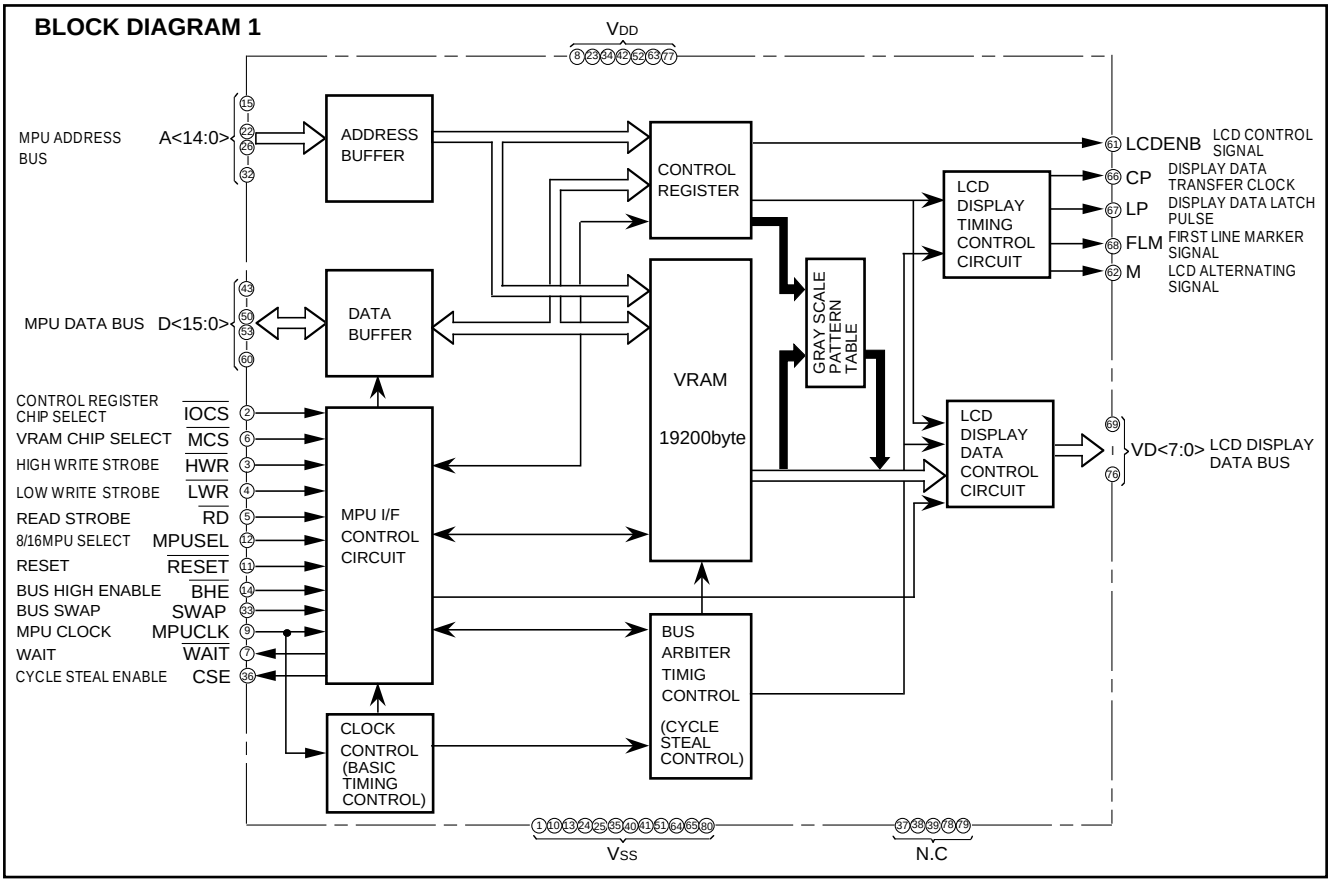
PIN CONFIGURATION (TOP VIEW)



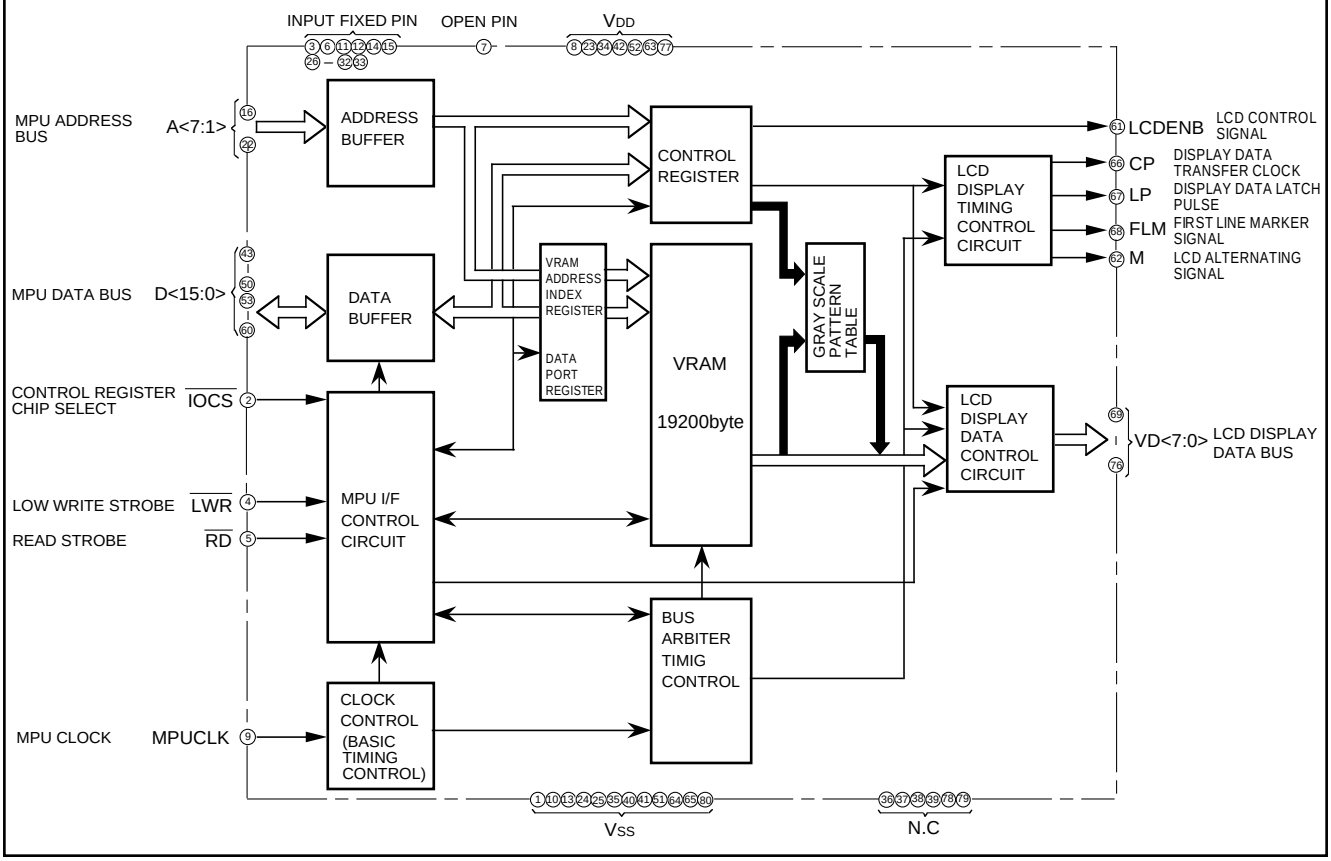
Outline 80P6N-A

N.C : No Connection

BLOCK DIAGRAM 1



BLOCK DIAGRAM 2 (When interfacing with the LCD module built-in system and having the maximum number of pins connected with MPU)



PIN DESCRIPTIONS

Item	Pin name	Input/ Output	Function	Number of pins
MPU interface	D<15:0>	Input/ Output	MPU data bus When selecting 8 bit MPU by MPUSEL input, connect D<15:8> to V_{DD} or V_{SS}.	16
	A<14:0>	Input	MPU address bus When selecting 8-bit MPU, use A<14:0>. When selecting 16-bit MPU, use A<14:1> as a address bus. By combining A<0> and $\overline{BHE}$, access to internal VRAM can be gained. When driving two screens (dual scan mode), notice that the allowable setup range of VRAM address is restricted. Use A<7:0> for selecting address of control register.	15
	$\overline{IOCS}$	Input	Chip select input of control register When this pin is "L", select the internal control register. Assign to I/O space of MPU.	1
	$\overline{MCS}$	Input	Chip select input of VRAM When this pin is "L", select the internal VRAM. Assign to memory space of MPU.	1
	$\overline{HWR}$	Input	High-Write strobe input When this pin is "L", write data to the internal VRAM. $\overline{HWR}$ is valid only in using 16-bit MPU controlled byte access by $\overline{LWR}$ and $\overline{HWR}$.	1
	$\overline{LWR}$	Input	Low-Write strobe input When this pin is "L", write data to the internal control register or VRAM.	1
	$\overline{RD}$	Input	Read strobe input When this pin is "L", read data from the internal control register or VRAM.	1
	MPUSEL	Input	8/16-bit MPU select input According to MPU, set "V_{SS}" for 8-bit MPU and set "V_{DD}" for 16-bit MPU.	1
	$\overline{RESET}$	Input	Reset input Use reset signal of MPU. When this pin is "L", initialize (reset) all internal control registers and counters.	1
	MPUCLK	Input	MPU clock Input system clock output from MPU.	1
	$\overline{BHE}$	Input	Bus-High-Enable input This pin is valid when using 16-bit MPU controlling byte access with A<0> and $\overline{BHE}$. Connect to "V_{DD}" to select 8-bit MPU.	1
	SWAP	Input	Bus swap input When selecting 16-bit MPU, connect SWAP to "V_{SS}" to transfer VD<n:0> in order of Upper/Lower byte of MPU data bus, reversally connect to "V_{DD}" in order of Lower/Upper byte. When selecting 8-bit MPU, connect to "V_{SS}". Even if connecting to "V_{DD}", use D<7:0> to access to register of 8-bit width.	1
	$\overline{WAIT}$	Output	WAIT output for MPU This signal makes WAIT for MPU. Change $\overline{WAIT}$ to "L" at timing of falling edge of overlapping with $\overline{MCS}$ and $\overline{RD}$ or $\overline{LWR}$ and $\overline{HWR}$. And return to "H" at synchronization with the rising edge of MPUCLK after internal processing. (Output $\overline{WAIT}$ only when requested access from MPU to VRAM is gained during cycle steal access.)	1
	CSE	Output	Cycle Steal Enable output State output of internal cycle steal access.	1
LCD interface	VD<7:0>	Output	Display data bus for LCD Transfer the LCD display data in synchronization with a rising edge of CP by putting 4-bit or 8-bit in parallel. The VD<n:0> output pin in use differs depending on the number of driven screens and the display mode.	8
	CP	Output	Display data transfer clock Shift clock for the transfer of display data to LCD. Take the display data of VD<n:0> to LCD at falling edge of CP.	1
	LP	Output	Display data latch pulse This clock use both as the latch pulse of display data for LCD and the transfer of scanning signal. LP is output when it finishes transferring display data of a line. Latch of display data and the transfer of scanning signal at falling edge of LP.	1
	FLM	Output	First Line Marker signal output Output the start pulse of scanning line. This signal is "H" active, the IC for driving scanning line catches FLM at falling edge of LP.	1
	M	Output	LCD alternating signal output Signal for driving LCD by alternating current.	1
	LCDENB	Output	LCD (ON/OFF) control signal output Output data which is set at bit "0" of mode register (R1) in the control register. This signal can be used for controlling the LCD power supply, because LCDENB is set to "L" by RESET.	1
Others	V_{DD}	——	Power supply pin	7
	V_{SS}	——	Ground	12
	N.C	——	No connection	5

OUTLINE

M66272FP is a graphic display only controller for displaying a dot matrix type STN-LCD.

- LCD display mode
  It is capable of displaying six types of LCD by combining the panel configuration, binary/gray scale, LCD display data bus width.

Display mode	Panel configuration	Binary/ gray scale	LCD display data	Displayable LCD size
①	Single scan	Binary	4bit	Equivalent to 640 x 240
②			8bit	
③		Gray scale	4bit	Equivalent to 320 x 240
④			8bit	
⑤	Dual scan	Binary	4bit	Equivalent to 320 x 240 x 2 screens
⑥		Gray scale	4bit	Equivalent to 320 x 240 x 2 screens

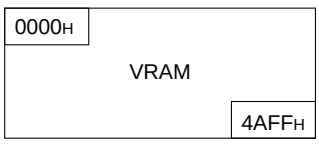
- Control register
  When accessing the control register from MPU, use pins $\overline{IOCS}$, $\overline{LWR}$, $\overline{RD}$, A<7:0> and D<7:0>. (However, use D<15:0> only when 16-bit MPU controls the LCD module built-in support function.)
  The IC contains the following registers as control registers.

Operation control	R1 to R11
Supporting LCD module built-in type	R12 to 14 or R15 to 16
Gray scale pattern table	R17 to R80

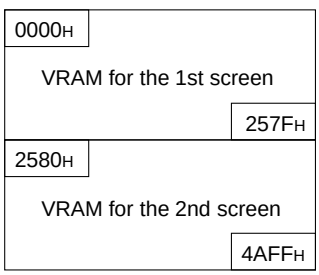
- VRAM
  This IC has a built-in 19200-byte VRAM which is equivalent to two screens of 320 x 240 dots LCD.
  When accessing VRAM from MPU, use pins $\overline{MCS}$, $\overline{HWR}$, $\overline{LWR}$, $\overline{RD}$, $\overline{BHE}$, A<14:0> and D<15:0>.
  Use of MPUSEL input can support both 8-bit MPU and 16-bit MPU.
  The VRAM address settable range is restricted depending on the panel configuration, as follows.

VRAM address settable range

♦When single scan mode
- A<14:0>=0000 to 4AFF$_H$ --- 19200 byte



♦When dual scan mode
- For the 1st screen --- A<14:0>=0000 to 257F$_H$ --- 9600 byte
- For the 2nd screen --- A<14:0>=2580 to 4AFF$_H$ --- 9600 byte



- Cycle steal system
  Cycle steal system is interact method of transforming display data for LCD from VRAM and accessing VRAM from MPU on the basic cycle (MAINCLK) of internal operation.
  Basic timing is two clocks of MAINCLK, and assign first clock to the access from MPU to VRAM and second clock to the transfer of display data from VRAM to LCD.

  In accessing VRAM from MPU, output $\overline{WAIT}$. Change $\overline{WAIT}$ to "L" at the timing of the falling edge of overlapping with $\overline{MCS}$ and $\overline{RD}$ or $\overline{LWR}$ / $\overline{HWR}$, and return to "H" at synchronizing with rising edge of MPUCLK after internal processing.
  For the cycle steal system, this IC provides a cycle steal control function to improve data transfer efficiency in a line. This function gains access with the cycle steal system by taking $\overline{WAIT}$ for MPU during the display term with necessity for the display data transfer from built-in VRAM to LCD. On the other side, it does not output $\overline{WAIT}$ for keeping throughput of MPU during horizontal synchronous term (idle running term) with no necessity for the display data transfer from VRAM to LCD side.

- Output to LCD side
  LCD display data VD<7:0> is output in parallel per 4 bits or 8 bits in synchronization with the rising edge of CP.
  Pin VD<n:0> differs depending on the display mode.

Single scan		Dual scan
4-bit transfer	8-bit transfer	4-bit transfer
		VD<7:4>
VD<3:0>	VD<7:0>	VD<3:0>

Display mode ①③ ②④ ⑤⑥

  When display data for a line has been sent, LP outputs data in synchronization with the falling edge of MAINCLK.
  The IC enables adjustment to an optimum value of the frame frequency as requested from the LCD PANEL side by adjusting pulse width of LP with the LPW register value.
  FLM is output when the display data for the first line has been sent.
  M output is an LCD alternating signal for driving LCD with alternating current.
  M output cycles can be set in lines with the M output cycle variable register and is available to prevent LCD from deterioration.

- Gray scale display function
  Gray scale display can assign 2-bit VRAM data to a picture element of LCD display to show the display density at four levels.
  Gray scale display pattern tables 0 and 1 (4 x 4 matrix x 16 patterns x 2 medium gray scale), consisting of SRAM of 64 bytes in total, can set any gray scale display pattern.

- Application to reflective color type LCD
  The above gradation display function is available to control about four display colors on the reflective color type LCD with ECB (Electrically Controlled Birefringence).