

# FMM5057VF

## 7.1-8.5GHz Power Amplifier MMIC

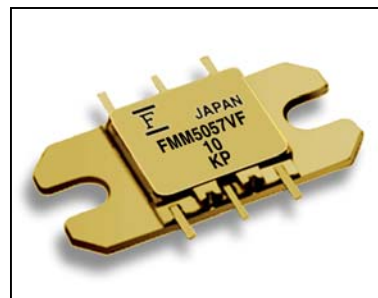
### FEATURES

- High Output Power: 34.0dBm(typ.)
- High Linear Gain: 26.0dB(typ.)
- Low VSWR
- Broad Band: 7.1 ~ 8.5GHz
- Impedance Matched  $Z_{in}/Z_{out} = 50\Omega$
- Small Hermetic Metal-Ceramic Package(VF)

### DESCRIPTION

The FMM5057VF is a MMIC amplifier that contains a four-stage amplifier, internally matched, for standard communications band in the 7.1 to 8.5GHz frequency range.

Fujitsu's stringent Quality Assurance Program assures the highest reliability and consistent performance.



### ABSOLUTE MAXIMUM RATINGS (Case Temperature $T_c=25^\circ\text{C}$ )

Item	Symbol	Rating	Unit
DC Input Voltage	$V_{DD}$	12	V
DC Input Voltage	$V_{GG}$	-7	V
Input Power	$P_{in}$	14	dBm
Storage Temperature	$T_{stg}$	-55 to +125	$^\circ\text{C}$

### Recommended Operating Condition

Item	Symbol	Condition	Unit
DC Input Voltage at $T_c=25^\circ\text{C}$	$V_{DD}$	10	V
Input Power at $T_c=25^\circ\text{C}$	$P_{in}$	12	dBm
DC Input Current at $T_c=25^\circ\text{C}$	$I_{DD}$	$\leq 1200$	mA
Operating Case Temperature	$T_c$	-40 to +85	$^\circ\text{C}$

### ELECTRICAL CHARACTERISTICS (Case Temperature $T_c=25^\circ\text{C}$ )

Item	Symbol	Test Conditions	Limit			Unit
			Min.	Typ.	Max.	
Frequency Range	f		7.1 - 8.5			GHz
Output Power at 1dB G.C.P.	$P_{1dB}$	$V_{DD}=10\text{V}$ $V_{GG}=-5\text{V}$ $f=7.1$ to $8.5\text{GHz}$	32.0	34.0	-	dBm
Power Gain at 1dB G.C.P.	$G_{1dB}$		23.0	26.0	-	dB
Gain Flatness	$\Delta G$		-	2.4	4.0	dB
Input VSWR	$VSWR_i$		-	2 : 1	2.6 : 1	-
Output VSWR	$VSWR_o$		-	2 : 1	-	-
DC Input Current	$I_{DD}$	$V_{DD}=10\text{V}, V_{GG}=-5\text{V}$	-	1100	1200	mA
DC Input Current	$I_{GG}$		-	5.0	15.0	mA
Channel Temperature Rise	$\Delta T_{ch}$		-	50	-	$^\circ\text{C}$

### CASE STYLE: VF

Note:  $G_{1dB}$  is referenced to Linear Gain measured at  $P_{in}=-3\text{dBm}$ .

G.C.P.: Gain Compression Point

ESD	Class 0	~ 199 V
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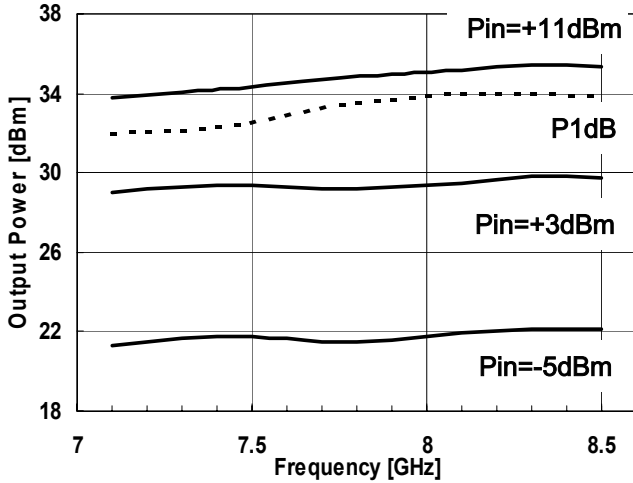
Note : Based on EIAJ ED-4701 C-111A(C=100pF, R=1.5k $\Omega$ )

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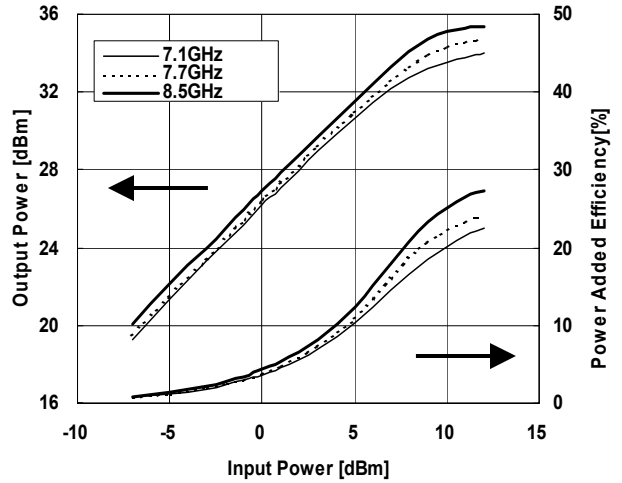
OUTPUT POWER vs. FREQUENCY

VDD=10V, VGG=-5V



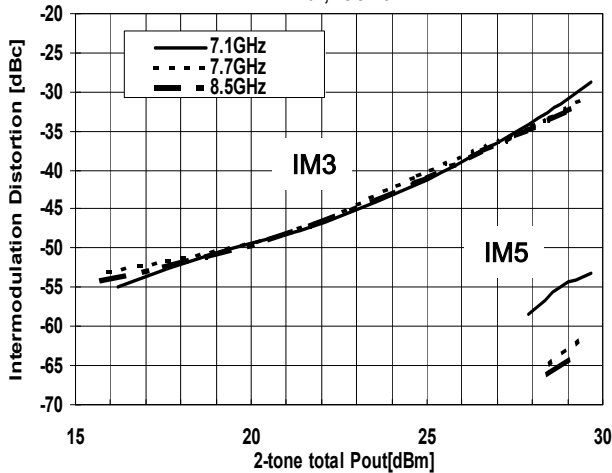
OUTPUT POWER, POWER ADDED EFFICIENCY vs. INPUT POWER

VDD=10V, VGG=-5V



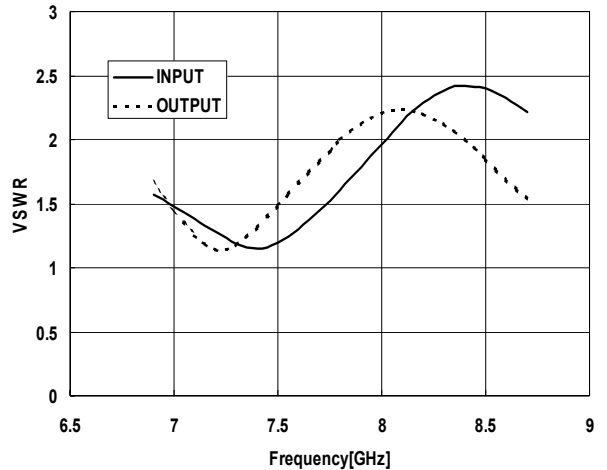
IMD vs. OUTPUT POWER

VDD=10V, VGG=-5V



VSWR vs. FREQUENCY

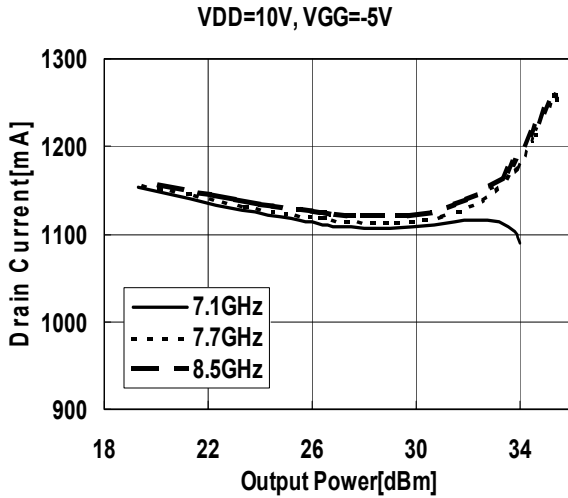
VDD=10V, VGG=-5V



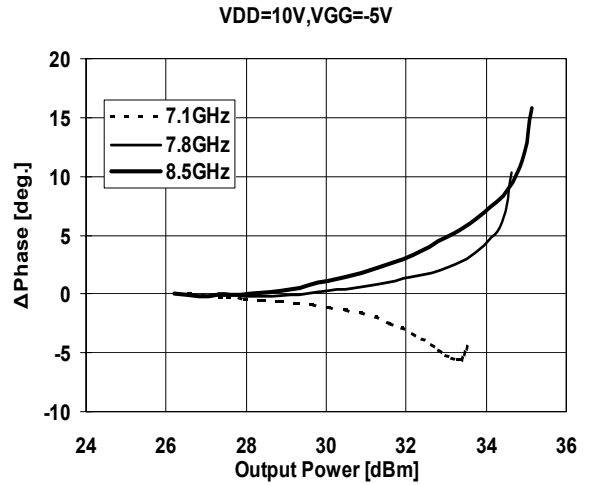
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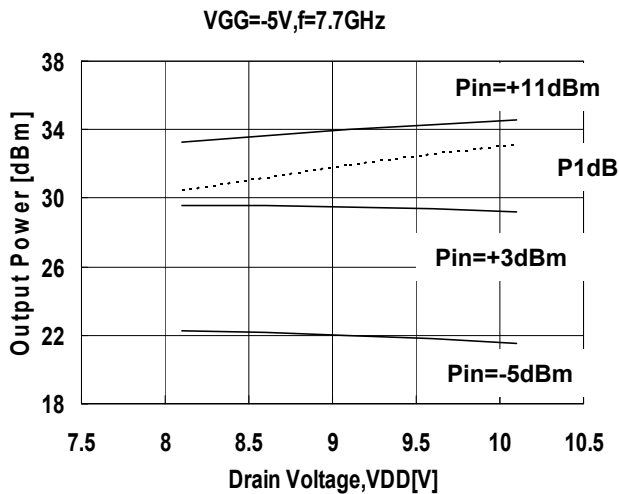
**DRAIN CURRENT vs OUTPUT POWER**



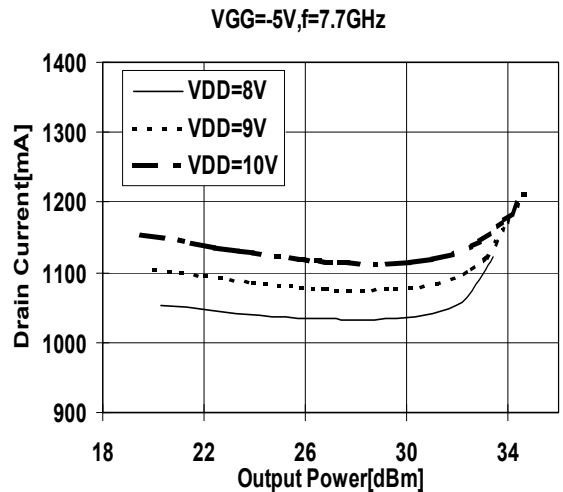
**AMPM vs OUTPUT POWER**



**OUTPUT POWER vs. DRAIN VOLTAGE**



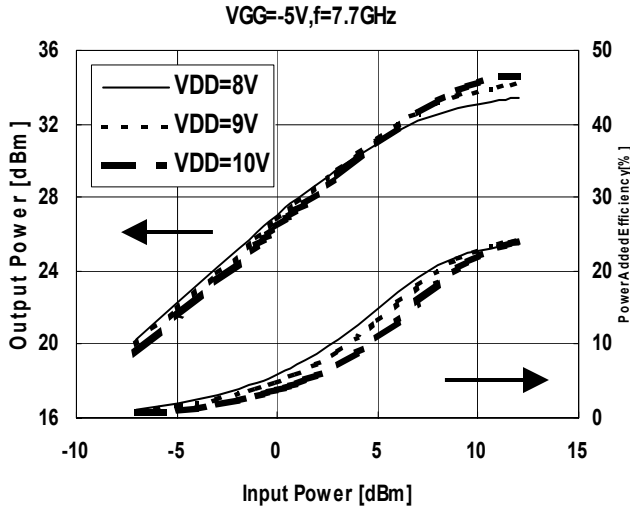
**DRAIN CURRENT vs OUTPUT POWER**



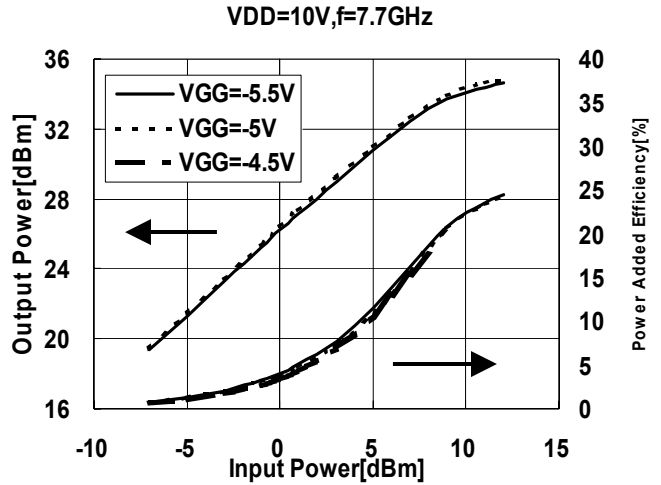
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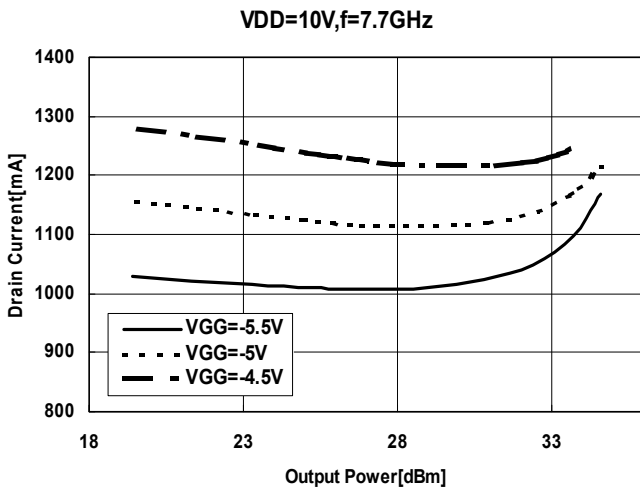
OUTPUT POWER , POWER ADDED EFFICIENCY vs. INPUT POWER



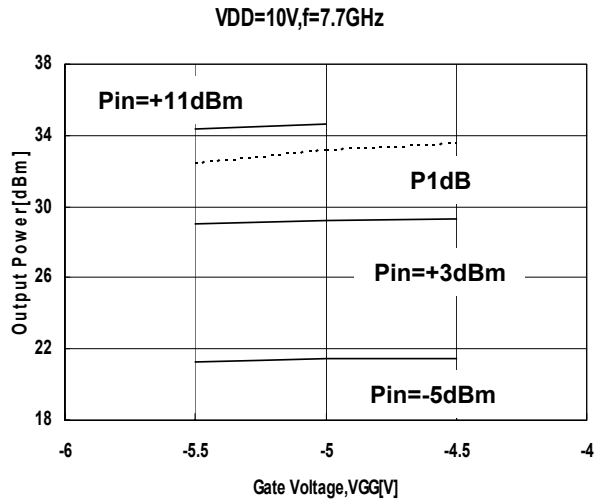
OUTPUT POWER , POWER ADDED EFFICIENCY vs. INPUT POWER



DRAIN CURRENT vs OUTPUT POWER



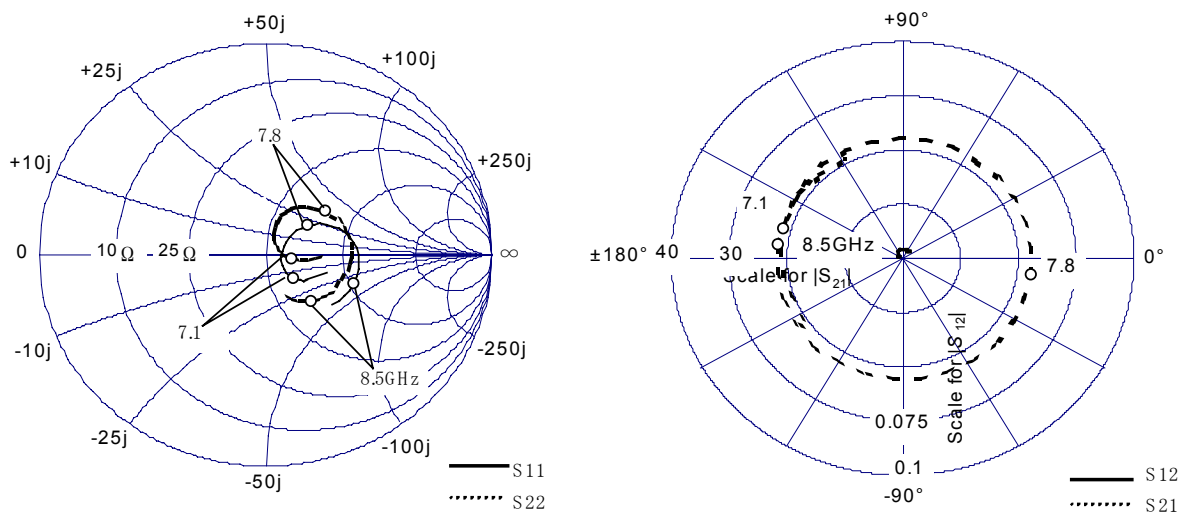
OUTPUT POWER vs. GATE VOLTAGE



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### ■ S-PARAMETER



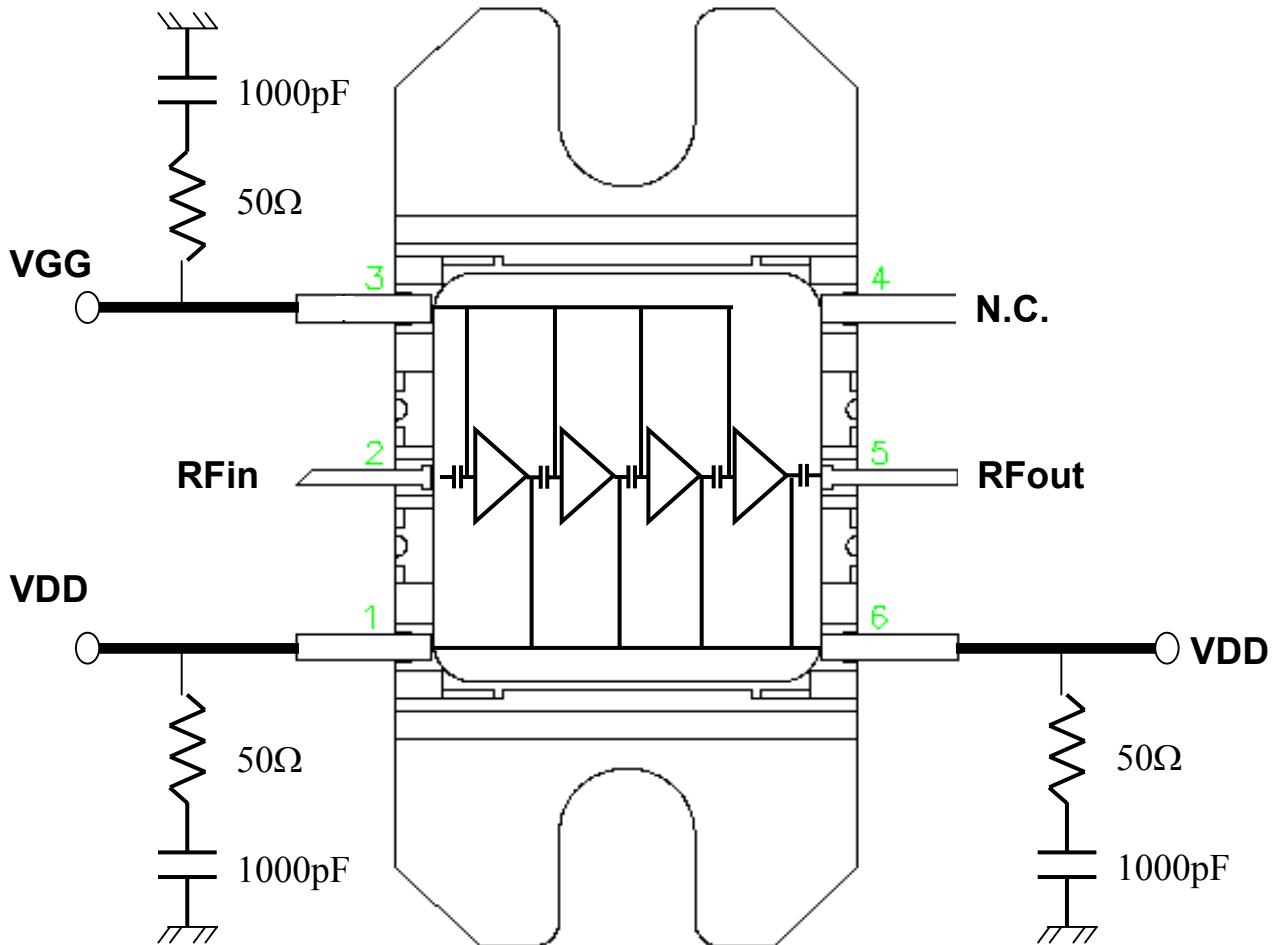
VDD=10.0V, VGG=-5.0V

Frequency [GHz]	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
6.9	0.22	-32.75	20.21	-147.13	0.0018	141.10	0.25	-1.17
7	0.19	-38.49	20.78	-171.17	0.0017	139.86	0.18	-7.55
7.1	0.16	-42.30	21.29	164.64	0.0017	144.62	0.11	-6.51
7.2	0.12	-42.44	21.74	140.28	0.0018	148.20	0.07	20.06
7.3	0.09	-32.59	22.04	115.51	0.0020	146.45	0.08	63.42
7.4	0.07	-2.59	22.24	90.84	0.0022	148.64	0.14	73.27
7.5	0.09	28.05	22.33	66.15	0.0025	143.94	0.20	68.70
7.6	0.13	38.99	22.35	41.55	0.0028	139.92	0.25	59.98
7.7	0.18	40.08	22.42	17.21	0.0031	134.35	0.29	49.76
7.8	0.23	36.58	22.37	-7.47	0.0033	127.55	0.33	38.34
7.9	0.28	31.41	22.44	-32.13	0.0036	121.48	0.36	26.63
8	0.33	24.61	22.42	-56.99	0.0038	116.50	0.38	14.30
8.1	0.36	16.99	22.41	-82.39	0.0040	105.95	0.38	1.81
8.2	0.39	8.76	22.35	-108.02	0.0042	97.60	0.37	-10.89
8.3	0.41	-0.24	22.15	-133.79	0.0044	89.83	0.36	-23.72
8.4	0.42	-9.50	21.99	-160.00	0.0044	81.16	0.33	-35.94
8.5	0.41	-19.29	21.71	173.43	0.0043	72.49	0.30	-47.13
8.6	0.40	-28.69	21.40	146.38	0.0041	63.50	0.26	-57.41

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### Recommended Bias Circuit and Internal Block Diagram



Note 1: The RC networks are recommended on the bias supply lines, close to the package, to prevent video oscillations which could damage the module.

Note 2: Bias point VDD can be connected at the input side or at the output. The two pins named VDD are internally connected.

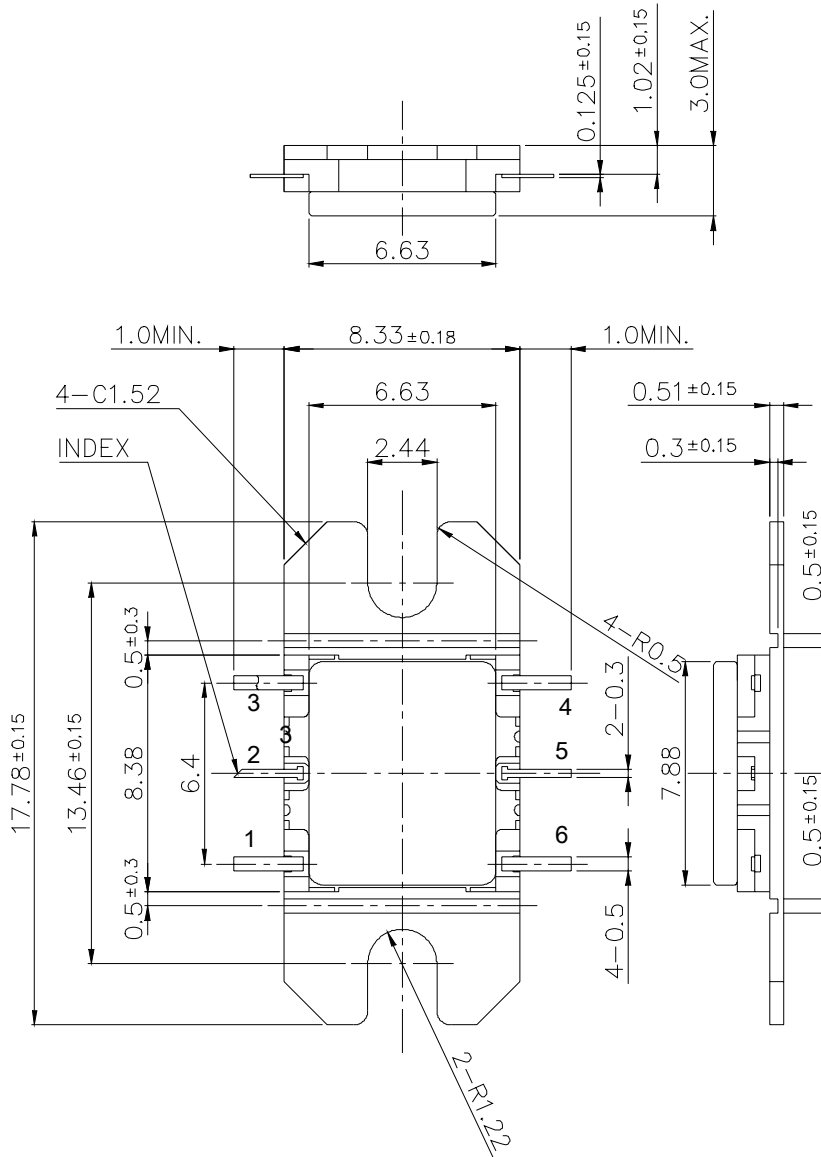
#### PIN ASSIGNMENT

- 1 : VDD
- 2 : RF in
- 3 : VGG
- 4 : N.C.
- 5 : RF out
- 6 : VDD

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### ■ Package Out Line



#### PIN ASSIGNMENT

- 1 : VDD
- 2 : RF in
- 3 : VGG
- 4 : N.C.
- 5 : RF out
- 6 : VDD

Unit : mm

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