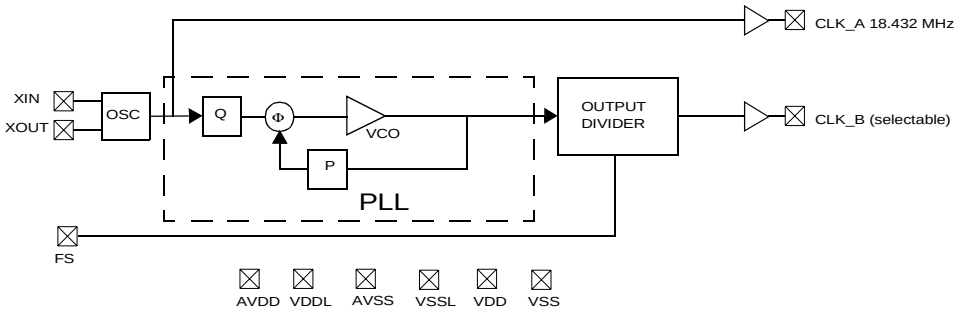
MediaClock™ Graphics Clock Generator

Features	Benefits
• **Integrated phase-locked loop (PLL)**	High-performance PLL tailored for multimedia applications
• **Low-jitter, high-accuracy output**	Meets critical timing requirements in complex system designs
• **3.3V operation with 2.5V/1.68V output**	Enables application compatibility
• **Ultra-linear crystal capacitors**	Ensures 0PPM Accuracy

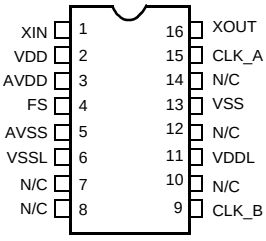
Part Number	Outputs	Input Frequency Range	Output Frequencies
CY24141-3	2	18.432 MHz	18.432 MHz, 53.94605395 MHz/54 MHz (selectable)

Logic Block Diagram



Pin Configurations

CY24141ZC-3
16-pin TSSOP



CY24141 Frequency Select Table

Frequency Select	PPM	CLK_B	Unit
1	–1.000073	53.94605395	MHz
0	0	54	MHz

Pin Summary

Pin Name	Pin Number	Pin Description
X_{IN}	1	Reference Input
V_{DD}	2	Voltage Supply
AV_{DD}	3	Analog Voltage Supply
FS	4	Frequency Select Pin (Internal Pull-down Resistor)
AV_{SS}	5	Analog Ground
V_{SSL}	6	Output Ground
N/C	7	No Connect
N/C	8	No Connect
CLK_B	9	53.94605395-MHz/54-MHz Clock Output (Frequency Selectable) @ V_{DDL} level
N/C	10	No Connect
V_{DDL}	11	Output Voltage Supply for CLK_B
N/C	12	No Connect
V_{SS}	13	Ground
N/C	14	No Connect
CLK_A	15	18.432-MHz Clock Output
XOUT[1]	16	Reference Output

Absolute Maximum Conditions

Parameter	Description	Min.	Max.	Unit
AVDD	Supply Voltage	–0.5	7.0	V
T_S	Storage Temperature[2]	–65	125	°C
T_J	Junction Temperature		125	°C
	Digital Inputs	V_{SS} – 0.3	V_{DD} + 0.3	V
	Digital Outputs referred to V_{DD}	V_{SS} – 0.3	V_{DD} + 0.3	V
	Electrostatic Discharge		2000	V

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
AVDD	Analog Voltage Supply	3.15	3.45	3.6	V
VDD	Voltage Supply	3.15	3.45	3.6	V
$VDDL_H$	2.5V Output Voltage Supply	2.25	2.5	2.75	V
$VDDL_L$	1.68V Output Voltage Supply	1.63	1.68	1.75	V
T_A	Ambient Temperature	0		85	°C
C_{LOAD}	Max Load Capacitance			15	pF
f_{REF}	Reference Frequency		18.432		MHz

Note:
1. Float X_{OUT} if X_{IN} is externally driven.
2. Rated for 10 years.

DC Electrical Characteristics

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$I_{OH3.3}$	Output High Current	$V_{OH} = V_{DD} – 0.5$, $V_{DD} = 3.3$ V	12	24		mA
$I_{OL3.3}$	Output Low Current	$V_{OL} = 0.5$, $V_{DD} = 3.3$ V	12	24		mA
$I_{OH2.5}$	Output High Current	$V_{OH} = V_{DDL} – 0.5$, $V_{DDL} = 2.5$ V	8	20		mA
$I_{OL2.5}$	Output Low Current	$V_{OL} = 0.5$, $V_{DDL} = 2.5$ V	8	20		mA
$I_{OH1.68}$	Output High Current	$V_{OH} = V_{DDL} – 0.5$, $V_{DDL} = 1.68$ V	6	12		mA
$I_{OL1.68}$	Output Low Current	$V_{OL} = 0.5$, $V_{DDL} = 1.68$ V	6	12		mA
V_{IH}	Input High Voltage	FS Frequency Select Input	70%			V_{DD}
V_{IL}	Input Low Voltage	FS Frequency Select Input			30%	V_{DD}
R_I	Input Resistor	FS Frequency Select Pull Down Resistor	80	100	135	kohm
C_{IN}	Input Capacitance				7	pF
X_{LDCAP}	Crystal Load Capacitance	Internal Load Caps		12.9		pF
I_{IZ}	Input Leakage Current			5	10	µA
I_{DD}	Supply Current	Sum of Core and Output Current		30	35	mA

Cycle-Cycle Jitter Specifications (V_{DD} = 3.15V–3.6V)

Parameter	Description	Conditions	1σ	Typ.	Max.	Unit
t_9	Clock Jitter–peak-peak	Cycle-Cycle Jitter–18.432 MHz	12	55	140	ps
t_9	Clock Jitter–peak-peak	Cycle-Cycle Jitter–54 MHz V_{DDL} = 1.63V–1.75V	32	135	220	ps
t_9	Clock Jitter–peak-peak	Cycle-Cycle Jitter–54 MHz V_{DDL} = 2.25V–2.75V	11	70	150	ps
t_9	Clock Jitter–peak-peak	Cycle-Cycle Jitter–53.94605395 MHz V_{DDL} = 1.63V–1.75V	31	160	220	ps
t_9	Clock Jitter–peak-peak	Cycle-Cycle Jitter–53.94605395 MHz V_{DDL} = 2.25V–2.75V	11	70	150	ps

1000-cycle Jitter (V_{DD} = 3.15V–3.6V)

Parameter	Description	Conditions	1σ	Typ.	Max.	Unit
t_{10}	Clock Jitter–peak-peak	1000-Cycle-Cycle Jitter–18.432 MHz	19	95	140	ps
t_{10}	Clock Jitter–peak-peak	1000-Cycle-Cycle Jitter–54 MHz V_{DDL} = 1.63V–1.75V	55	275	400	ps
t_{10}	Clock Jitter–peak-peak	1000-Cycle-Cycle Jitter–54 MHz V_{DDL} = 2.25V–2.75V	50	275	400	ps
t_{10}	Clock Jitter–peak-peak	1000-Cycle-Cycle Jitter–53.94605395 MHz–V_{DDL} = 1.63V–1.75V	293	1025	1200	ps
t_{10}	Clock Jitter–peak-peak	1000-Cycle-Cycle Jitter–53.94605395 MHz–V_{DDL} = 2.25V–2.75V	290	1025	1200	ps

Phase Noise Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
	Phase Noise	18.432 MHz @ 10-kHz offset		–119		dBc
	Phase Noise	54 MHz @ 10-kHz offset		–95		dBc
	Phase Noise	53.94605395 MHz @ 10-kHz offset		–92		dBc

AC Electrical Characteristics (V_{DD} = 3.15V–3.6V)

Parameter[3]	Description	Conditions	Min.	Typ.	Max.	Unit
F_{ppm}	Frequency Error	Part to Part (three lots tested on same board, PCB board can vary more than ±5 ppm)		±5	±10	ppm
F_{ppm}	Frequency Error	Over temperature from 0 to 85°C (crystal should not be heated for this test, only IC)		±2	±5	ppm

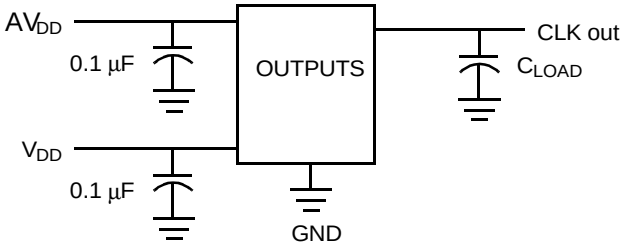
Note:

3. Not 100% tested.

AC Electrical Characteristics (V_{DD} = 3.15V–3.6V) (continued)

Parameter[3]	Description	Conditions	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in Figure 1, 50% of V_{DD}	45	50	55	%
t_3	Rising Edge Slew Rate	Output Clock Rise Time, 20%–80% of V_{DD}/ V_{DDL} = 2.5V	0.8	1.4		V/ns
t_4	Falling Edge Slew Rate	Output Clock Fall Time, 80%–20% of V_{DD}/ V_{DDL} = 2.5V	0.8	1.4		V/ns
t_5	PLL Lock Time				3	ms

Test Circuit



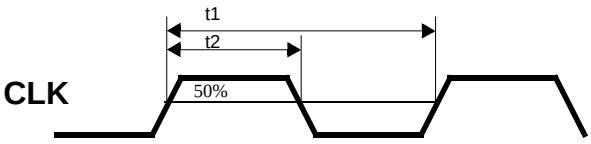


Figure 1. Duty Cycle Definition; DC = t2/t1

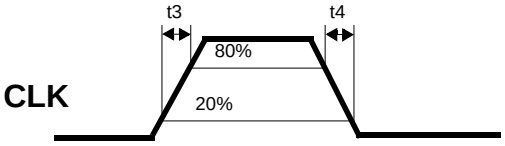


Figure 2. Rise and Fall Time Definitions

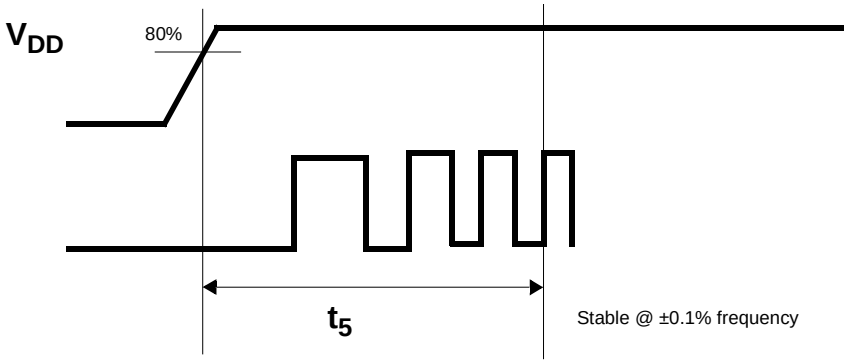


Figure 3. PLL Lock Time

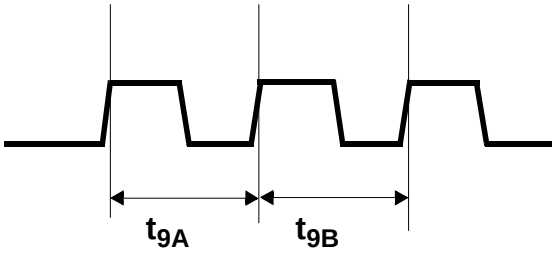


Figure 4. Cycle-Cycle Jitter

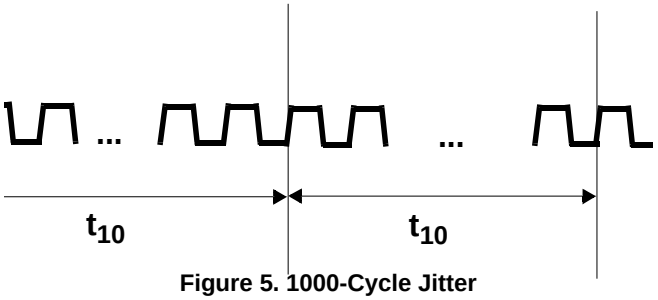
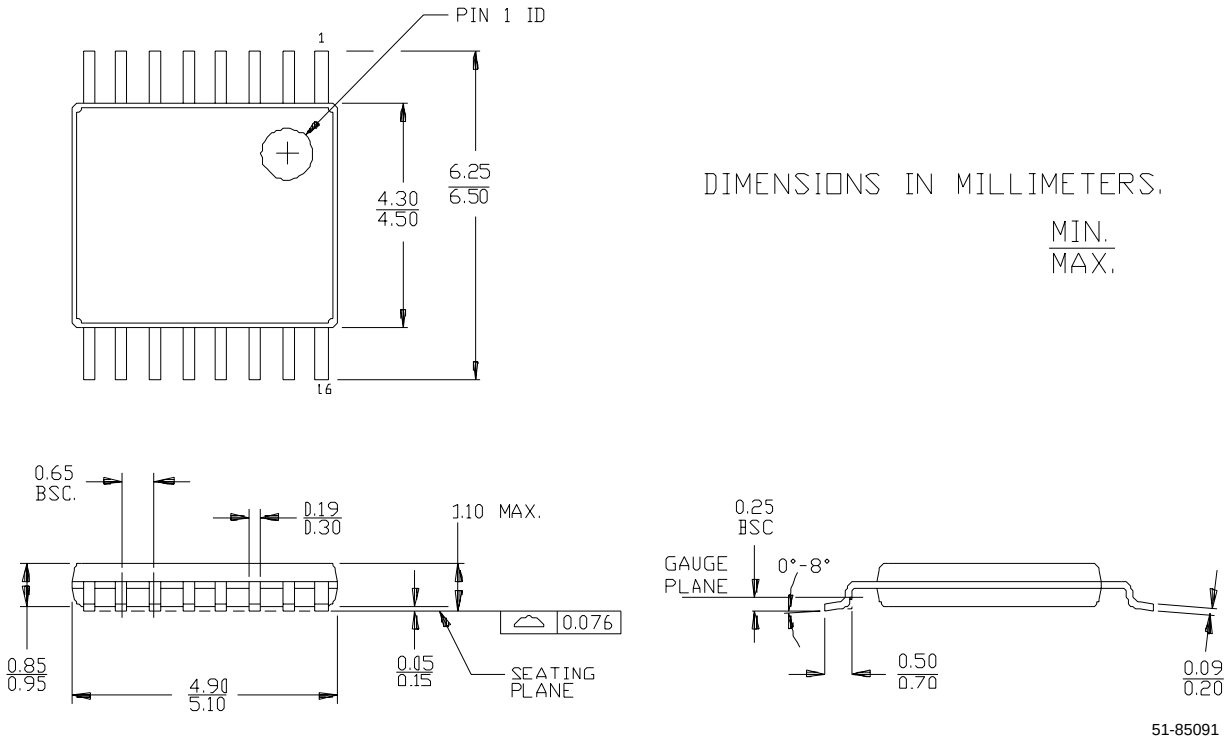


Figure 5. 1000-Cycle Jitter

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY24141ZC-3	Z16	16-TSSOP	Commercial	3.3V

16-lead Thin Shrunk Small Outline Package (4.40-MM Body) Z16



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**	111593	04/30/02	CKN	New Data Sheet