ANALOG DEVICES

LC²MOS GSM Baseband I/O Port

AD7001

FEATURES

Single +5 V Supply
Single Channel 8-Bit A/D Converter
- **2.16 MHz Sampling Rate**
- **Receive Difference Amplifier**
- **Programmable Gain Amplifier**

Two 10-Bit D/A Converters
- **2 MHz Throughput Rate**
- **Simultaneous Update Mode**
- **4th Order Antialias Filters**

Single Serial Auxiliary 8-Bit D/A Converter
Fast Interface Port
Power Down Mode(s)
On-Chip Voltage Reference
44-Pin PQFP

APPLICATIONS

Digital Cellular Telephony
Private Mobile Telephony
Satellite Baseband Digitization
Radar Signal Processing
Signal Generation and Acquisition

GENERAL DESCRIPTION

The AD7001 is a complete low power, LC²MOS, input/output port with single +5 V power supply. The part is designed to perform the conversion of I and Q signals in the transmit and receive data paths of Pan-European Digital Cellular Telephone (GSM) systems. However, the device can be used in any application requiring fast and accurate signal conversion in the sub-600 kHz band.

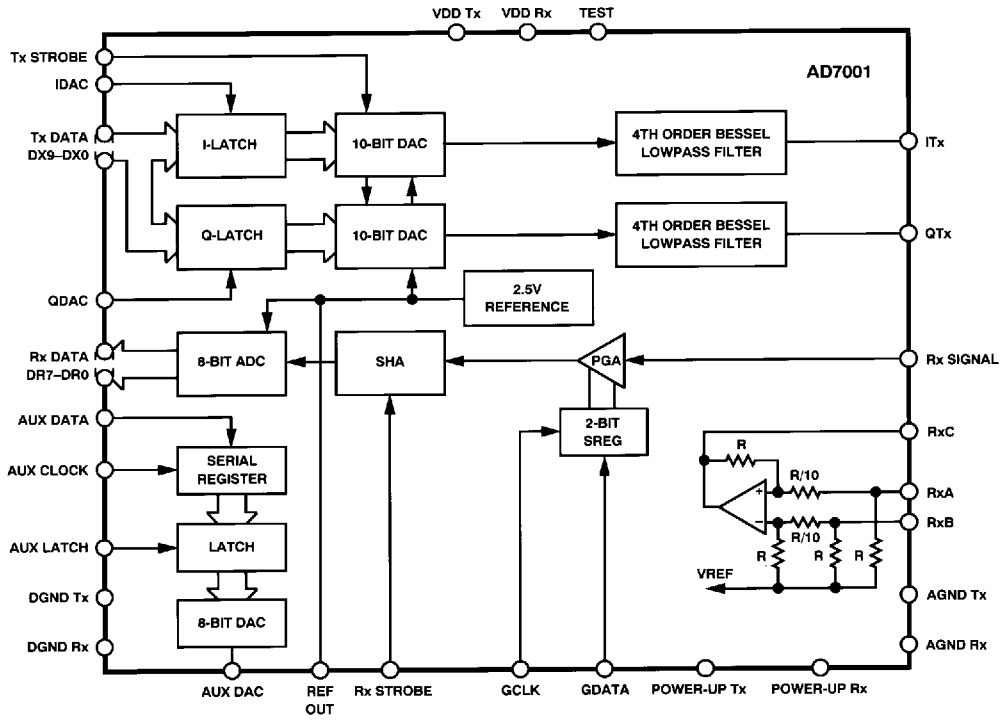
Besides providing two high accuracy 10-bit digital-to-analog converters in the transmit path and a single fast analog-to-digital converter in the receive path, the part also provides antialiasing filters and signal conditioning functions.

A single serial 8-bit DAC is included for such functions as AFC, AGC or carrier signal shaping in the IF/RF portion of the system.

All logic necessary for control of this device is contained on board. A fast data bus allows easy interface with all commonly available microprocessors.

As it is a necessity for all GSM mobile systems to use the lowest possible power, the device has power down options for both the transmit path and the receive path which are independent of each other. The AD7001 is housed in a space efficient 44-pin PQFP (Plastic Quad Flatpack).

FUNCTIONAL BLOCK DIAGRAM



REV. A

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AD7001—SPECIFICATIONS[1] (V_{DD} Tx = V_{DD} Rx = +5 V ± 7%; Test = AGNDTx = AGNDRx = DGNDTx = DGNDRx = 0 V; T_A = T_{MIN} to T_{MAX}, POWER-UP Tx = POWER-UP Rx = 0 V, unless otherwise noted)

Parameter	AD7001A	Units	Test Conditions/Comments
ADC SPECIFICATIONS			POWER-UP Rx = V_{DD}
Resolution	8	Bits	
Signal Input Range	V_{REF} ±V_{REF}/2	Volts	PGA = 1
	V_{REF} ±V_{REF}/4	Volts	PGA = 2
	V_{REF} ±V_{REF}/8	Volts	PGA = 4; All Biased on V_{REF}
Sampling Rate	2.17	MSPS	
DC Accuracy			
Integral Nonlinearity	±1.5	LSB max	PGA = 1, 2 or 4
Differential Nonlinearity	±1.5	LSB max	PGA = 1, 2 or 4
Offset Error			
T_{MIN} to T_{MAX}	±3	LSB max	PGA = 1
T_{MIN} to T_{MAX}	±5	LSB max	PGA = 2
T_{MIN} to T_{MAX}	±10	LSB max	PGA = 4
Full-Scale Error			Positive and Negative
$T_{MIN}$to T_{MAX}	±6	LSB max	PGA = 1
T_{MIN} to T_{MAX}	±8	LSB max	PGA = 2
T_{MIN} to T_{MAX}	±10	LSB max	PGA = 4
Input Resistance (DC)	5	kΩ min	
Input Capacitance	20	pF typ	
Dynamic Specifications			V_{IN} = 500 kHz Full-Scale Sine Wave,
Signal-to-Noise Ratio	40	dB min	f_{SAMPLE} = 2.16 MHz; PGA = 1, 2 or 4
Peak Spurious Noise	−40	dB max	PGA = 1, 2 or 4
Total Harmonic Distortion	−40	dB max	PGA = 1, 2 or 4
Gain Accuracy	±0.5	dB max	PGA = 1
	±0.75	dB max	PGA = 2
	±1.5	dB max	PGA = 4
Coding	Binary		
Power-Down Option	Yes		POWER-UP Rx = 0 V
DIFFERENCE AMPLIFIER SPECIFICATIONS			POWER-UP Rx = V_{DD}
Differential Gain	19.5	dB min	V_{IN} = 474 kHz ± 80 kHz; Biased on V_{REF}
	21.5	dB max	
Input Common-Mode Rejection Ratio	40	dB min	RxA = RxB = 0.4 V p-p @ 500 kHz
Distortion	−40	dB max	V_{OUT} = 1 V p-p @ 500 kHz; Biased on V_{REF}
Input Impedance			
RxA to REF OUT	20/60	kΩ min/max	40 kΩ Typical
RxB to REF OUT	10/40	kΩ min/max	25 kΩ Typical
RxA to RxB	3/10	kΩ min/max	6.5 kΩ Typical
Output Offset	±20	mV max	At RxC When Inputs Are Floating
Power-Down Option	Yes		POWER-UP Rx = 0 V
SIGNAL DAC SPECIFICATIONS			POWER-UP Rx = V_{DD}
Resolution	10	Bits	
Number of Channels	2		
Update Rate	2.17	MSPS	
DC Accuracy			
Integral Nonlinearity	±1	LSB typ	
Differential Nonlinearity	±1	LSB typ	
Output Signal Range	V_{REF} ±V_{REF}/2	Volts	Biased on V_{REF}; 10 kΩ/20 pF Load
Offset Error	±50	mV max	10 0000 0000 Loaded to DAC
Dynamic Specifications			
Gain Accuracy	±0.5	dB max	Measure at 66.65 kHz
ITx and QTx Gain Matching	±0.1	dB max	Generating 66.65 kHz Sine Waves
Differential Group Delay	200	ns max	Measured Relative to the Absolute Group Delay at 10 kHz in the Frequency Band 10 kHz–200 kHz
ITx and QTx Phase Matching	±1	° max	Measured at 66.65 kHz

Parameter	AD7001A	Units	Test Conditions/Comments
GMSK Spectrum Mask			Refer to Figure 1
100 kHz	+0.5	dB min	
200 kHz	−30	dB min	
250 kHz	−33	dB min	
400 kHz	−60	dB min	
600 kHz	−70	dB min	
1200 kHz	−70	dB min	
>4200 kHz	−60	dB min	
GMSK Phase Trajectory Error	0.7	° RMS typ	
	1.5	° Peak typ	
LP Filter Response			
300 kHz	−3	dB typ	
1 MHz	−20	dB typ	
2 MHz	−44	dB typ	
SNR + THD (0 MHz–1.08 MHz)			Producing 66.65 kHz Sine Wave with 2.17 MHz
T_{MIN} to T_{MAX}	52	dB min	Updated Rate
Peak Spurious Noise (0 MHz–6.5 MHz)	−70	dB typ	
Coding	Binary		
Power-Down Option	Yes		POWER-UP Tx = 0 V
AUXILIARY DAC SPECIFICATIONS			POWER-UP Tx = V_{DD}
Resolution	8	Bits	
DC Accuracy			
Integral Nonlinearity[2]	±2	LSB max	
Differential Nonlinearity[2]	±1	LSB max	Guaranteed Monotonic
Offset Error	1.25 ± 1	LSB max	
Full-Scale Error	±60	mV max	
Output Signal Range	0 to 2.5	Volts	
Output Impedance	2	kΩ max	I_{SINK} = 250 μA
	20	Ω typ	I_{SOURCE} = 250 μA
	850	Ω typ	I_{SINK} = 250 μA
Coding	Binary		
Power-Down Option	Yes		POWER-UP Tx = 0 V
REFERENCE SPECIFICATIONS			
V_{REF}, Reference Output	2.4/2.6	V min/V max	
Reference Variation[3]	25	mV max	
LOGIC INPUTS			
V_{INH}, Input High Voltage	V_{DD}–0.9	V min	
V_{INL}, Input Low Voltage	0.9	V max	
I_{INH}, Input Current	10	μA max	
C_{IN}, Input Capacitance	10	pF max	
LOGIC OUTPUTS			
V_{OH}, Output High Voltage	4.0	V min	$\|I_{OUT}\| \leq 200$ μA
V_{OL}, Output Low Voltage	0.4	V max	$\|I_{OUT}\| \leq 1.6$ mA
POWER SUPPLIES			
V_{DD}	4.65/5.35	V min/V max	
I_{DD}			
All Sections	62	mA max	
ADC and Diff Amp Active[4]	40	mA max	POWER-UP Tx = 0 V
Signal DACs and AUX DAC Active[5]	22	mA max	POWER-UP Rx = 0 V
All Sections Powered Down[6]	2.0	mA max	POWER-UP Tx = POWER-UP Rx = 0 V

NOTES

[1]Operating temperature ranges as follows: A Version; −25°C to +85°C.

[2]AUX DAC dc linearity is measured between codes 5 and 255, see terminology.

[3]Variation of the Reference between different POWER-UP Tx and POWER-UP Rx modes.

[4]Measured while the digital inputs to the transmit interface are static.

[5]Measured while the digital inputs to the receive interface are static.

[6]Measured while the digital inputs are equal to 0 V or V_{DD}.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

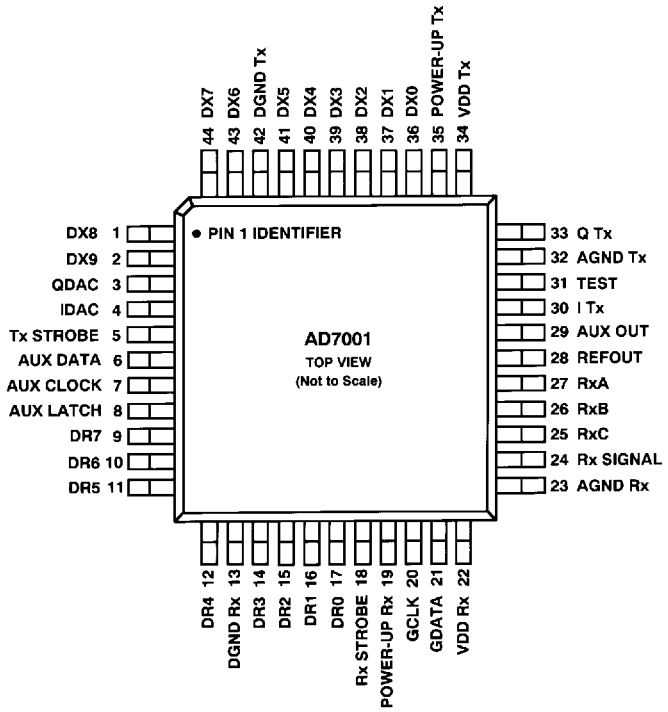
V_{DD} Tx, V_{DD} Rx to AGND . . . . . −0.3 V to +7 V
AGND to DGND . . . . . −0.3 V to +0.3 V
Digital I/O Voltage to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to AGND . . . . . −0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Industrial (A Version) . . . . . −25°C to +85°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Storage Temperature Range . . . . . −65°C to +150°C
Power Dissipation to +75°C . . . . . 450 mW
Derates Above +75°C by . . . . . 10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7001AS	−25°C to +85°C	Plastic Quad Flatpack	S-44

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although devices feature proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper precautions are recommended to avoid any performance degradation or loss of functionality.

Table I. Truth Table for I_{DD} Control

POWER-UP Tx	POWER-UP Rx	Operation	I_{DD} max
0	0	All Sections Powered Down	2 mA
0	1	Tx Section Powered Down, Rx Section Operational	40 mA
1	0	Tx Section Operational, Rx Section Powered Down	22 mA
1	1	All Sections Operational	62 mA

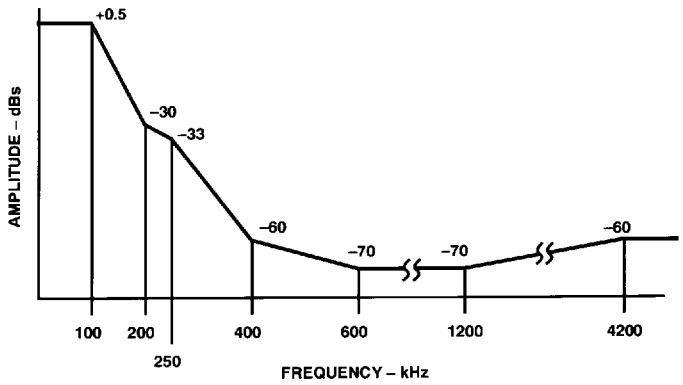


Figure 1. AD7001 Transmit GMSK Spectrum Mask

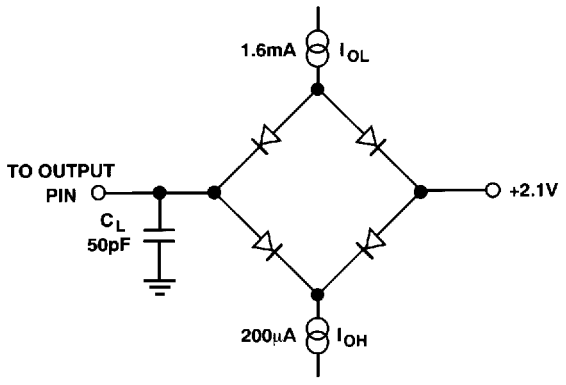


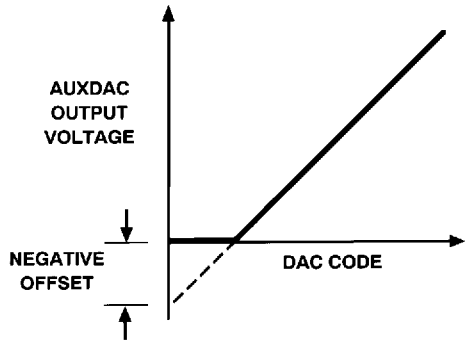
Figure 2. Load Circuit for Access Time Test

TERMINOLOGY

Signal Input Range
The input signal range for Rx SIGNAL is biased about V_{REF}. It can go $\pm V_{REF}/2$, $\pm V_{REF}/4$ or $\pm V_{REF}/8$ volts (depending on the PGA setting) about this point.

Auxiliary DAC Linearity
The AUX DAC output amplifier can have an internal negative offset, even though the part operates from a single (5 V) supply. However, because the negative rail is 0 V, the output cannot actually go below ground, resulting in the transfer function shown below. This "Knee" is an offset effect, not a linearity error, and the transfer function would have followed the dotted line if the output voltage could have gone negative.

Normally, linearity is measured between zero (all 0s) and full scale (all 1s) after offset and full scale have been adjusted out, but this is not possible with the AD7001 AUX DAC if the offset is negative. Instead, linearity of the AUX DAC is measured between full scale and the lowest code which is guaranteed to produce a positive output voltage. This code is calculated from the maximum specification for negative offset. For the AD7001 AUX DAC the linearity is measured between codes 5 and 255.



Effect of Negative Offset

Bias Offset Error
This is the offset error (in LSBs) in the DAC or ADC and is measured with respect to V_{REF}.

Signal-to-Noise Ratio
Signal-to-noise ratio (SNR) is the measured signal to noise at the output of the receive channel. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. SNR is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical SNR for a sine wave is given by:

$$SNR = (6.02\ N + 1.76)\ dB$$

Differential Group Delay
Absolute group delay is the rate of change of phase versus frequency, $d\phi/df$. For the AD7001, differential group delay is the absolute group delay in a specified band relative to the absolute group delay at 10 kHz. The specified band for the AD7001 is 10 kHz–200 kHz.

Group Delay Between Channels
This is the difference between the group delay of the I and Q channels and is a measure of the phase matching characteristics of the two.

Output Signal Span
This is the output signal range for the transmit channel section and the auxiliary DAC section. For the transmit channel the span is ± 1.25 volts centered on V_{REF} and for the auxiliary DAC section it is 0 to $+V_{REF}$.

Output Signal Full-Scale Accuracy
This is the accuracy of the full scale output (all 1s loaded to the DACs) on the transmit channel and is expressed in dBs.

DAC Offset Error
This is the amount of offset in the transmit DACs and the auxiliary DACs and is expressed in mVs for the transmit section and in LSBs for the auxiliary section.

AUXDAC Full-Scale Error
This is a measure of the output error between an ideal full-scale output of 2.5 V and the measured output when all 1s are loaded.

Output Impedance
This is a measure of the drive capability of the auxiliary DAC output and is expressed in kΩs.

GMSK Spectrum Mask
This is the output spectrum of the I and Q transmit channels when transmitting a random sequence of data bits using GMSK modulation, as specified in the GSM standard, using a bit truncation of ± 6 bit periods.

GMSK Phase Trajectory Error
This is a measure of the phase error between the transmitted phase of an ideal GMSK modulator and the actual phase transmitted by the AD7001, when transmitting a random sequence of data bits. It is specified as a peak phase error and also as a rms phase error.

ADC TIMING (V_{DD} Tx = V_{DD} Rx = +5 V ± 7%; Test = AGND Tx = AGND Rx = DGND Tx = DGND Rx = 0 V; unless otherwise noted)

Parameter	Limit at T_A = −25°C to +85°C	Units	Description
t_1	100	μs min	POWER-UP Rx to Rx STROBE Setup Time
t_2	t_3 +100	ns min	Rx STROBE to New Rx DATA
	t_3 +220	ns max	
t_3	460	ns min	Rx STROBE Period
t_4	200	ns min	Rx STROBE High Period
t_5	200	ns min	Rx STROBE Low Period
t_6	0	ns min	POWER-UP Rx Going Low to Rx DATA 3-State
	40	ns max	

NOTES
[1]All input signals are specified with tr= tf= 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figure 2.
[3]t_2 is measured with the load circuit of Figure 1 and is defined as the time required for an output to cross 0.8 V or 2.4 V.
[4]t_6 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_6, quoted in the timing characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

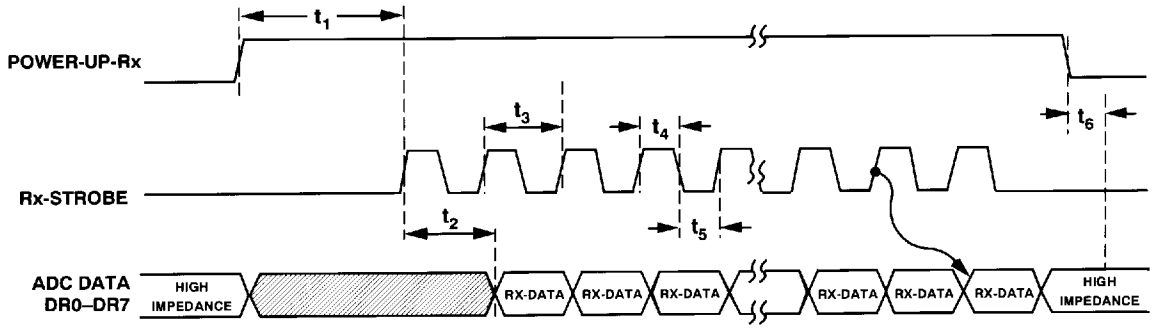


Figure 3. ADC Timing Diagram

PGA TIMING (V_{DD} Tx = V_{DD} Rx = +5 V ± 7%; Test = AGND Tx = AGND Rx = DGND Tx = DGND Rx = 0 V; unless otherwise noted)

Parameter	Limit at T_A = +25°C	Limit at T_A = −25°C to +85°C	Units	Description
t_7	150	150	ns min	GCLK Period
t_8	75	75	ns min	GCLK Low Period
t_9	75	75	ns min	GCLK High Period
t_{10}	40	40	ns min	GDATA to GCLK Setup Time
t_{11}	50	50	ns min	GDATA to GCLK Hold Time

NOTES
[1]All input signal rise and fall times measured from 10% to 90% of +5 V; tr = tf = 10 ns.
[2]Timing measurement reference level is $(V_{IH} + V_{IL})/2$.

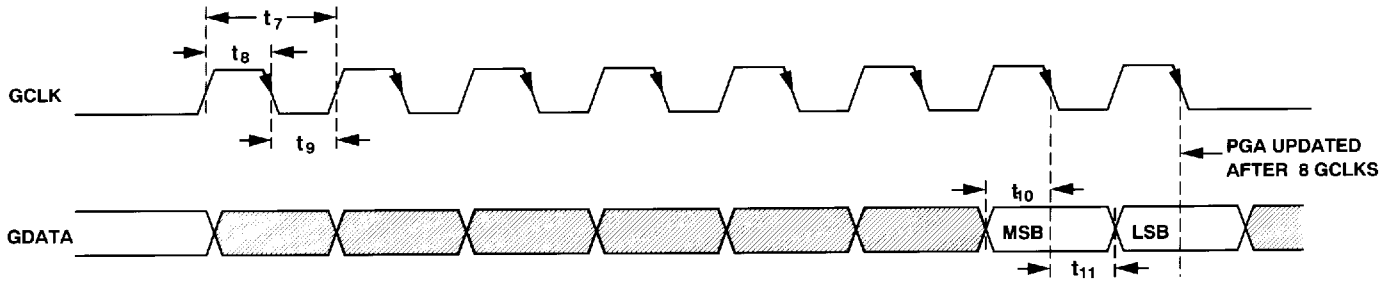


Figure 4. PGA Timing Diagram

SIGNAL DAC TIMING (V_{DD} Tx = V_{DD} Rx = +5 V ± 7%; Test = AGND Tx = AGND Rx = DGND Tx = DGND Rx = 0V; unless otherwise noted)

Parameter	Limit at T_A = −25°C to +85°C	Units	Description
t_{12}	100	µs min	POWER-UP Tx to Tx STROBE Setup Time.
t_{13}	100	ns min	IDAC, QDAC Pulse Width
t_{14}	40	ns min	Tx DATA Setup Time
t_{15}	10	ns min	Tx DATA Hold Time
t_{16}	50	ns min	IDAC to Tx STROBE Setup Time
t_{17}	50	ns min	QDAC to Tx STROBE Setup Time
t_{18}	100	ns min	Tx STROBE Pulse Width
t_{19}	400	ns min	Tx STROBE Period

NOTES
[1]All input signal rise and fall times measured from 10% to 90% of +5 V; tr = tf = 20 ns.
[2]Timing measurement reference level is $(V_{IH} + V_{IL})/2$.

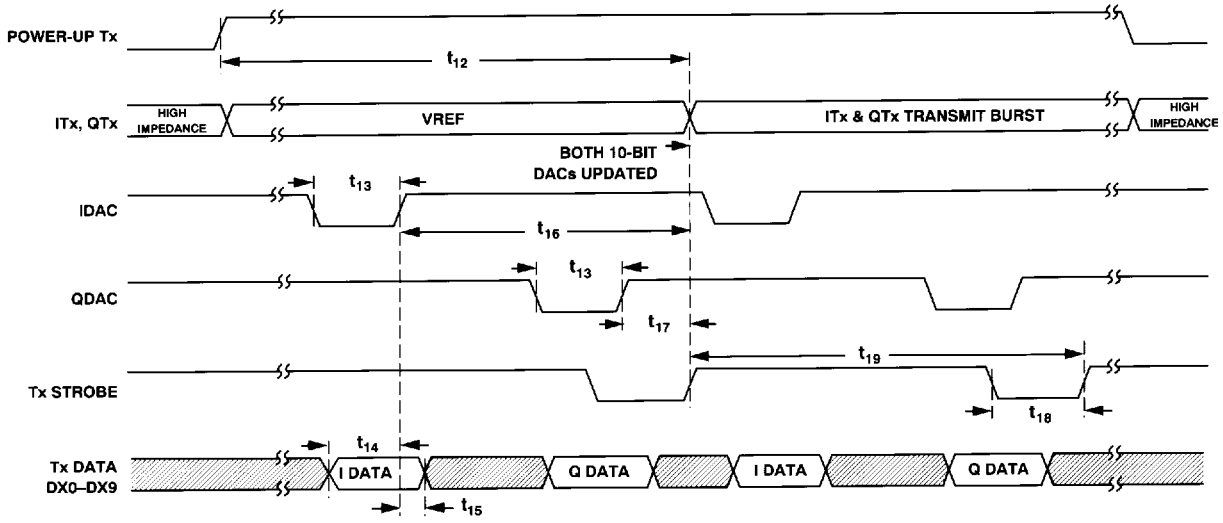


Figure 5. Signal DAC Timing Diagram

AUXILIARY DAC TIMING (V_{DD} Tx = V_{DD} Rx = +5 V ± 7%; Test = AGND Tx = AGND Rx = DGND Tx = DGND Rx = 0 V; unless otherwise noted)

Parameter	Limit at T_A = −25°C to +85°C	Units	Description
t_{20}	75	ns min	AUX CLOCK Low Duration
t_{21}	75	ns min	AUX CLOCK High Duration
t_{22}	40	ns min	AUX DATA to AUX CLOCK Setup Time
t_{23}	50	ns min	AUX DATA to AUX CLOCK Hold Time
t_{24}	50	ns min	AUX LATCH to AUX CLOCK Setup Time
t_{25}	40	ns min	AUX LATCH to AUX CLOCK Hold Time
t_{26}	8 (t_{20} + t_{21})	ns min	AUX LATCH Duration

NOTES
[1]All input signal rise and fall times measured from 10% to 90% of +5 V; tr = tf = 20 ns.
[2]Timing measurement reference level is (V_{IH} + V_{IL})/2.

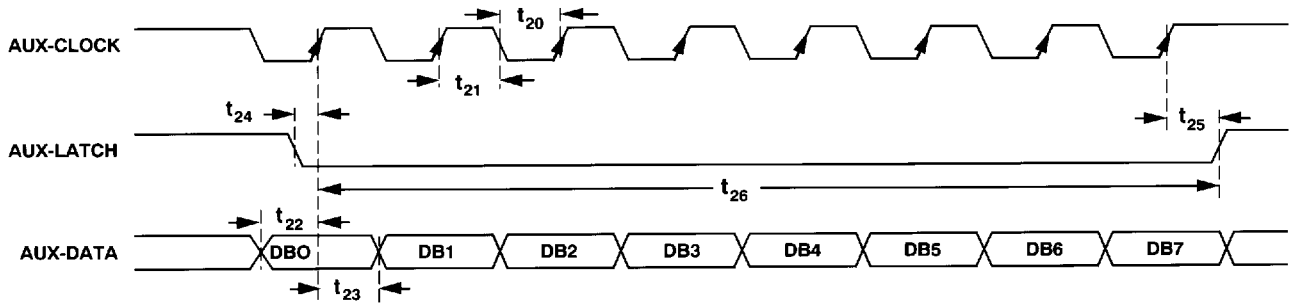


Figure 6. Auxiliary DAC Timing Diagram

TRANSMIT SECTION

The transmit section of the AD7001 performs the baseband conversion of I and Q (In-phase and Quadrature) waveforms for the GSM Pan-European Digital Cellular Communications system. The transmit channel consists of two 10-bit DACs, followed by 4th order Bessel reconstruction filters. Also included in the transmit channel is a single 8-bit auxiliary DAC.

Transmit DACs

The 10-bit DACs can be used to perform the conversion of I and Q waveforms when implementing GMSK modulation in accordance with the GSM 5.04 standard.

Reconstruction Filters

The reconstruction filters smooth the DAC output signals, providing continuous time I and Q waveforms at the output pins. These are 4th order Bessel low-pass filters with a cutoff frequency of approximately 300 kHz. Figure 7 shows a typical transmit filter frequency response, while Figure 8 shows a typical plot of group delay versus frequency. The filters are designed to have a linear phase response in the passband and due to the reconstruction filters being on-chip, the phase mismatch between the I and Q transmit channels is kept to a minimum.

Transmit DACs Digital Interface

The 10-bit DACs are double buffered, allowing the DACs to be simultaneously updated via a single 10-bit data bus (DX0–DX9). Figure 5 illustrates the Timing interface for the I and Q DACs. The I and Q latches are loaded on the rising edges of IDAC and QDAC, respectively, with data on the DX0–DX9 databus. When both latches have been updated, Tx STROBE is then used to transfer the contents of both I and Q Latches to the 10-bit DACs.

The transmit DACs are put into sleep mode (drawing minimum current) by bringing POWER-UP Tx low. During sleep mode the I Tx and Q Tx outputs go into high impedance. On POWER-UP Tx going high, the I and Q DACs are reset to V_{REF}, which prevents any imbalance between the I and Q channels when the I Tx and Q Tx outputs are ac coupled to the IF/RF modulator. Allow time for the transmit section to fully power-up before updating the I and Q latches. Figure 9 shows a typical GSM transmission burst.

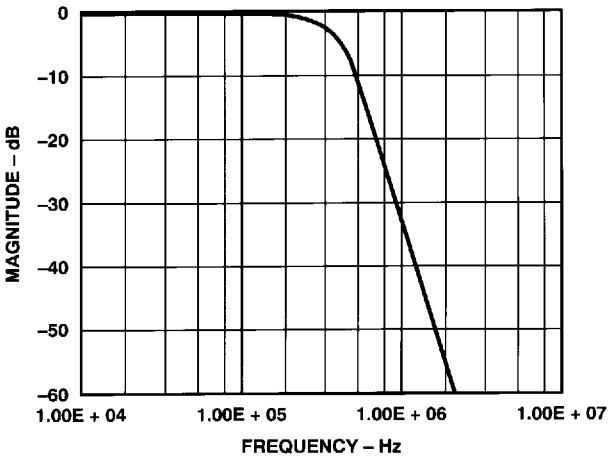


Figure 7. Transmit Filter Frequency Response

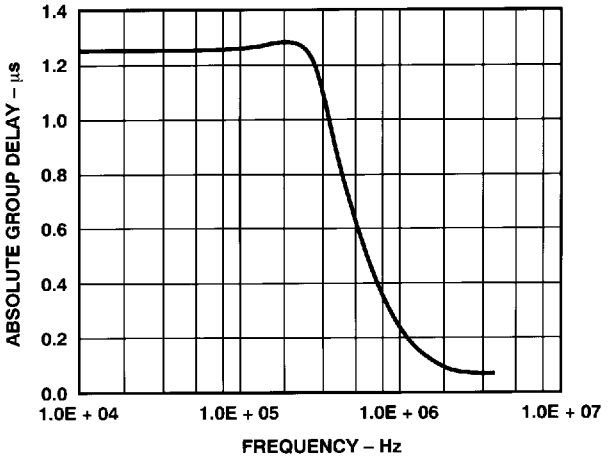


Figure 8. Transmit Filter Group Delay

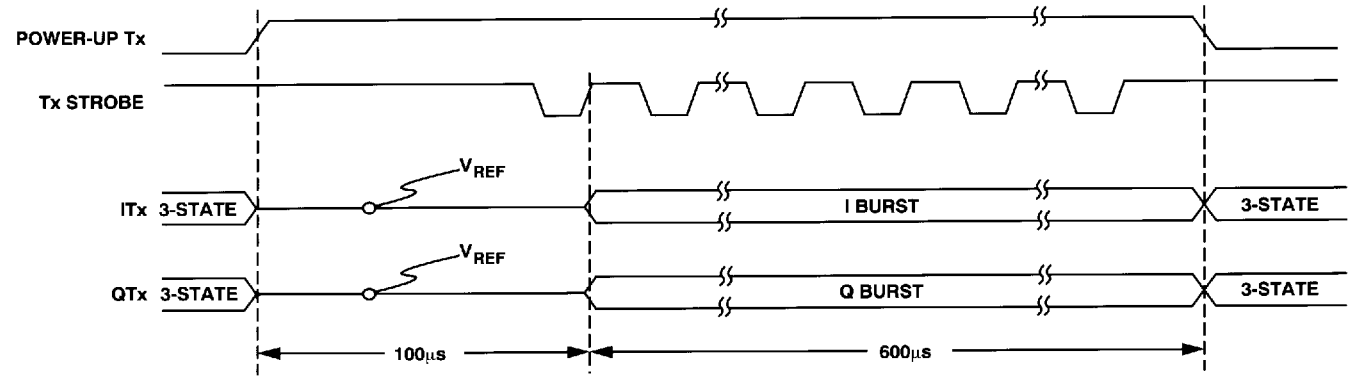


Figure 9. Typical GSM Transmission Burst

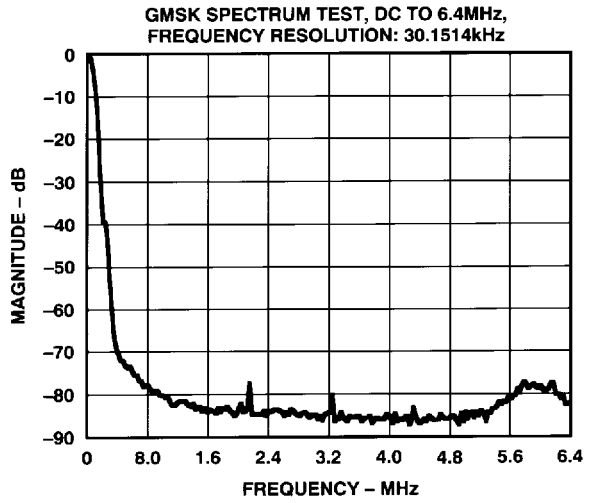


Figure 10. Transmit GMSK Composite Spectrum (0–6.4 MHz)

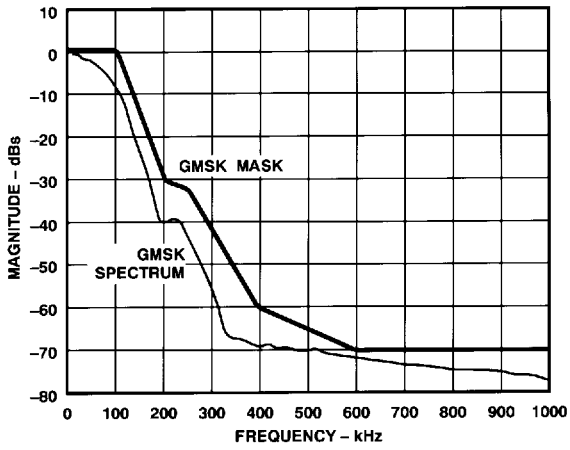


Figure 11. Transmit GMSK Composite Spectrum (0–1 MHz)

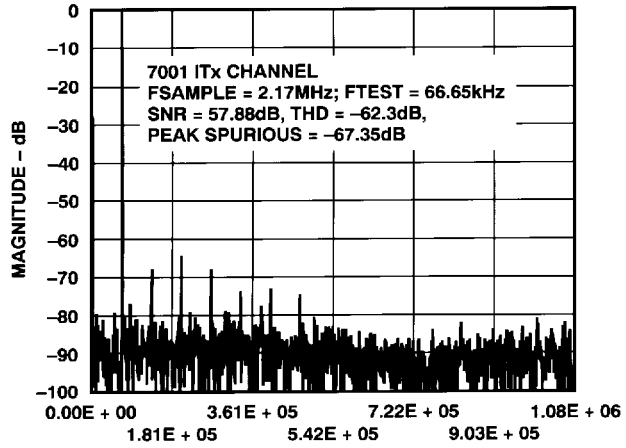


Figure 12. Frequency Plot of the I Channel Generating a Sine Wave at 66.65 kHz

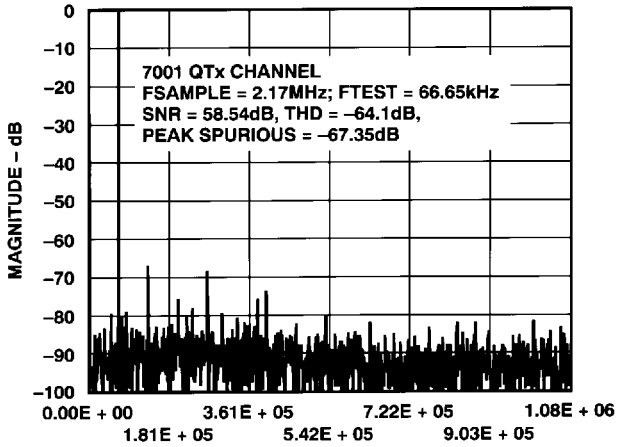


Figure 13. Frequency Plot of the Q Channel Generating a Sine Wave at 66.65 kHz

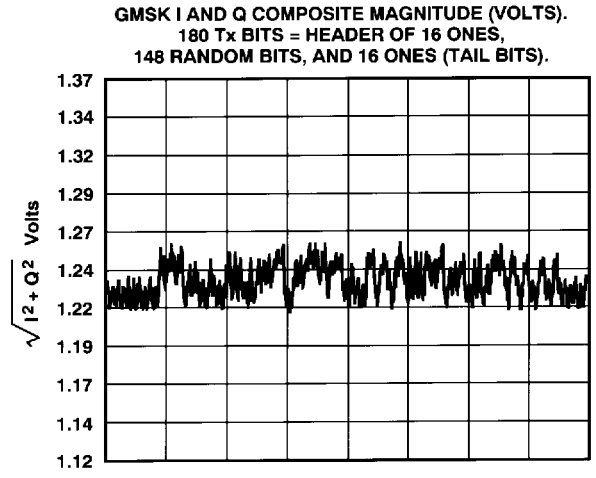


Figure 14. Typical Plot of the GMSK I and Q Composite Magnitude Generated Using the I and Q Transmit Channels

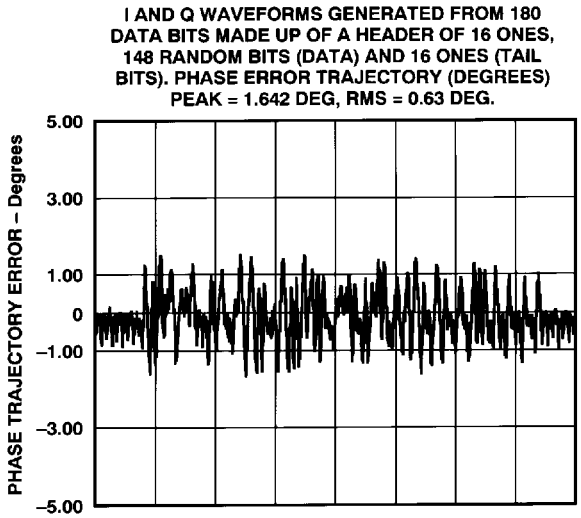


Figure 15. Typical Plot of the GMSK Phase Error Trajectory Generated Using the AD7001 I and Q Transmit Channels

Auxiliary DAC

An 8-bit auxiliary serial DAC is also provided for such functions as Automatic Gain Control or for ramping up/down the transmit power amplifiers during the beginning/end of a transmit burst. Interfacing to the auxiliary section is accomplished via a serial interface.

The AD7001 auxiliary DAC is a voltage mode DAC, consisting of R–2R ladder network, constructed from highly stable thin-films resisters and high speed single pole, double throw switches.

The output of the voltage mode auxiliary DAC is buffered by a noninverting CMOS amplifier with a gain of two. This scales the output of the R–2R network from a voltage range of 0 – $V_{REF}/2$ to a voltage range of 0–V_{REF}. Due to the single supply operation of the buffer it has limited sink capability near ground.

AUX DAC Digital Interface

The serial interface timing is illustrated in Figure 6. The serial interface is controlled using AUX CLOCK, AUX LATCH and AUX DATA. AUX LATCH must go low prior to the clocking of new serial data, this prevents the AUX DAC output from being corrupted while new serial data is being loaded. The AUX CLOCK must be a gated clock; i.e., it must only be active when loading the auxiliary DAC. AUX DATA is latched on the rising edge of AUX CLOCK. When eight data bits have loaded, where DB0 is the LSB and DB7 is the MSB, AUX LATCH is brought high to update the AUX DAC output.

The auxiliary DAC is also put into sleep mode by bringing POWER-UP Tx low. During sleep mode the AUX DAC output is put into high impedance. The auxiliary DAC does not lose its contents while in sleep mode and will power-up to its previous value and settle within 100 μs. The auxiliary DAC can also be loaded with new data while in sleep mode thereby allowing the AUX DAC output to power-up to a different value. However, while exercising the serial interface during sleep mode, the sleep current will increase.

RECEIVE SECTION

The receive channel consists of a low power, two stage flash 8-bit analog to digital converter (ADC) combined with an on-chip sample and hold amplifier (SHA) and a PGA. The PGA provides programmable gains settings of 1, 2 or 4. Also included in the receive path is a differential amplifier.

Differential Amplifier

The differential amplifier provides a means for amplifying the IF receive signal before being digitized. The differential inputs can configured either for single-ended or for differential-ended operation. The RxC output can be directly connected to the Rx SIGNAL pin. For optimum performance the inputs (RxA and RxB) should be ac coupled, as this ensures proper internal biasing around V_{REF}. The output (RxC) of the differential amplifier is given as:

$$RxC = 10\ (RxB–RxA) + V_{REF}$$

POWER-UP Rx is used to put the differential amplifier into sleep mode. Figure 16 illustrates the operation of the differential amplifier under the control of POWER-UP Rx and Rx STROBE. While the receive section is in sleep mode (POWER-UP Rx low), the differential inputs (RxA and RxB) are open circuit. On POWER-UP Rx going high, the differential inputs are then connected to V_{REF} through a nominal impedance of 300 Ω. The inputs are connected for normal operation after two Rx STROBE cycles, i.e., on the third rising edge of Rx STROBE. If RXC is directly connected to Rx SIGNAL, then the first two ADC conversions, after POWER-UP RX going high, can be used to measure the combined offset of both the differential amplifier and the ADC channel.

PGA

The PGA allows Rx SIGNAL to be amplitude by a factor 1, 2 or 4 depending on the value loaded into the 2-bit PGA register. When power is applied to the part, the 2-bit PGA register will be uninitialized and, therefore, must be initialized as described in the following section.

PGA Digital Interface

The receive channel PGA is programmed via a two pin serial interface (GCLK and GDATA). Figure 4 illustrates the serial interface timing diagram for the PGA. GDATA is latched on the falling edge of GCLK. GCLK must be a gated clock, active only when updating the PGA. Eight clock cycles are required to update the PGA setting, where the first six cycles are dummy cycles and only the last two clock cycles load new data into the 2-bit PGA register. These last two data bits are loaded MSB first. On the last falling edge of GCLK the PGA is set to a gain of 1, 2 or 4, depending on the 2-bit value contain in the PGA register. Table II illustrates the truth table for the PGA setting.

Table II. PGA Truth Table

MSB	LSB	PGA Gain
0	0	1
0	1	2
1	0	2
1	1	4

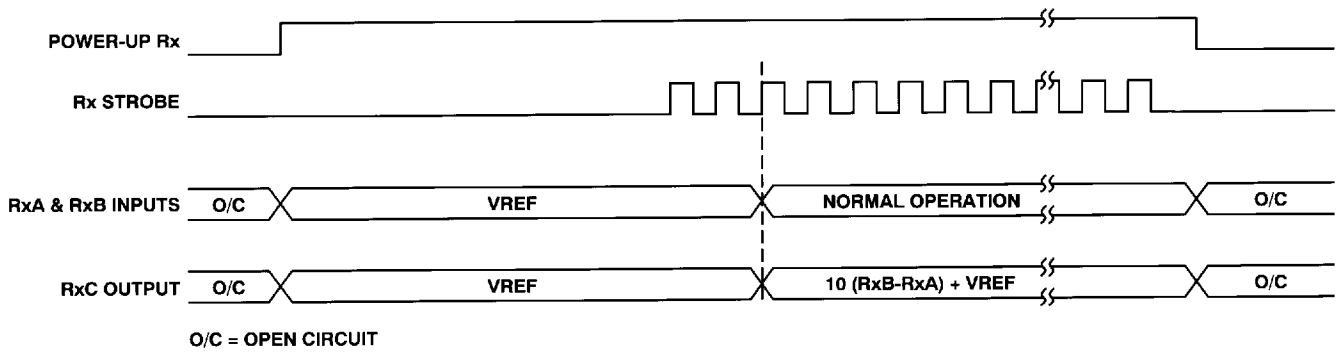


Figure 16. Operation of the Differential Amplifier

On initial power being applied to the part, the PGA serial logic will be in an undetermined state; however, each time the receive section is brought out of sleep mode (POWER-UP Rx brought high) the serial logic is reset. In order to correctly initialize the 2-bit PGA register, one must first reset the serial logic after power has initially been applied to the part. The PGA can be updated at any time, except when the serial logic is being reset. Hence, one should not attempt to update the PGA register immediately before or after POWER-UP Rx goes high. A guard band of 150 ns before and 300 ns after POWER-UP Rx going high is sufficient for correct operation.

SHA and ADC

The 8-bit flash pipelined ADC combined with the on-board Sample and Hold Amplifier (SHA) generates 8-bit samples up to a data rate of 2.17 MHz.

ADC Digital Interface

Figure 3 illustrates the receive timing interface, control of the receive interface is effected through the use of the POWER-UP RX and Rx-STROBE pins with the receive data available on a parallel interface (DR0–DR7). Conversions are initiated on the rising edge of Rx-STROBE and the DR0–DR7 pins are updated on the following rising edge of Rx-STROBE, after approximately 130 ns. On POWER-UP RX going high time (t_1) must be provided to allow the receive circuity to become fully powered up. Rx-STROBE can now be activated to initiate ADC conversions.

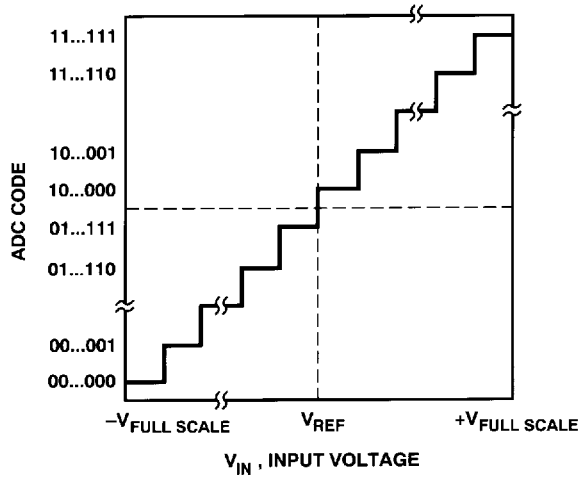


Figure 17. ADC Transfer Function

As described earlier, if the differential amplifier is connected to Rx SIGNAL, the first two conversions can be used to measure the offset contained in the receive path. The user can average the first two conversions to obtain an offset value which can subtracted, by the user, from subsequent ADC conversions. Although the ADC will continue to convert, time must be allowed for the differential amplifier to settle due to the internal switching from V_{REF} to the RX A and RX B input pins.

VOLTAGE REFERENCE

The AD7001 contains an on-chip bandgap reference which provides a low noise, temperature compensated reference to the I/Q transmit DACs and the I/Q receive ADC. The Reference is also make available on the REFOUT pin and can be used to bias other analog circuit in the in the IF section.

A decoupling scheme as illustrated in Figure 18 should be used to decouple the reference for correct operation. If the reference is required to bias external circuitry, then this should be connected after the 100 Ω series resistance.

When both the transmit section and the receive section are in sleep mode (POWER-UP TX and POWER-UP RX low), the reference output buffer is also powered down by approximately 80%.

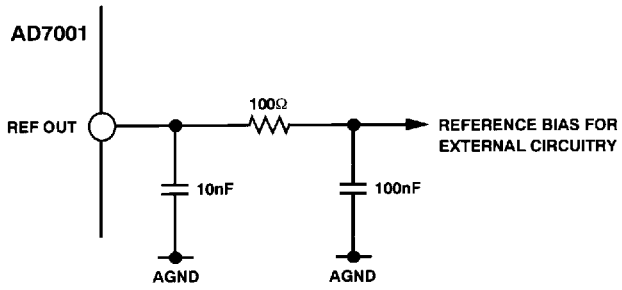


Figure 18. Reference Decoupling for the REF OUT Pin

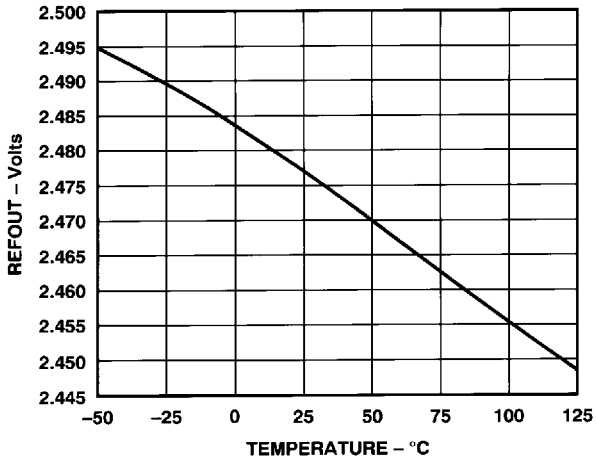


Figure 19. Typical Plot of Reference Variation vs. Temperature

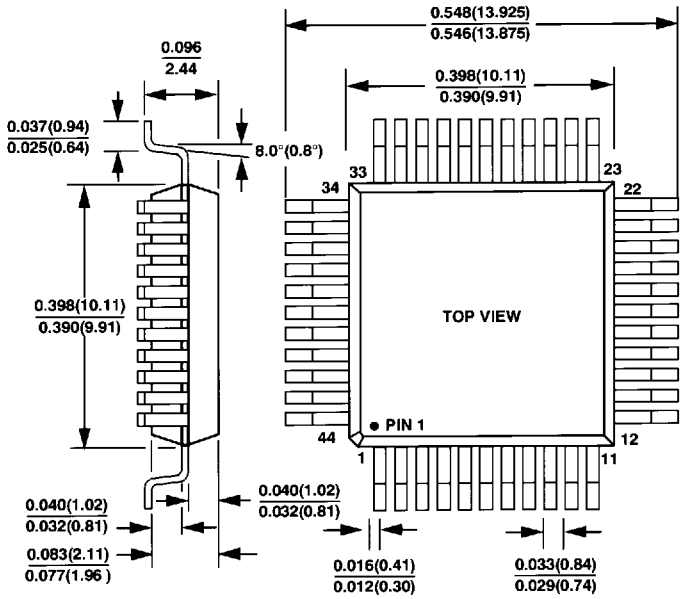
PIN FUNCTION DESCRIPTION

PQFP Pin Number	Mnemonic	Function
POWER SUPPLY		
34	V_{DD} Tx	Positive Power Supply for transmit section.
22	V_{DD} Rx	Positive Power Supply for receive section. Both V_{DD} pins must be tied together.
32	AGND Tx	Analog Ground for transmit section.
23	AGND Rx	Analog Ground for receive section. Both AGND pins must be tied together.
42	DGND Tx	Digital Ground for transmit section.
13	DGND Rx	Digital Ground for receive section. Both DGND pins must be tied together.
ANALOG SIGNAL AND REFERENCE		
28	REF OUT	Reference Output, this is 2.5 V nominal.
24	Rx SIGNAL	Analog Input for receive channel.
30	I Tx	Analog Output Voltage from the I transmit channel. This output comes from a 10-bit DAC and is filtered by a 4th order Bessel low-pass filter.
33	Q Tx	Analog Output Voltage from the Q Transmit channel. This output comes from a 10-bit DAC and is filtered by a 4th order Bessel low-pass filter.
29	AUX DAC	Analog Output Voltage from the 8-bit Auxiliary DAC. This output comes from a buffer amplifier.
27	RxA	Analog Input for the inverting input of the differential amplifier.
26	RxB	Analog Input for the noninverting input of the differential amplifier.
25	RxC	Analog Output Voltage from the differential amplifier.
TRANSMIT INTERFACE AND CONTROL		
5	Tx STROBE	Transmit Strobe, Digital Input. Tx STROBE transfers the contents of both the I and Q Latches, on a rising edge, to the I and Q 10-bit DACs, respectively. This is used to update both 10-bit DACs simultaneously after the I and Q latches have been loaded via a single 10-bit port.
4	I DAC	I Latch Update, Digital Input. I DAC is used to update the I latch via DX9–DX0. This is an edge triggered latch, DX9–DX0 are latched on the rising edge of I DAC.
3	Q DAC	Q Latch Update, Digital Input. Q DAC is used to update the Q latch via DX9–DX0. This is an edge triggered latch, DX9–DX0 are latched on the rising edge of Q DAC.
2,1	DX9, DX8	Transmit Data Bit 9 and Data Bit 8, digital inputs. DX9 is the most significant bit (MSB).
44, 43	DX7, DX6	Transmit Data Bit 7 and Data Bit 6, digital inputs.
41–36	DX5–DX0	Transmit Data Bits 5 to 0, digital inputs. DX0 is the least significant bit (LSB).
7	AUX CLOCK	Auxiliary Clock, edge triggered digital input. Serial data bits are latched on the rising edge AUX CLOCK when AUX LATCH is low. AUX CLOCK must be a gated clock, which is only active when data is being loaded into the serial register
6	AUX DATA	Auxiliary Data, digital input. This data input is used in conjunction with AUX CLOCK and AUX LATCH to load the 8-bit Auxiliary DAC register.
8	AUX LATCH	Level triggered Digital Input. AUX LATCH controls the transfer of data between the AUX DAC serial register and the AUX DAC latch. When high, the AUX DAC latch is transparent. Data is latched when AUX LATCH is brought low.
35	POWER-UP Tx	Power-Up Transmit, Digital Input. When this goes low the transmit section goes into standby mode, drawing minimum current.
RECEIVE INTERFACE AND CONTROL		
18	Rx STROBE	Receive Strobe, Digital Input. Rx STROBE initiates an ADC conversion, at the end of which DR7–DR0 are updated.
9–12	DR7–DR4	Receive Data Bits 7 to 4, Digital Outputs. DR7 is the most significant bit (MSB).
14–17	DR3–DR0	Receive Data Bits 3 to 0, Digital Outputs. DR0 is the least significant bit (LSB).
20	GCLK	PGA Clock, Digital Input. GDATA bits are latched on the falling edge of GCLK. The PGA must be loaded using 8 GCLKs, the last two bits that are loaded are used to set the PGA.
21	GDATA	Programmable Gain Data, Digital Input. This input is used in conjunction with GCLK to set the gain for the PGA.
19	POWER-UP Rx	Power-Up Receive, Digital Input. When this goes low the receive section goes into standby mode, drawing minimal current.
31	TEST	Test mode, Digital Input. This pin is used to put the device into a special factory test mode. For normal device operation this pin must be tied to DGND.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Plastic Quad Flatpack (S) Package (S-44)



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