

**4-BIT SINGLE-CHIP MICROCONTROLLER WITH ONE-TIME PROM AND
 HARDWARE FOR DIGITAL TUNING SYSTEM**
DESCRIPTION

μ PD17P005 is a model of μ PD17005 equipped with one-time PROM instead of a mask ROM.

Since the user program can be written to the PROM of the μ PD17P005, this 4-bit microcontroller is ideal for experimental or small-scale production of application systems using μ PD17005 or μ PD17003A (a model of μ PD17005 with reduced ROM and RAM).

Also refer to the Data Sheets of the μ PD17005 and μ PD17003A.

The electrical characteristics (such as the supply current) of the μ PD17P005 and the analog characteristics of the PLL are different from those of the μ PD17005. Therefore, take these differences into consideration when designing and producing the application systems.

FEATURES

- Compatible with μ PD17005 and 17003A
- Internal one-time PROM: 7932 x 16 bits
- Operating voltage range: 5 V \pm 10%
- I²C bus (μ PD17P005GF-E00-3B9)
- QTOPTM microcontroller model available (μ PD17P005GF-xxx-3B9)

ORDERING INFORMATION

PART NUMBER	PACKAGE	QUALITY GRADE
μ PD17P005GF-3B9	80-pin plastic QFP (14 x 20 mm)	Standard
μ PD17P005GF-E00-3B9*1	80-pin plastic QFP (14 x 20 mm)	Standard
μ PD17P005GF-xxx-3B9*2	80-pin plastic QFP (14 x 20 mm)	Standard

* 1: I²C bus model

* 2: QTOP microcontroller model

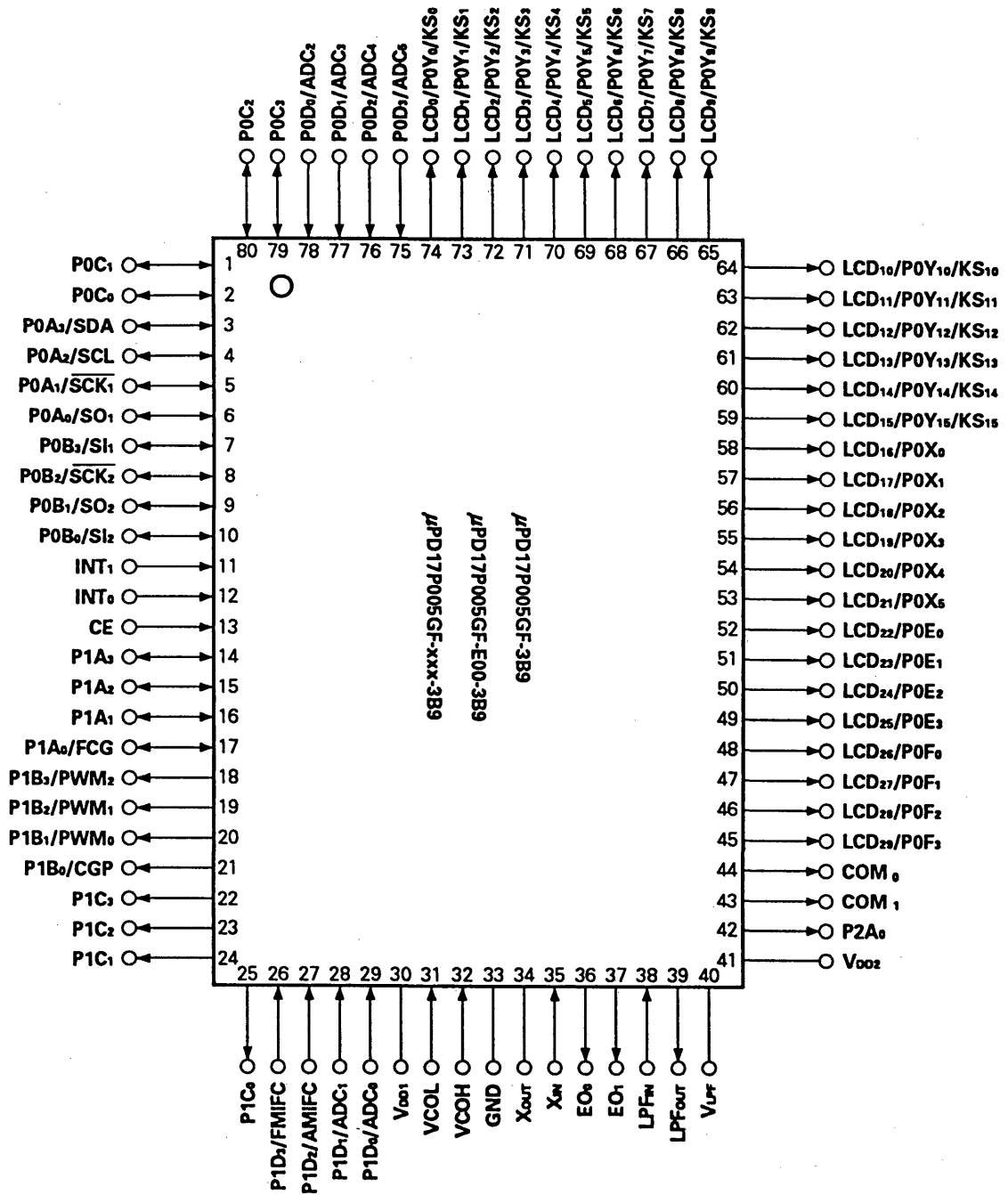
Remarks: QTOP microcontroller is the generic name of a single-chip microcontroller with a one-time PROM that is programmed, stamped, screened, and verified by NEC.

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grades on the devices and their recommended applications.

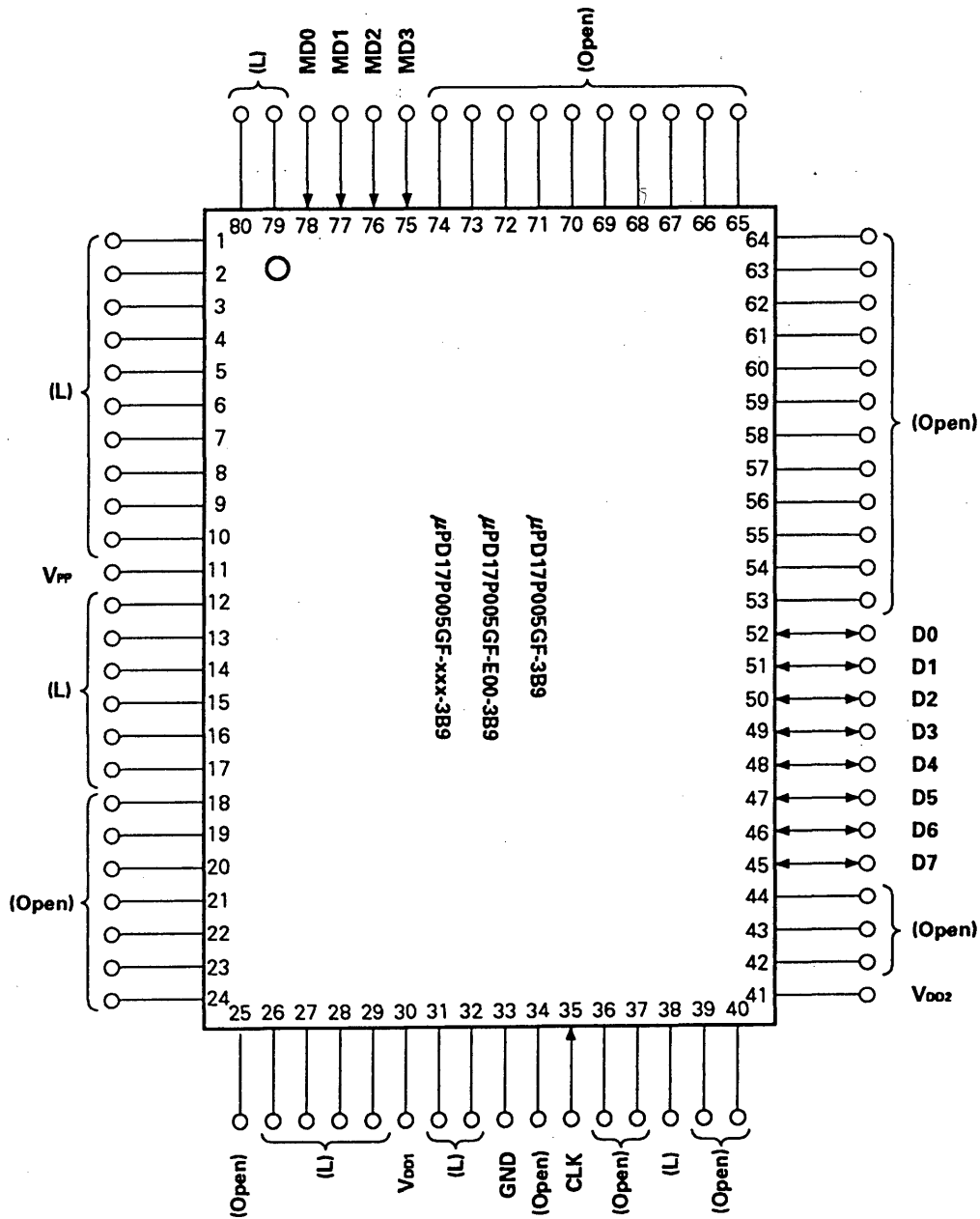
The information in this document is subject to change without notice.

PIN CONFIGURATION (Top View)

(1) In normal operation mode



(2) In PROM programming mode



Note: () indicates the processing of the pins not used in the PROM programming mode.
 L :Ground these pins through an individual resistor (470Ω)
 Open :Do not connect anything to these pins.

PIN NAME

ADC ₀ -ADC ₅	: A/D converter input	P0E ₀ -P0E ₃	: Port 0E
AMIFC	: Frequency counter input	P0F ₀ -P0F ₃	: Port 0F
CE	: Chip enable input	P0X ₀ -P0X ₃	: Port 0X
CGP	: Clock generator port	P0Y ₀ -P0Y ₃	: Port 0Y
COM ₀ , COM ₁	: LCD common signal output	P1A ₀ -P1A ₃	: Port 1A
CLK	: PROM address updating clock input	P1B ₀ -P1B ₃	: Port 1B
D0-D7	: PROM data I/O	P1C ₀ -P1C ₃	: Port 1C
EO ₀ , EO ₁	: Error out output	P1D ₀ -P1D ₃	: Port 1D
FCG	: External gate counter input	P2A ₀	: Port 2A
FMIFC	: Frequency counter input	PWM ₀ -PWM ₂	: D/A converter output
GND	: Ground	SCK ₁ , SCK ₂	: Serial clock I/O
INT ₀ , INT ₁	: External interrupt input	SCL	: Serial clock I/O
KS ₀ -KS ₁₅	: Key source signal output	SDA	: Serial data I/O
LCD ₀ -LCD ₂₉	: LCD segment signal output	Sl ₁ , Sl ₂	: Serial data input
LPF _{IN}	: LPF amplifier input	SO ₁ , SO ₂	: Serial data output
LPF _{OUT}	: LPF amplifier output	VCOH	: Local oscillator input, high
MD0-MD3	: Operation mode select	VCOL	: Local oscillator input, low
P0A ₀ -P0A ₃	: Port 0A	VDD ₁ , VDD ₂	: Positive power supply
P0B ₀ -P0B ₃	: Port 0B	V _L PF	: LPF amplifier power source
P0C ₀ -P0C ₃	: Port 0C	V _{PP}	: PROM write power source
P0D ₀ -P0D ₃	: Port 0D	X _{IN} , X _{OUT}	: Main clock oscillator

BLOCK DIAGRAM

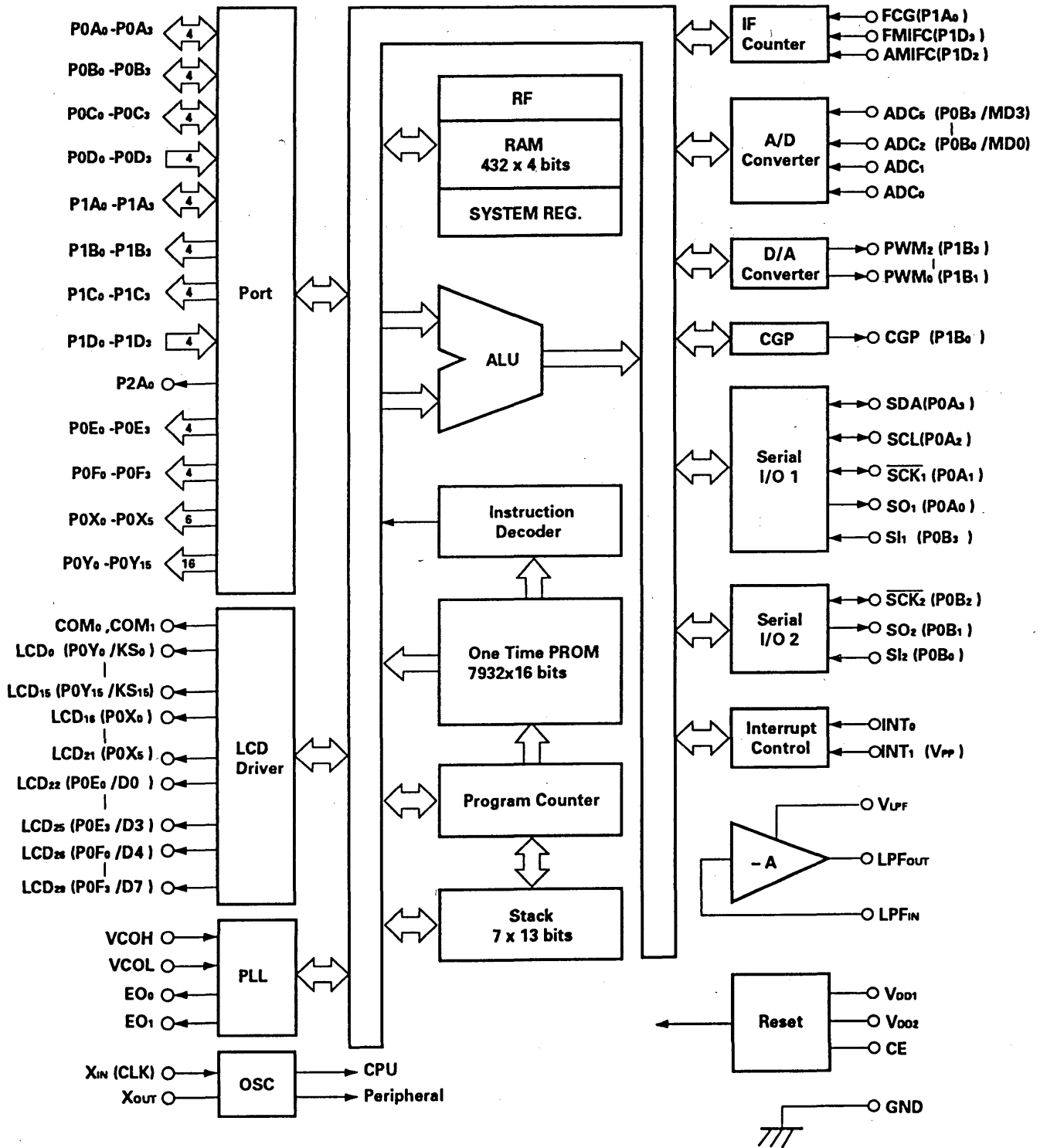


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1. PIN FUNCTIONS

1.1 NORMAL OPERATION MODE

PIN NO.	SYMBOL	FUNCTION	OUTPUT FORM	WHEN POWER-ON RESET
79 80 1 2	P0C3 P0C2 P0C1 P0C0	4-bit I/O port. Can be set in input or output mode in 4-bit units	CMOS push-pull	Input
3 4 5 6 7 8 9 10	P0A3/SDA P0A2/SCL P0A1/SCK1 P0A0/SO1 P0B3/SI1 P0B2/SCK2 P0B1/SO2 P0B0/SI2	I/O lines of port 0A, port 0B, and serial interface. <ul style="list-style-type: none"> • P0A3-P0A0 • 4-bit I/O port • Can be set in input or output mode in 1-bit units. • P0B3-P0B0 • 4-bit CMOS I/O port • Can be set in input or output mode in 1-bit units. • SDA, SCL • SDA: Serial data I/O • SCL: Serial clock I/O • SCK1, SO1, SI1 • SCK1: Serial clock I/O • SO1: Serial data output • SI1: Serial data input • SCK2, SO2, SI2 • SCK2: Serial clock I/O • SO2: Serial data output • SI2: Serial data input 	N-ch. open-drain 5 V [P0A3/SDA, P0A2/SCL] CMOS push-pull [P0A1, SCK1, P0A0/SO1, P0B3, P0B2/SCK2, P0B1/SO2, P0B0]	Input [P0A3-P0A0, P0B3-P0B0]
11 12	INT1 INT0	Edge-detectable vector interrupt input. Both rising and falling edges can be selected	—	Input
13	CE	Selects operation of μPD17P005 and inputs reset signal	—	Input
14 16 17	P1A3 P1A1 P1A0/FCG	I/O lines of port 1A and external gate counter input line <ul style="list-style-type: none"> • P1A3-P1A0 • 4-bit CMOS I/O port • Can be set in input or output mode in 1-bit units • FCG • External gate counter input 	CMOS push-pull (P1A3-P1A0)	Input (P1A3-P1A0)
18 19 20 21	P1B3/PWM2 P1B2/PWM1 P1B1/PWM0 P1B0/CGP	Output lines of port 1B, D/A converter, and clock generator port <ul style="list-style-type: none"> • P1B3-P1B0 • 4-bit output port • PWM2-PWM0 • Output of D/A converter with 8-bit resolution • CGP • Clock generator port output 	N-ch open-drain 16 V [P1B3/PWM2 P1B1/PWM0] CMOS push-pull (P1B0/CGP)	Outputs undefined data (P1B3-P1B0)
22 25	P1C3 P1C0	4-bit CMOS output port	CMOS push-pull	Outputs undefined data

PIN NO.	SYMBOL	FUNCTION	OUTPUT FORM	WHEN POWER-ON RESET	
26	P1D ₃ /FMIFC	Analog input to port 1D, frequency counter, and A/D converter	—	Input (P1D ₃ -P1D ₀)	
27	P1D ₂ /AMIFC	<ul style="list-style-type: none"> • P1D₃-P1D₀ • 4-bit input port 			
28	P1D ₁ /ADC ₁	<ul style="list-style-type: none"> • FMIFC, AMIFC • Input of frequency counter 			
29	P1D ₀ /ADC ₀	<ul style="list-style-type: none"> • ADC₁, ADC₀ • Analog input to A/D converter with 6-bit resolution 			
30	V _{DD1}	Positive power supply. Apply 5 V±10% to this pin in normal operation mode. Apply 6 V to write, read, or verify program memory.	—	—	
31	VCOL	Inputs local oscillation frequency of PLL	—	Input	
32	VCOH				
33	GND	Ground	—	—	
34	X _{OUT}	Connect crystal oscillator for system clock oscillation across these pins.	CMOS push-pull	—	
35	X _{IN}		—		
36	EO ₀	Output from charge pump of PLL frequency synthesizer. Compares divided value of local oscillation frequency with phase of reference frequency, and outputs result of comparison	CMOS 3-state	High Impedance	
37	EO ₁				
38	LPF _{IN}	Input of amplifier for low-pass filter	—		
39	LPF _{OUT}	Output of amplifier for low-pass filter	N-ch open-drain 16 V		
40	V _{LPF}	Power to amplifier for low-pass filter	—		
41	V _{DD2}	Positive power supply. Apply 5 V±10% to this pin in normal operation mode. Apply 6 V to write, read, or verify program memory.	—	—	
42	P2A ₀	1-bit CMOS output port	CMOS push-pull	Outputs undefined data	
43	COM ₁	Outputs common signal of LCD controller/driver	CMOS 3-value output	Low-level output	
44	COM ₀				
45	LCD ₂₈ /P0F ₃	Output lines of ports 0F, 0E, 0X, 0Y, and segment signals of LCD controller/driver, and key source signals of key matrix	CMOS push-pull	Low-level output (LCD ₂₈ -LCD ₀)	
48	LCD ₂₈ /P0F ₀				<ul style="list-style-type: none"> • P0F₃-P0F₀ • 4-bit CMOS output port
49	LCD ₂₅ /P0E ₃				<ul style="list-style-type: none"> • P0E₃-P0E₀ • 4-bit CMOS output port
52	LCD ₂₂ /P0E ₀				<ul style="list-style-type: none"> • P0X₅-P0X₀ • 6-bit CMOS output port
53	LCD ₂₁ /P0X ₅				<ul style="list-style-type: none"> • P0Y₁₅-P0Y₀ • 16-bit CMOS output port
58	LCD ₁₈ /P0X ₀				<ul style="list-style-type: none"> • LCD₂₈-LCD₀ • Segment signal output of LCD controller/driver
59	LCD ₁₅ /P0Y ₁₅ /KS ₁₅				<ul style="list-style-type: none"> • KS₁₅-KS₀ • Key source signal output of key matrix
74	LCD ₀ /P0Y ₀ /KS ₀				

PIN NO.	SYMBOL	FUNCTION	OUTPUT FORM	WHEN POWER-ON RESET
<p>75</p> <p>—</p> <p>78</p>	<p>P0D₃/ADC₅</p> <p>—</p> <p>P0D₀/ADC₂</p>	<p>Port 0D, analog input line to A/D converter, and key source signal return input line of LCD segment</p> <ul style="list-style-type: none"> • P0D₃-P0D₀ <ul style="list-style-type: none"> · 4-bit input port · Connected to pull-down resistor • ADC₅-ADC₂ <ul style="list-style-type: none"> · Analog input to A/D converter with 6-bit resolution · Key source signal return input 	<p>—</p>	<p>Input with pull-down resistor (P0D₃-P0D₀)</p>

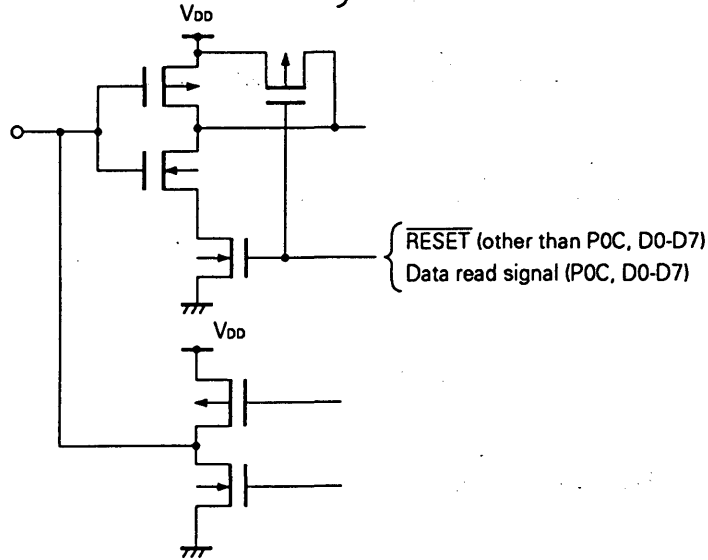
1.2 PROMPROGRAMMINGMODE

PIN NO.	SYMBOL	FUNCTION	OUTPUT FORM
11	V _{PP}	Positive power supply for PROM programming. Apply 12.5 V to this pin to write, read, or verify program memory.	—
30	V _{DD1}	Positive power supply. Apply 6 V to this pin to write, read, or verify program memory.	—
33	GND	Ground	—
35	CLK	Clock input for PROM programming	—
41	V _{DD2}	Positive power supply. Apply 6 V to this pin to write, read, or verify program memory.	—
45 52	D7 D0	8-bit data I/O for PROM programming	CMOS push-pull
75 78	MD3 MD0	Input to select operation mode when PROM is programmed	—

Remarks: Pins other than the above are not used in the PROM programming mode. For the processing of the unused pins, refer to (2) PROM programming mode in Pin Connections.

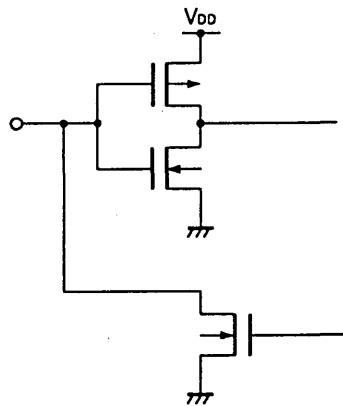
1.3 EQUIVALENT CIRCUIT OF PIN

- 1.3.1 P0A (P0A1/ $\overline{\text{SCK}}_1$, P0A0/SO1)
 - P0B (P0B3/SI1, P0B2/ $\overline{\text{SCK}}_2$, P0B1/SO2, P0B0/SI2)
 - P0C (P0C3, P0C2, P0C1, P0C0)*
 - P1A (P1A3, P1A2, P1A1, P1A0)
 - D0-D7*
- } (I/O)

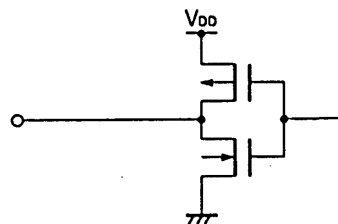


* :The $\overline{\text{RESET}}$ signal is not supplied to P0C and D0-D7.

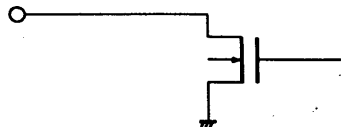
- 1.3.2 P0A (P0A3/SDA, P0A2/SCL) (I/O)



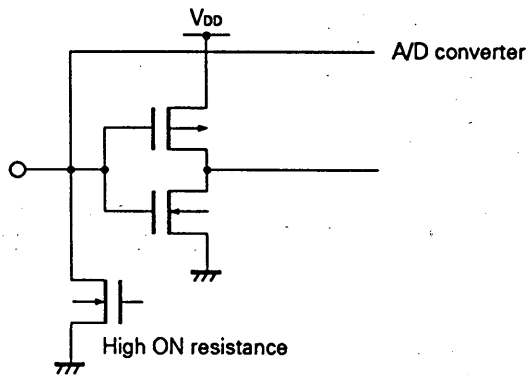
- 1.3.3 P1B (P1B0/CGP)
 - P1C (P1C3, P1C2, P1C1, P1C0)
 - P2A (P2A0)
 - LCD0/P0Y0/KS0-LCD29/P0F3
- } (Output)



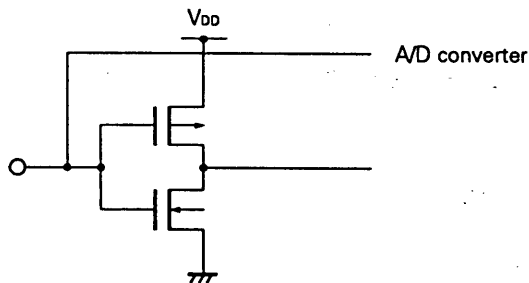
1.3.4 P1B (P1B₃/PWM₂, P1B₂/PWM₁, P1B₁/PWM₀) (Output)



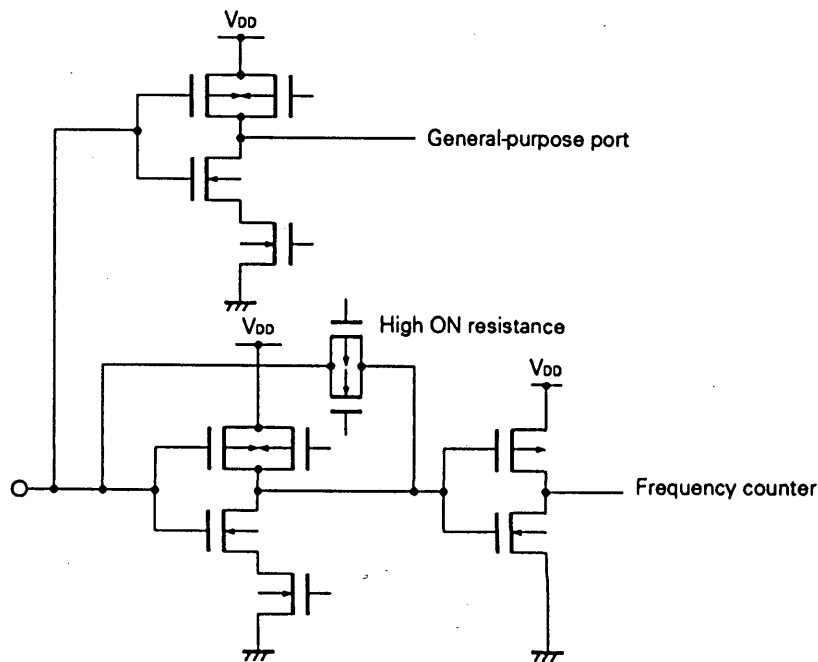
1.3.5 P0D (P0D₃/ADC₅/MD3, P0D₂/ADC₄/MD2, P0D₁/ADC₃/MD1, P0D₀/ADC₂/MD0) (Input)



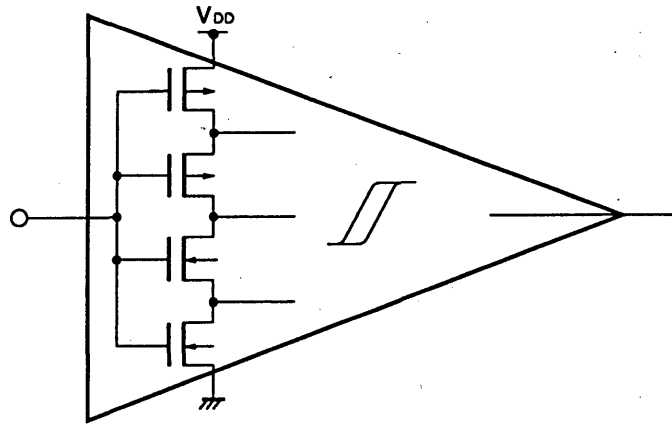
1.3.6 P1D (P1D₁/ADC₁, P1D₀/ADC₀) (Input)



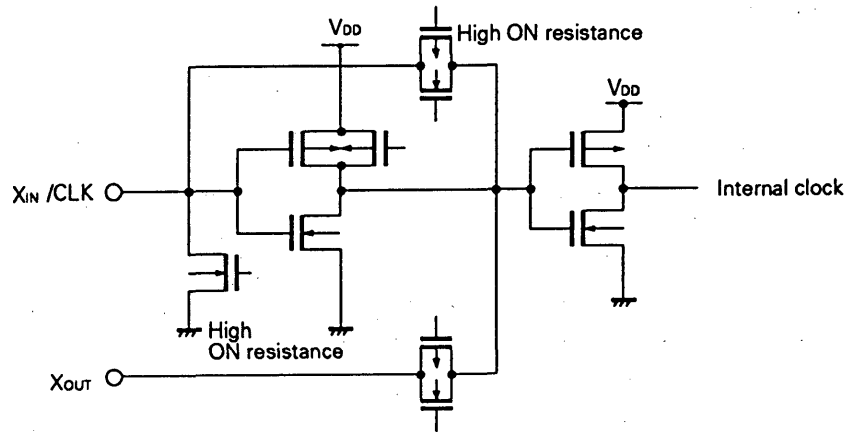
1.3.7 P1D (P1D₃/FMIFC, P1D₂/AMIFC) (Input)



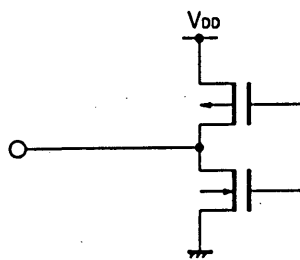
1.3.8 CE
 INT₁/V_{PP}
 INT₀ } (Schmitt trigger input)



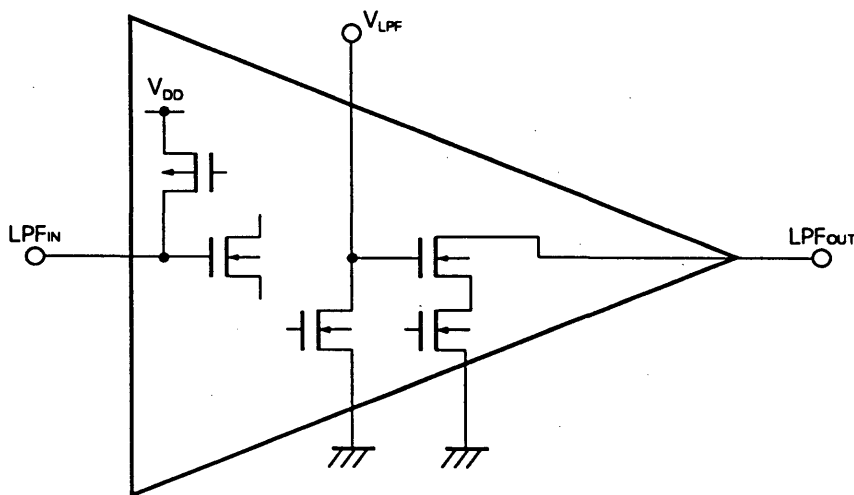
1.3.9 X_{out} (output), X_{in}/CLK (input)



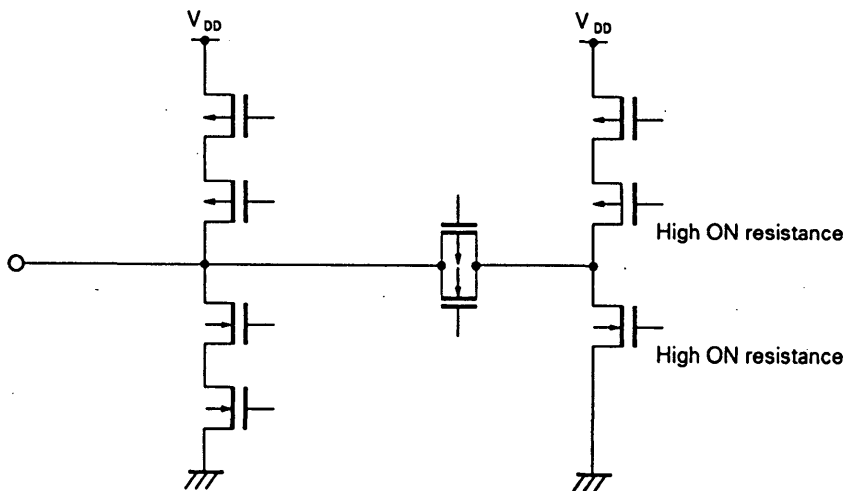
1.3.10 EO₁
 EO₀ } (Output)



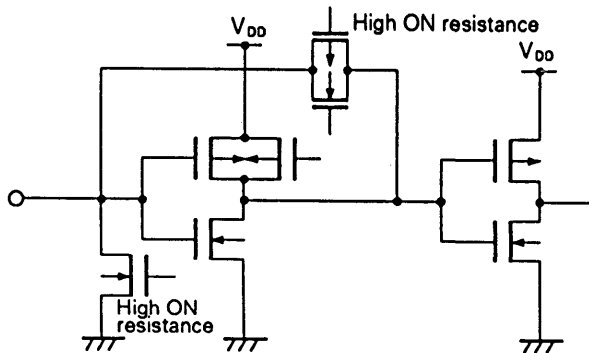
1.3.11 LPFin (input), LPFOut (output), VLPF



1.3.12 COM₁ } (Output)
COM₀ }



1.3.13 VCOH } (Input)
VCOL }



2. FUNCTION LIST

PRODUCT NAME		μPD17003A	μPD17005	μPD17P005
ROM (x16 bits)		3836 (mask ROM)	7932 (mask ROM)	7932 (PROM)
	Table reference area	256	7932	
RAM (x4 bits)		320	432	
	Data buffer	4		
	General register	16		
System register		12 x 4 bits		
Register file		33 x 4 bits (control register)		
General-purpose port register		24 x 4 bits		
Instruction execution time		4.44 μs (at 4.5 MHz, crystal oscillator)		
Stack level		7 (stack can be manipulated)		
General-purpose port	I/O port	16 lines		
	Input port	8 lines		
	Output port	9 lines (+30: LCD segment pin)		
Clock generator port		1 line		
LCD controller/driver		<ul style="list-style-type: none"> • 30 segment, 2 common 1/2 duty, 1/2 bias, frame frequency 250 Hz, drive voltage V_{DD} Segment pins multiplexed with key source: 16 lines All 30 lines can be used as output port pins (4, 4, 6, and 16 lines each of which can be independently set) 		
Serial interface		<ul style="list-style-type: none"> • 2 systems (3 channels) Serial interface 1: 2-line ... I²C bus mode*, serial I/O mode 3-line ... Serial I/O mode Serial interface 2: 3-line ... Serial I/O mode 		
D/A converter		• 8 bits x 3 lines (PWM output, output voltage: 16 V max.)		
A/D converter		• 6 bits x 6 lines (successive approximation method by software)		
Interrupt		<ul style="list-style-type: none"> • 5 channels (maskable interrupt) External interrupt : 2 channels (INT₀ pin, INT₁ pin) Internal interrupt : 3 channels (timer, serial interface 1, frequency counter) 		
Timer		<ul style="list-style-type: none"> • 2 systems Timer carry (1, 5, 100, 250 ms) Timer interrupt (1, 5, 100, 250 ms) 		
Reset function		<ul style="list-style-type: none"> • Power-ON reset (on power application) • Reset by CE pin (CE pin: low level → high level) • Power failure detection function 		

*: Among the PROM models, only μPD17P005GF-E00-3B9 can use the I²C bus mode.
 For the mask ROM model, it is confirmed when an order for the custom code is received.

(con't)

PRODUCT NAME		μPD17003A	μPD17005	μPD17P005
PLL frequency synthesizer	Division modes	<ul style="list-style-type: none"> • 2 modes Direct division mode (VCOL pin 30 MHz max.) Pulse swallow method (VCOL pin 40 MHz max.) (VCOH pin 150 MHz max.) 		
	Reference frequency	<ul style="list-style-type: none"> • 12 types selected by program 1, 1.25, 2.5, 3, 5, 6.25, 9, 10, 12.5, 25, 50, 100 kHz 		
	Charge pump	<ul style="list-style-type: none"> • Two independent error outputs 		
	Phase comparator	<ul style="list-style-type: none"> • Unlock can be detected through program Delay time of unlock FF selectable 		
	LPF amp	<ul style="list-style-type: none"> • CMOS operational amp. Output withstand voltage: 16 V max. 		
Frequency counter		<ul style="list-style-type: none"> • Frequency measurement P1D₃/FMIFC pin 5 to 15 MHz P1D₂/AMIFC pin 0.1 to 1 MHz • External gate width measurement P1A₀/FCG pin 		
Supply voltage		<ul style="list-style-type: none"> • V_{DD} = 4.5 to 5.5 V (PLL and CPU operate) • V_{DD} = 3.5 to 5.5 V (PLL stops, CPU operates) • V_{DD} = 2.2 to 5.5 V (crystal oscillator stops) 		
Package		80-pin plastic QFP (14 × 20 mm)		

3. WRITING, READING, AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The internal program memory of the μPD17P005 is a 15864 × 8 bit one-time PROM to which data can be electrically written. This PROM is accessed in 1-word or 16-bit units in a normal operation mode. When the program memory is written, read, or verified, the PROM is accessed in 1-word or 8-bit units. The higher 8 bits of 1 word or 16 bits are assigned to an even address, while the lower 8 bits are assigned to an odd address.

When the PROM is to be written, read, or verified, set the PROM mode and use the pins shown in Table 3-1 below.

Note that there is no address input pin. Instead, the clock signal input from the CLK pin is used to update the address.

Table 3-1 Pins Used to Write, Read, or Verify Program Memory

PIN NAME	FUNCTION
V _{PP}	Applies program voltage (12.5 V)
CLK	Inputs address updating clock
MD0-MD3	Select operation mode
D0-D7	Input/output 8-bit data
V _{DD1} , V _{DD2}	Apply supply voltage (6 V)

Write the internal PROM by using the following PROM programmer and program adapter:

- PROM programmer AF-9703 (Ando Electric.)
- AF-9704 (ditto)
- Program adapter AF-9803 (ditto)

3.1 OPERATION MODE FOR WRITING, READING, AND VERIFYING PROGRAM MEMORY

The μPD17P005 is set in a mode to write, read, or verify the program memory when +6 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin.

To set the program memory write, read, and verify modes, use the MD0 through MD3 pins as shown in Table 3-2.

The pins not used to write, read, or verify the program memory should be either opened, or connected to GND through a pull-down resistor (470 Ω). (Refer to (2) PROM programming mode in Pin Configuration.)

Table 3-2 Operation Mode When Program Memory is Written, Read, or Verified

SPECIFIES OPERATION MODE						OPERATION MODE
V _{PP}	V _{DD}	MD0	MD1	MD2	MD3	
+12.5V	+6V	H	L	H	L	Clears program memory address to 0
		L	H	H	H	Write mode
		L	L	H	H	Read, verify modes
		H	X	H	H	Program inhibit mode

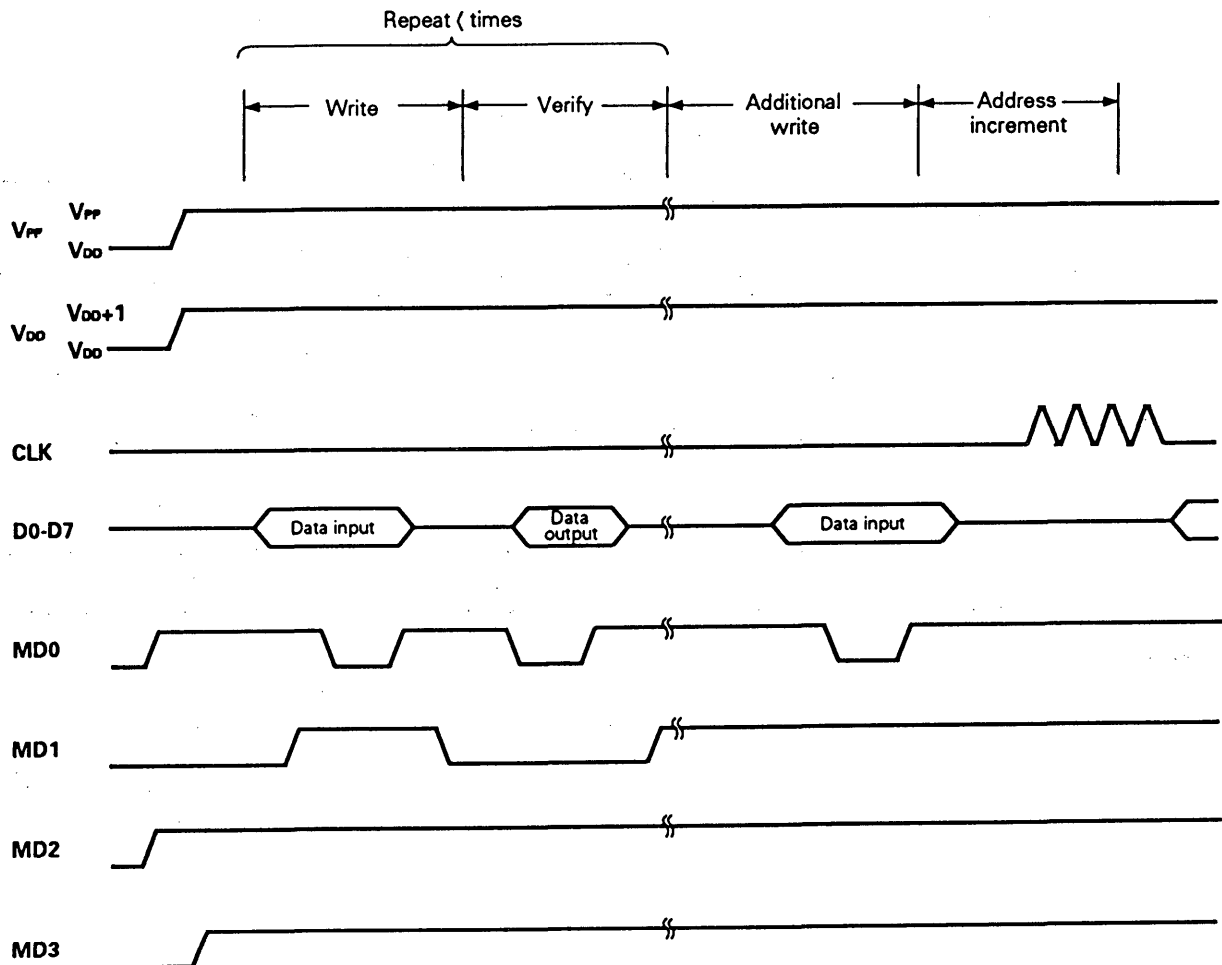
Remarks: X: L or H

3.2 WRITING PROGRAM MEMORY

The program memory can be written at high speeds in the following sequence:

- (1) Pull down the unused pins to GND through a resistor. Keep the CLK pin at the low level.
- (2) Supply 5 V to the V_{DD} and V_{PP} pins.
- (3) Wait for 10 us.
- (4) Set the program memory address 0 clear mode.
- (5) Supply 6 V to the V_{DD} pin and 12.5 V to the V_{PP} pin.
- (6) Set the program inhibit mode.
- (7) Write data in 1-ms write mode.
- (8) Set the program inhibit mode.
- (9) Set the verify mode. If the program memory has been correctly written, proceed to step (10). If not, repeat steps (7) through (9).
- (10) Additional writing of (Number of times the program memory has been written in (7) through (9): X) × 1 ms
- (11) Set the program inhibit mode.
- (12) Input a pulse to the CLK pin four times to update the program memory address by one (+1).
- (13) Repeat steps (7) through (12) until the last address is written.
- (14) Set the program memory address 0 clear mode.
- (15) Change the voltage on the V_{DD} and V_{PP} pins to 5 V.
- (16) Turn off the power.

Steps (2) through (12) are illustrated below.

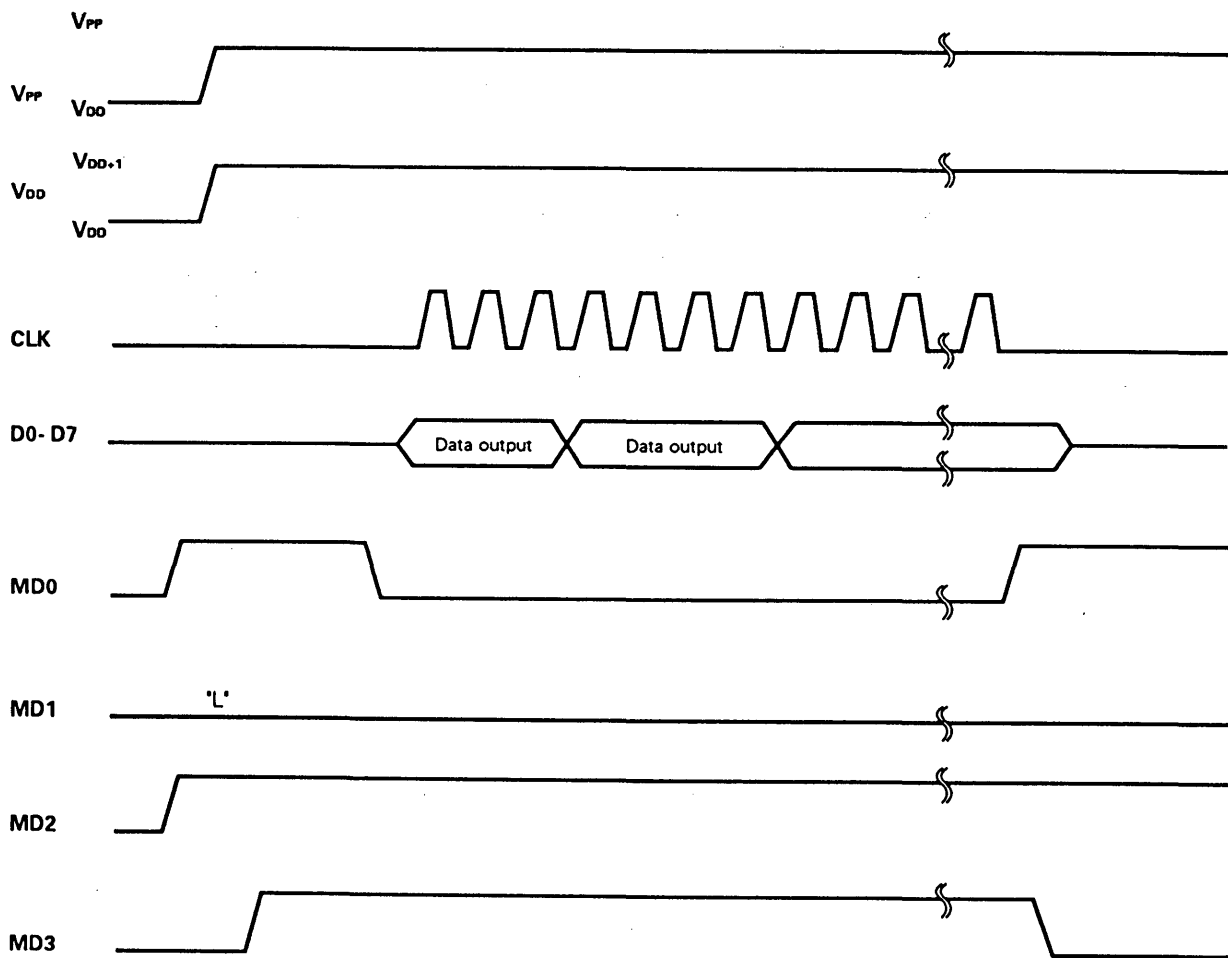


3.3 READING PROGRAM MEMORY

Read the contents of the program memory of the μPD17P005 in the following sequence:

- (1) Pull down the unused pins to GND through a resistor. Keep the CLK pin at the low level.
- (2) Supply 5 V to the V_{DD} and V_{PP} pins.
- (3) Wait for 10 us.
- (4) Set the program memory address 0 clear mode.
- (5) Supply 6 V to the V_{DD} pin and 12.5 V to the V_{PP} pin.
- (6) Set the program inhibit mode.
- (7) Set the verify mode. When the clock pulse is input to the CLK pin, data is sequentially output one address at a time with four clocks constituting one cycle.
- (8) Set the program inhibit mode.
- (9) Set the program memory address 0 clear mode
- (10) Change the voltage on the V_{DD} and V_{PP} pins to 5 V.
- (11) Turn off the power.

Steps (2) through (9) are illustrated below.



4. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (Ta = 25±2°C)

PARAMETER	SYMBOL	CONDITION	RATINGS	UNIT
Supply Voltage	V _{DD}		- 0.3 to +6.0	V
Input Voltage	V _I		- 0.3 to V _{DD} + 0.3	V
Output Voltage	V _O	Except P1B ₁ - P1B ₃ , P0A ₂ , P0A ₃ , LPF _{OUT}	- 0.3 to V _{DD} + 0.3	V
Output Withstand Voltage	V _{BDS1}	P1B ₁ - P1B ₃ , LPF _{OUT}	18.0	V
	V _{BDS2}	P0A ₂ , P0A ₃	V _{DD} + 0.3	V
High-Level Output Current	I _{OH}	1 pin	- 12	mA
		Total of all pins	- 20	mA
Low-Level Output Current	I _{OL}	1 pin	12	mA
		Total of all pins	20	mA
Operating Temperature	T _{opt}		- 40 to + 85	°C
Storage Temperature	T _{stg}		- 55 to + 125	°C

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V _{DD1}	PLL and CPU operate	4.5	5.0	5.5	V
Supply Voltage	V _{DD2}	PLL stops, CPU operates	3.5	5.0	5.5	V
Data Retention Voltage	V _{DDR}	Crystal oscillator stops	2.2		5.5	V
Supply Voltage Rise Time	t _{rise}	V _{DD} = 0 → 4.5 V			500	ms
Input Amplitude	V _{In1}	V _{COL} , V _{COH}	0.5		V _{DD}	V _{P-P}
	V _{In2}	AMIFC, FMIFC	0.5		V _{DD}	V _{P-P}
Output Withstand Voltage	V _{BDS}	P1B ₁ - P1B ₃ , LPF _{OUT}			16.0	V
Operating Temperature	T _{opt}		- 40		+85	°C

DC Characteristics (Ta = -40 to +85°C, VDD = 4.5 to 5.5 V)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VDD1	CPU and PLL operate	4.5	5.0	5.5	V
	VDD2	CPU operates, PLL stops	3.5	5.0	5.5	V
Supply Current	IDD1	CPU operates, PLL stops. XIN pin Sine wave input (fIN = 4.5 MHz, VIN = VDD), Ta = 25°C		2.8	5.6	mA
	IDD2	CPU operates, PLL stops, HALT instruction is used (20 instructions executed in 1 ms) XIN pin Sine wave input (fIN = 4.5 MHz, VIN = VDD), Ta = 25°C		1.9	3.8	mA
Data Retention Voltage	VDDR1	Power failure detected by timer FF; with crystal oscillator	3.5		5.5	V
	VDDR2	Power failure detected by timer FF; crystal oscillator stops	2.2		5.5	V
	VDDR3	Data memory (RAM) retained	2.0		5.5	V
Data Retention Current	IDDR1	Crystal oscillator stops Ta = 25°C		2	15	μA
	IDDR2	Crystal oscillator stops VDD = 5.0 V, Ta = 25°C		2	10	μA
Intermediate Level Output Voltage	VOM1	COM0, COM1 VDD = 5 V	2.3	2.5	2.7	V
High-Level Input Voltage	VIH1	P0A0-P0A3, P0B0-P0B3, P0C0-P0C3, P1A0-P1A3, P1D0-P1D3, CE, INT0, INT1	0.8 VDD		VDD	V
	VIH2	P0D0-P0D3	0.6 VDD		VDD	V
Low-Level Input Voltage	VIL	P0A0-P0A3, P0B0-P0B3, P0C0-P0C3, P0D0-P0D3, P1A0-P1A3, P1D0-P1D3, CE, INT0, INT1	0		0.2 VDD	V
High-Level Output Current	IOH1	P0A0, P0A1, P0B0-P0B3, P0C0-P0C3, P1A0-P1A3, P1C0-P1C3, P1B0, P2A3, VOH = VDD - 1 V	-1.0	-5.0		mA
	IOH2	LCD0-LCD29, EO0, EO1 VOH = VDD - 1 V	-1.0	-4.0		mA
Low-Level Output Current	IOL1	P0A0-P0A3, P0B0-P0B3, P0C0-P0C3, P1A0-P1A3, P1C0-P1C3, P1B0, P2A0, VOL = 1 V	1.0	7.0		mA
	IOL2	LCD0-LCD29, EO0, EO1 VOL = 1 V	1.0	3.5		mA
	IOL3	P1B1-P1B3 VOL = 1 V	1.0	2.0		mA
	IOL4	P0A2, P0A3 VOL = 1 V	1.0	10.0		mA
High-Level Input Current	IiH1	VCOH pulled down VIH = VDD	0.1	0.8		mA
	IiH2	VCOL pulled down VIH = VDD	0.1	0.8		mA
	IiH3	XIN pulled down VIH = VDD	0.1	1.3		mA
	IiH4	P0D0-P0D3 pulled down VIH = VDD	0.05	0.13	0.30	mA
Output Off Leakage Current	IL1	P0A2, P0A3 VOH = VDD			500	nA
	IL2	P1B1-P1B3, LPFOUT VOH = 16 V			500	nA
	IL3	EO0, EO1 VOH = VDD, VOL = 0 V			±100	nA

AC Characteristics (Ta = -40 to +85°C, VDD = 4.5 to 5.5 V)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX	UNIT
Operating Frequency	f _{IN1}	VCOL MF mode, sine wave input V _{IN} = 0.3 V _{P-P}	0.5		30	MHz
	f _{IN2}	VCOL HF mode, sine wave input V _{IN} = 0.3 V _{P-P}	5		40	MHz
	f _{IN3}	VCOH, sine wave input V _{IN} = 0.3 V _{P-P}	9		150	MHz
	f _{IN4}	AMIFC, sine wave input V _{IN} = 0.5 V _{P-P}	0.1		1	MHz
	f _{IN5}	AMIFC, sine wave input V _{IN} = 0.05 V _{P-P}	0.44		0.46	MHz
	f _{IN6}	FMIFC, sine wave input V _{IN} = 0.5 V _{P-P}	5		15	MHz
	f _{IN7}	FMIFC, sine wave input V _{IN} = 0.06 V _{P-P}	10.5		10.9	MHz
A/D Converter Resolution					6	bit
A/D Converter Total Error		Ta = -10 to +50°C		±1	±1.5	LSB

Reference Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX	UNIT
Supply Current	I _{DD3}	CPU and PLL operate VCOH sine wave input f _{IN} = 150 MHz, V _{IN} = 0.5 V _{P-P} V _{DD} = 5 V, Ta = 25°C		15		mA
High-Level Output Current	I _{OH4}	COM ₀ , COM ₁ V _{OH} = V _{DD} - 1 V		-0.2		mA
Intermediate Level Output Current	I _{OM1}	COM ₀ , COM ₁ V _{OM} = V _{DD} - 1 V		-20		μA
	I _{OM2}	COM ₀ , COM ₁ V _{OM} = 1 V		20		μA
Low-Level Output Current	I _{OL5}	COM ₀ , COM ₁ V _{OL} = 1 V		0.2		mA

DC Programming Characteristics (Ta = 25°C, VDD = 6.0±0.25 V, VPP = 12.5±0.5 V)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
High-Level Input Voltage	V _{IH1}	Other than CLK	0.7 V _{DD}		V _{DD}	V
	V _{IH2}	CLK	V _{DD} - 0.5		V _{DD}	V
Low-Level Input Voltage	V _{IL1}	Other than CLK	0		0.3 V _{DD}	V
	V _{IL2}	CLK	0		0.4	V
Input Leakage Current	I _{LI}	V _{IN} = V _{IL} or V _{IH}			±10	μA
High-Level Output Voltage	V _{OH}	I _{OH} = -1 mA	V _{DD} - 1.0			V
Low-Level Output Voltage	V _{OL}	I _{OL} = 1 mA			1.0	V
V _{DD} Supply Current	I _{DD}				30	mA
V _{PP} Supply Current	I _{PP}	MD0 = V _{IL} , MD1 = V _{IH}			30	mA

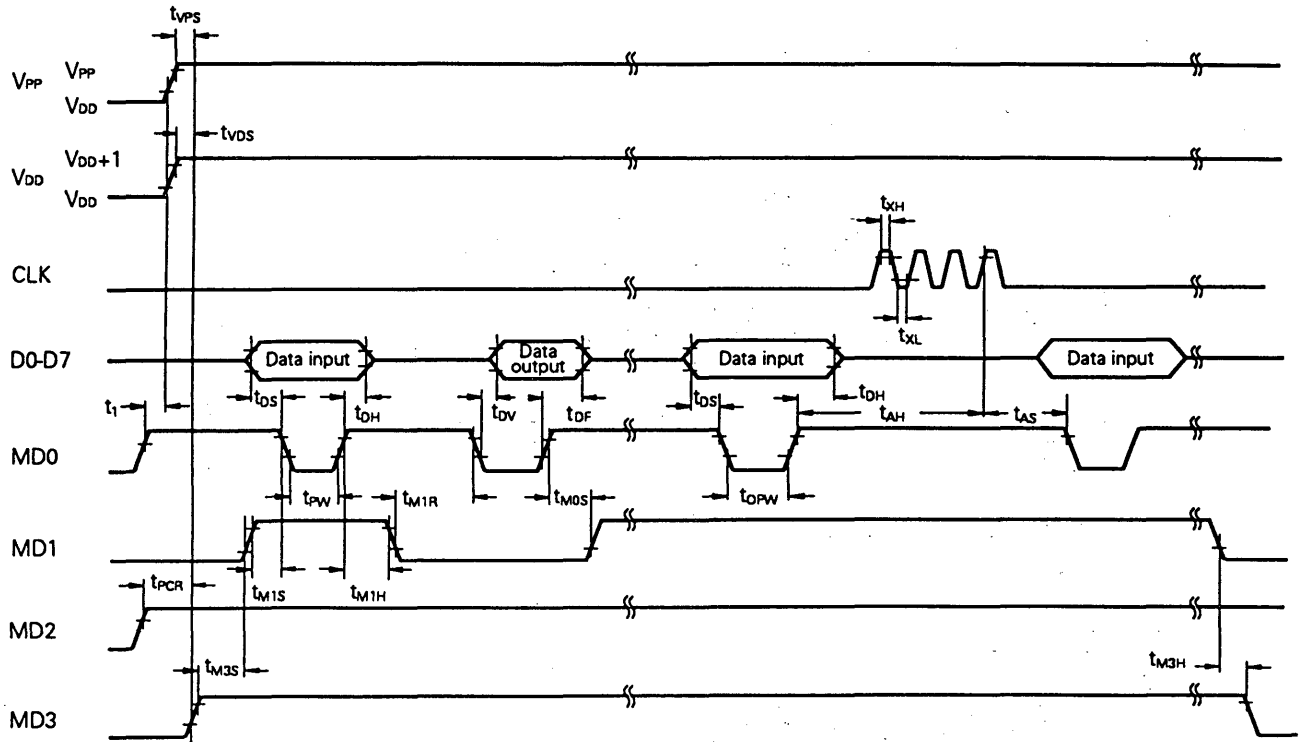
Note: 1. Keep V_{PP} to within +13.5 V including the overshoot.
 2. Apply V_{DD} before V_{PP} and turn it off after V_{PP}.

AC Programming Characteristics (Ta = 25°C, VDD = 6.0±0.25 V, VPP = 12.5±0.5 V)

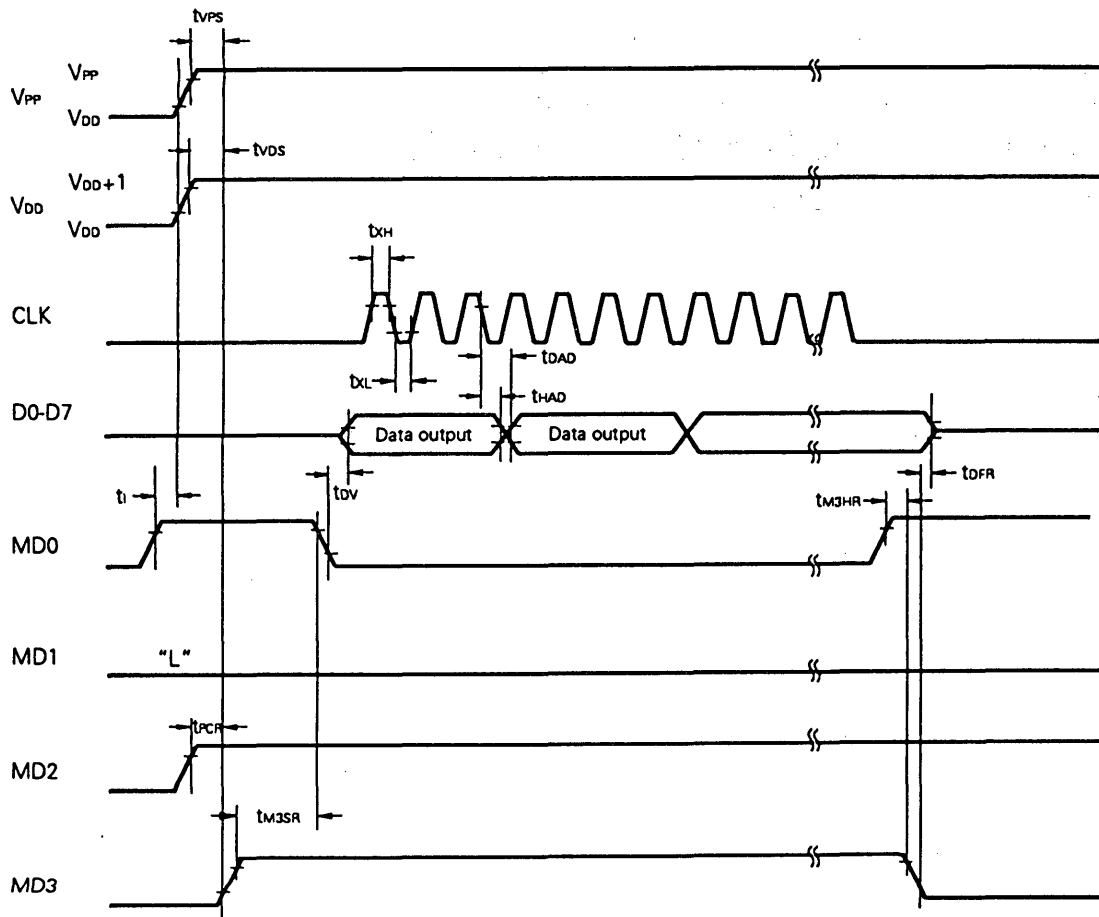
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Address Setup Time* (vs. MD0↓)	t _{AS}		2			μs
MD1 Setup Time (vs. MD0↓)	t _{M1S}		2			μs
Data Setup Time (vs. MD0↓)	t _{DS}		2			μs
Address Hold Time* (vs. MD0↑)	t _{AH}		2			μs
Data Hold Time (vs. MD0↑)	t _{DH}		2			μs
MD0↑→Data Output Float Delay Time	t _{DF}		0		130	ns
V _{PP} Setup Time (vs. MD3↑)	t _{VPS}		2			μs
V _{DD} Setup Time (vs. MD3↑)	t _{VDS}		2			μs
Initial Program Pulse Width	t _{PW}		0.95	1.0	1.05	ms
Additional Program Pulse Width	t _{OPW}		0.95		21.0	ms
MD0 Setup Time (vs. MD1↑)	t _{M0S}		2			μs
MD0↓→Data Output Delay Time	t _{DOV}	MD0 = MD1 = V _{IL}			1	μs
MD1 Hold Time (vs. MD0↑)	t _{M1H}	t _{M1H} + t _{M1R} ≥ 50 μs	2			μs
MD1 Recovery Time (vs. MD0↓)	t _{M1R}		2			μs
Program Counter Reset Time	t _{PCR}		10			μs
CLK Input High-, Low-Level Width	t _{XH} , t _{XL}		0.125			μs
CLK Input Frequency	f _X				4.19	MHz
Initial Mode Set Time	t _I		2			μs
MD3 Setup Time (vs. MD1↑)	t _{M3S}		2			μs
MD3 Hold Time (vs. MD1↓)	t _{M3H}		2			μs
MD3 Setup Time (vs. MD0↓)	t _{M3SR}	Program memory read	2			μs
Address*→Data Output Delay Time	t _{DAD}	Program memory read	2			μs
Address*→Data Output Hold Time	t _{HAD}	Program memory read	0		130	ns
MD3 Hold Time (vs. MD0↑)	t _{M3HR}	Program memory read	2			μs
MD3↓→Data Output Float Delay Time	t _{DFR}	Program memory read	2			μs

*: The internal address signal is incremented (+1) at the falling edge of the address signal. The internal address is not connected to a pin.

Program memory write timing

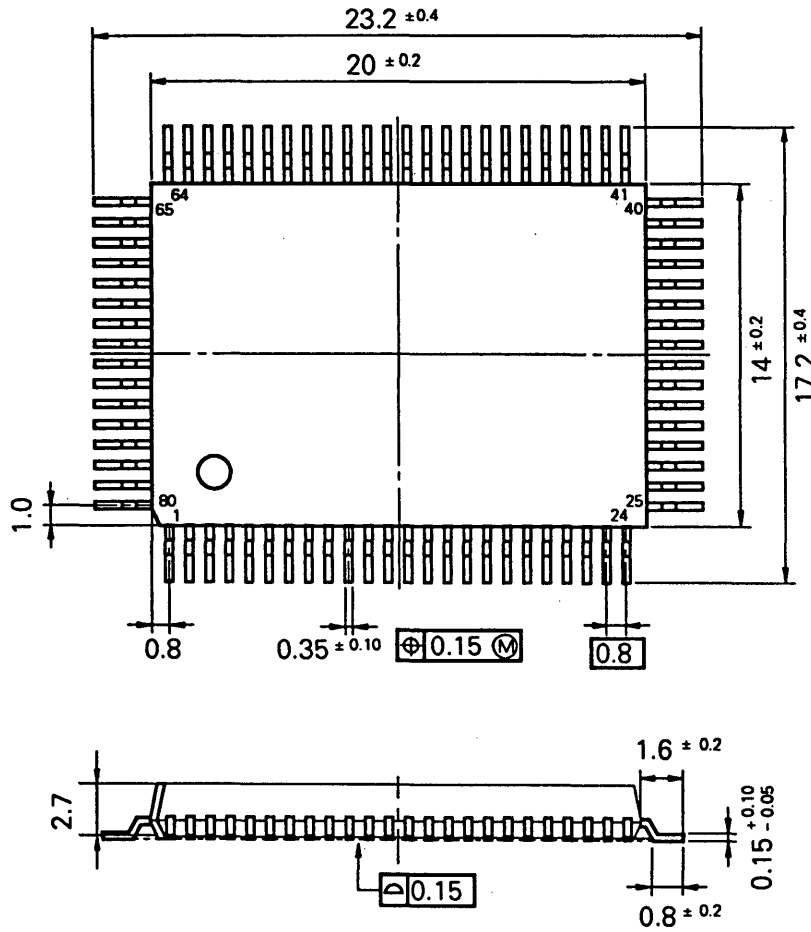


Program memory read timing

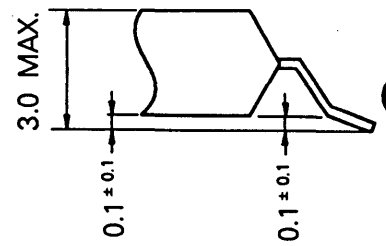


5. PACKAGE DRAWINGS

80-Pin Plastic QFP (14 × 20) (Unit: mm)



Details of tip of pin



6. RECOMMENDED SOLDERING CONDITIONS

The μPD17P005 should be soldered under the following recommended conditions. For soldering conditions other than those recommended below, consult NEC.

Table 6-1 List of Recommended Soldering Conditions

PRODUCT NAME	PACKAGE	CODE
μPD17P005GF-3B9	80-pin plastic QFP (14 × 20 mm)	.IR30-162
μPD17P005GF-E00-3B9		.VP15-162
μPD17P005GF-xxx-3B9		.WS60-162
		.Pin partial heating

Table 6-2 Soldering Conditions

CODE	SOLDERING METHOD	SOLDERING CONDITIONS
IR30-162	Infrared reflow	Package peak temperature: 230°C, Time: 30 seconds max. (210°C min.), Number of times: 1, Number of days*: 2 (after this, prebaking is necessary at 125°C for 16 hours)
VP15-162	VPS	Package peak temperature: 215°C, Time: 40 seconds max. (200°C min.), Number of times: 1, Number of days*: 2 (after this, prebaking is necessary at 125°C for 16 hours)
WS60-162	Wave soldering	Soldering oven temperature: 260°C max., Time: 10 seconds max., Number of times: 1, Number of days*: 2 (after this, prebaking is necessary at 125°C for 16 hours)
Pin partial heating	Pin partial heating	Pin temperature: 300°C max., Time: 10 seconds max.

*: The number of days the device can be stored after the dry pack has been opened. The storing conditions are 25°C, 65% RH max.

Note: Do not use two or more soldering methods in combination (except for the pin partial heating method).

Remarks: For details of the recommended soldering conditions, refer to "Semiconductor Device Mounting Manual" (IEI-616).

APPENDIX DEVELOPMENT TOOLS

The following development tools are readily available to support the development of the μPD17P005 program:

Hardware

NAME	OUTLINE	ORDERCODE
In-circuit Emulator	This in-circuit emulator is used in common with the 17K series products. When developing the program of μPD17P005, a system evaluation board (SE board) is used in combination with the in-circuit emulator. The in-circuit emulator operates with a RAM base. By connecting it to a console, the program can be added to and edited on the console. In addition, more sophisticated program development environments can be created by using the support software SIMPLEHOST™.	IE-17K IE-17K-ET*
SE board	Used to evaluate the system of μPD17P005 in stand-alone mode, or in combination with the in-circuit emulator.	SE-17010
Emulation Probe	Connects the SE board to the target system.	EP-17003GF
Conversion socket	Connects to the target system in combination with the emulation probe.	EV-9200G-80
PROM programmer	The PROM of the μPD17P005 can be programmed by using a dedicated program adapter AF-9803.	AF-9703 AF-9704 (Ando Electric)
Program adapter	Used in combination with the PROM programmer.	AF-9803 (Ando Electric)

Remarks: For the details of the PROM programmer and program adapter, consult Ando Electric.

*: Low-cost model: with external power supply

Software

NAME	OUTLINE	HOST MACHINE	OS	SUPPLY MEDIA	ORDER CODE	
17K series assembler	AS17K is an assembler that can be used in common with the 17K series products. When developing the program of the μPD17P005, AS17K is used in combination with a device file (AS17005).	PC-9800 series	MS-DOS™ (Ver.3.1toVer.3.30C)	5"2HD	μS5A10AS17K	
				3.5"2HD	μS5A13AS17K	
		IBM PC/AT™	PCDOS™ (Ver. 3.1)	5"2HC	μS7B10AS17K	
Device file (AS17005)	AS17005 is a device file for μPD17005 and μPD17P005, and is used in combination with an assembler for the 17K series (AS17K).	PC-9800 series	MS-DOS (Ver.3.1toVer.3.30C)	5"2HD	μS5A10AS17005	
				3.5"2HD	μS5A13AS17005	
		IBM PC/AT	PCDOS (Ver. 3.1)	5"2HC	μS7B10AS17005	
Support software (SIMPLEHOST)	SIMPLEHOST is a software package that enables man-machine interface in MS-WINDOWS™ when a program is developed by using an in-circuit emulator and a personal computer.	PC-9800 series	MS-DOS (Ver. 3.1to Ver. 3.30C)	MS- WINDOWS (Ver. 2.1 to Ver. 3.0)	5"2HD	μS5A10E17K
					3.5"2HD	μS5A13E17K
		IBM PC/AT	PCDOS (Ver. 3.1)	5"2HC	μS7B10E17K	

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(MEMO)

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