LTC1595/LTC1596

Serial 16-Bit Multiplying DACs

October 1997

FEATURES

- **SO-8 Package (LTC1595)**
- **DNL and INL: 1LSB Max**
- **Low Glitch Impulse: <2nV-s**
- Pin Compatible with Industry Standard 12-Bit DACs: LTC8043 and LTC8143/LTC7543
- 4-Quadrant Multiplication
- Low Power Consumption
- Power-On Reset
- Daisy-Chain Serial Output (LTC1596)
- Asynchronous Clear Input (LTC1596)

APPLICATIONS

- Process Control and Industrial Automation
- Software Controlled Gain Adjustment
- Digitally Controlled Filter and Power Supplies
- Automatic Test Equipment

DESCRIPTION

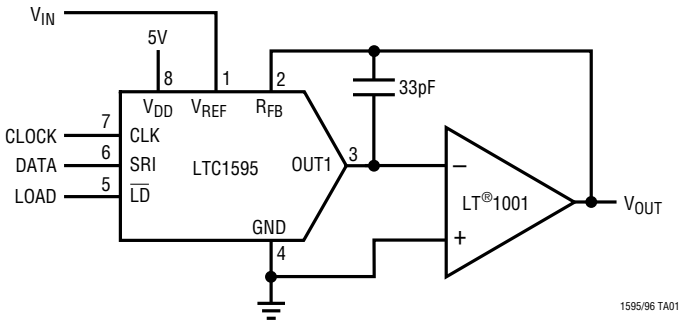
The LTC®1595/LTC1596 are serial input, 16-bit multiplying current output DACs. The LTC1595 is pin and hardware compatible with the 12-bit LTC8043 and comes in 8-pin PDIP and SO packages. The LTC1596 is pin and hardware compatible with the 12-bit LTC8143/LTC7543 and comes in 16-pin PDIP and SO wide packages.

Both are specified over the industrial temperature range. Sensitivity of INL to op amp V_{OS} is reduced by five times compared to the industry standard 12-bit DACs, so most systems can be easily upgraded to true 16-bit resolution and linearity without requiring more precise op amps.

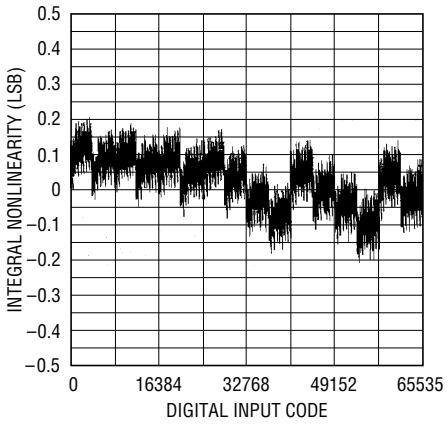
These DACs include an internal deglitching circuit that reduces the glitch impulse by more than ten times to less than 2nV-s typ.

TYPICAL APPLICATION

SO-8 Multiplying DAC Has Easy 3-Wire Serial Interface



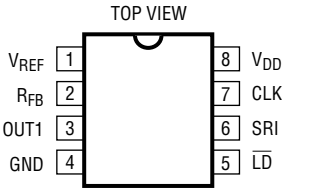
Integral Nonlinearity



ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... −0.5V to 7V
V_{DD} to DGND ..... −0.5V to 7V
AGND to DGND ..... V_{DD} + 0.5V
DGND to AGND ..... V_{DD} + 0.5V
V_{REF} to AGND, DGND ..... ±25V
R_{FB} to AGND, DGND ..... ±25V
Digital Inputs to DGND ..... −0.5V to V_{DD} + 0.5V
V_{OUT1}, V_{OUT2} to AGND ..... −0.5V to V_{DD} + 0.5V
Maximum Junction Temperature ..... 150°C
Operating Temperature Range
LTC1595C/LTC1596C ..... 0°C to 70°C
LTC1595I/LTC1596I ..... −40°C to 85°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



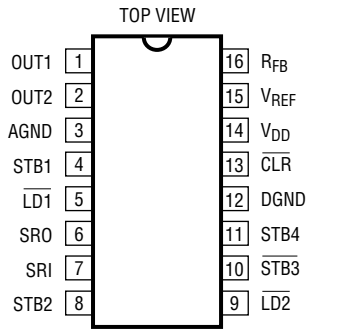
N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 130°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 190°C/W (S)

ORDER PART NUMBER
LTC1595ACN8
LTC1595ACS8
LTC1595BCN8
LTC1595BCS8
LTC1595CCN8
LTC1595CCS8
LTC1595AIN8
LTC1595AIS8
LTC1595BIN8
LTC1595BIS8
LTC1595CIN8
LTC1595CIS8

S8 PART MARKING	
1595A	1595AI
1595B	1595BI
1595C	1595CI



N PACKAGE
16-LEAD PDIP

SW PACKAGE
16-LEAD PLASTIC SO WIDE

T_{JMAX} = 150°C, θ_{JA} = 100°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 130°C/W (SW)

ORDER PART NUMBER
LTC1596ACN
LTC1596ACSW
LTC1596BCN
LTC1596BCSW
LTC1596CCN
LTC1596CCSW
LTC1596AIN
LTC1596AISW
LTC1596BIN
LTC1596BISW
LTC1596CIN
LTC1596CISW

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V ±10%, V_{REF} = 10V, V_{OUT1} = V_{OUT2} = AGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1595A/96A MIN	LTC1595A/96A TYP	LTC1595A/96A MAX	LTC1595B/96B MIN	LTC1595B/96B TYP	LTC1595B/96B MAX	LTC1595C/96C MIN	LTC1595C/96C TYP	LTC1595C/96C MAX	UNITS
Accuracy													
	Resolution		●	16			16			16			Bits
	Monotonicity		●	16			16			15			Bits
INL	Integral Nonlinearity	(Note 1) T_A = 25°C			±0.25	±1			±2			±4	LSB
		T_{MIN} to T_{MAX}	●		±0.35	±1			±2			±4	LSB
DNL	Differential Nonlinearity	T_A = 25°C			±0.2	±1			±1			±2	LSB
		T_{MIN} to T_{MAX}	●		±0.2	±1			±1			±2	LSB
GE	Gain Error	(Note 2) T_A = 25°C			2	±16			±16			±32	LSB
		T_{MIN} to T_{MAX}	●		3	±16			±32			±32	LSB

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V ±10%, V_{REF} = 10V, V_{OUT1} = V_{OUT2} = AGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Gain Temperature Coefficient	(Note 3) ΔGain/ΔTemperature	●		1	2	ppm/°C
$I_{LEAKAGE}$	OUT1 Leakage Current	(Note 4) T_A = 25°C T_{MIN} to T_{MAX}	 ●			±3 ±15	nA nA
	Zero-Scale Error	T_A = 25°C T_{MIN} to T_{MAX}	 ●			±0.2 ±1	LSB LSB
PSRR	Power Supply Rejection	V_{DD} = 5V ±10%	●		±1	±2	LSB/V
Reference Input							
R_{REF}	V_{REF} Input Resistance	(Note 5)	●	5	7	10	kΩ
AC Performance							
	Output Current Settling Time	(Notes 6, 7)			1		µs
	Midscale Glitch Impulse	$C_{FEEDBACK}$ = 33pF			1.9		nV-s
	Digital-to-Analog Glitch Impulse	(Notes 6, 8)			2		nV-s
	Multiplying Feedthrough Error	V_{REF} = ±10V, 10kHz Sine Wave			1		mV_{P-P}
THD	Total Harmonic Distortion	(Note 9)			108		dB
	Output Noise Voltage Density	(Note 10) f = 1kHz			11		nV/√Hz
Analog Outputs (Note 3)							
C_{OUT}	Output Capacitance (Note 3)	DAC Register Loaded to All 1s C_{OUT1}	 ●		100		pF
		DAC Register Loaded to All 0s C_{OUT1}	 ●		60		pF
Digital Inputs							
V_{IH}	Digital Input High Voltage		●	2.4			V
V_{IL}	Digital Input Low Voltage		●			0.8	V
I_{IN}	Digital Input Current		●		0.001	±1	µA
C_{IN}	Digital Input Capacitance	(Note 3) V_{IN} = 0V	●			8	pF
Digital Outputs: SRO (LTC1596)							
V_{OH}	Digital Output High Voltage	I_{OH} = 200µA	●	4			V
V_{OL}	Digital Output Low Voltage	I_{OL} = 1.6mA	●			0.4	V

V_{DD} = 5V ±10%, V_{REF} = 10V, V_{OUT1} = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Timing Characteristics (LTC1595)							
t_{DS}	Serial Input to CLK Setup Time		●	30	5		ns
t_{DH}	Serial Input to CLK Hold Time		●	30	5		ns
t_{SRI}	Serial Input Data Pulse Width		●	60			ns
t_{CH}	Clock Pulse Width High		●	60			ns
t_{CL}	Clock Pulse Width Low		●	60			ns
t_{LD}	Load Pulse Width		●	60			ns
t_{ASB}	LSB Clocked into Input Register to DAC Register Load Time		●	0			ns

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V ±10%, V_{REF} = 10V, V_{OUT1} = V_{OUT2} = AGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Timing Characteristics (LTC1596)							
t_{DS1}	Serial Input to Strobe Setup Time	STB1 Used as the Strobe	●	30	5		ns
t_{DS2}		STB2 Used as the Strobe	●	20	–5		ns
t_{DS3}		$\overline{STB3}$ Used as the Strobe	●	25	0		ns
t_{DS4}		STB4 Used as the Strobe	●	20	–5		ns
t_{DH1}	Serial Input to Strobe Hold Time	STB1 Used as the Strobe	●	30	5		ns
t_{DH2}		STB2 Used as the Strobe	●	40	15		ns
t_{DH3}		STB3 Used as the Strobe	●	35	10		ns
t_{DH4}		STB4 Used as the Strobe	●	40	15		ns
t_{SRI}	Serial Input Data Pulse Width		●	60			ns
t_{STB1} to t_{STB4}	Strobe Pulse Width	(Note 11)	●	60			ns
$t_{\overline{STB1}}$ to $t_{\overline{STB4}}$	$\overline{Strobe}$ Pulse Width	(Note 12)	●	60			ns
$t_{\overline{LD1}}$, $t_{\overline{LD2}}$	$\overline{LD}$ Pulse Width		●	60			ns
t_{ASB}	LSB Strobed into Input Register to Load DAC Register Time		●	0			ns
t_{CLR}	Clear Pulse Width		●	100			ns
t_{PD1}	STB1 to SRO Propagation Delay	C_L = 50pF	●	30		150	ns
t_{PD}	STB2, $\overline{STB3}$, STB4 to SRO Propagation Delay	C_L = 50pF	●	30		200	ns
Power Supply							
V_{DD}	Supply Voltage		●	4.5	5	5.5	V
I_{DD}	Supply Current	Digital Inputs = 0V or V_{DD}	●		1.5	10	µA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: ±1LSB = ±0.0015% of full scale = ±15.3ppm of full scale.

Note 2: Using internal feedback resistor.

Note 3: Guaranteed by design, not subject to test.

Note 4: I_{OUT1} with DAC register loaded with all 0s.

Note 5: Typical temperature coefficient is 100ppm/C.

Note 6: OUT1 load = 100Ω in parallel with 13pF.

Note 7: To 0.0015% for a full-scale change, measured from the falling edge of $\overline{LD1}$, $\overline{LD2}$ or $\overline{LD}$.

Note 8: V_{REF} = 0V. DAC register contents changed from all 0s to all 1s or all 1s to all 0s.

Note 9: V_{REF} = $6V_{RMS}$ at 1kHz. DAC register loaded with all 1s; op amp = LT1007.

Note 10: Calculation from $e_n = \sqrt{4kTRB}$ where: k = Boltzmann constant (J/°K); R = resistance (Ω); T = temperature (°K); B = bandwidth (Hz).

Note 11: Minimum high time for STB1, STB2, STB4. Minimum low time for $\overline{STB3}$.

Note 12: Minimum low time for STB1, STB2, STB4. Minimum high time for $\overline{STB3}$.

PIN FUNCTIONS

LTC1595

V_{REF} (Pin 1): Reference Input.

R_{FB} (Pin 2): Feedback Resistor. Normally tied to the output of the current to voltage converter op amp.

OUT1 (Pin 3): Current Output Pin. Tie to inverting input of current to voltage converter op amp.

GND (Pin 4): Ground Pin.

$\overline{LD}$ (Pin 5): The Serial Interface Load Control Input. When $\overline{LD}$ is pulled low, data is loaded from the shift register into the DAC register, updating the DAC output.

SRI (Pin 6): The Serial Data Input. Data on the SRI pin is latched into the shift register on the rising edge of the serial clock. Data is loaded MSB first.

CLK (Pin 7): The Serial Interface Clock Input.

V_{DD} (Pin 8): The Positive Supply Input. $4.5V \leq V_{DD} \leq 5.5V$. Requires a bypass capacitor to ground.

LTC1596

OUT1 (Pin 1): True Current Output Pin. Tie to inverting input of current to voltage converter op amp.

OUT2 (Pin 2): Complement Current Output Pin. Tie to analog ground.

AGND (Pin 3): Analog Ground Pin.

STB1, STB2, $\overline{STB3}$, STB4 (Pins 4, 8, 10, 11): Serial Interface Clock Inputs. STB1, STB2 and STB4 are rising edge triggered inputs. $\overline{STB3}$ is a falling edge triggered input (see Truth Tables).

$\overline{LD1}$, $\overline{LD2}$ (Pins 5, 9): Serial Interface Load Control Inputs. When $\overline{LD1}$ and $\overline{LD2}$ are pulled low, data is loaded from the shift register into the DAC register, updating the DAC output (see Truth Tables).

SRO (Pin 6): The Output of the Shift Register. Becomes valid on the active edge of the serial clock.

SRI (Pin 7): The Serial Data Input. Data on the SRI pin is latched into the shift register on the active edge of the serial clock. Data is loaded MSB first.

DGND (Pin 12): Digital Ground Pin.

$\overline{CLR}$ (Pin 13): The Clear Pin for the DAC. Clears DAC to zero scale when pulled low. This pin should be tied to V_{DD} for normal operation.

V_{DD} (Pin 14): The Positive Supply Input. $4.5V \leq V_{DD} \leq 5.5V$. Requires a bypass capacitor to ground.

V_{REF} (Pin 15): Reference Input.

R_{FB} (Pin 16): Feedback Resistor. Normally tied to the output of the current to voltage converter op amp.

TRUTH TABLES

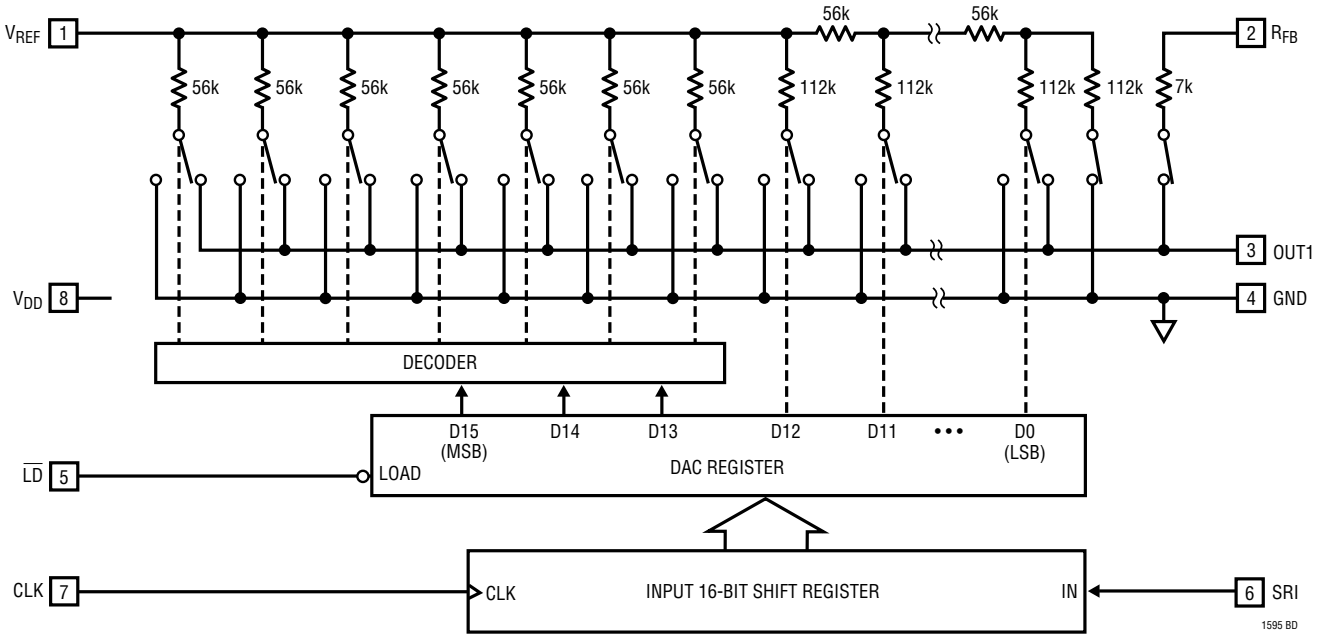
Table 1. LTC1596 Input Register

CONTROL INPUTS				
STB1	STB2	$\overline{STB3}$	STB4	Input Register and SRO Operation
↓	0	1	0	Serial Data Bit on SRI Loaded into Input Register, MSB First
0	↓	1	0	
0	0	↓	0	Data Bit or SRI Appears on SRO Pin After 16 Clocked Bits
0	0	1	↓	
1	X	X	X	No Input Register Operation
X	1	X	X	No SRO Operation
X	X	0	X	
X	X	X	1	

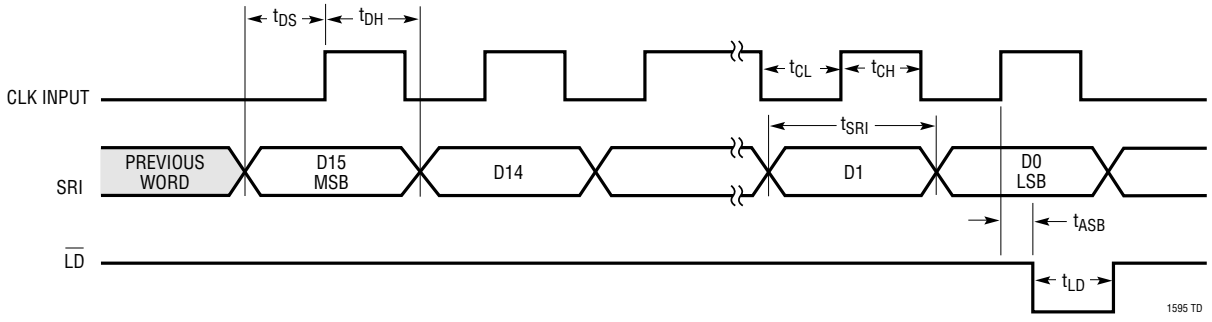
Table 2. LTC1596 DAC Register

CONTROL INPUTS			
$\overline{CLR}$	$\overline{LD1}$	$\overline{LD2}$	DAC Register Operation
0	X	X	Reset DAC Register and Input Register to All 0s (Asynchronous Operation)
1	1	X	No DAC Register Operation
1	X	1	
1	0	0	Load DAC Register with the Contents of Input Register

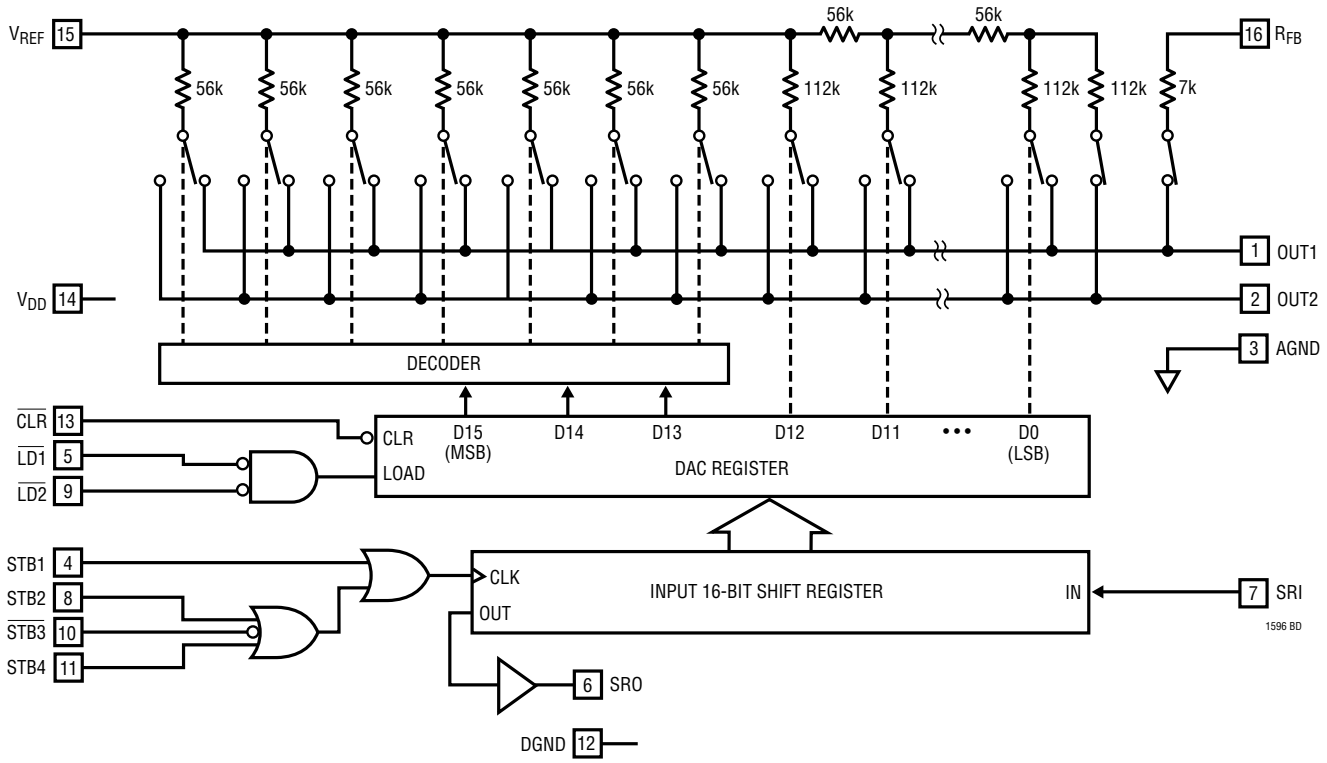
BLOCK DIAGRAM (LTC1595)



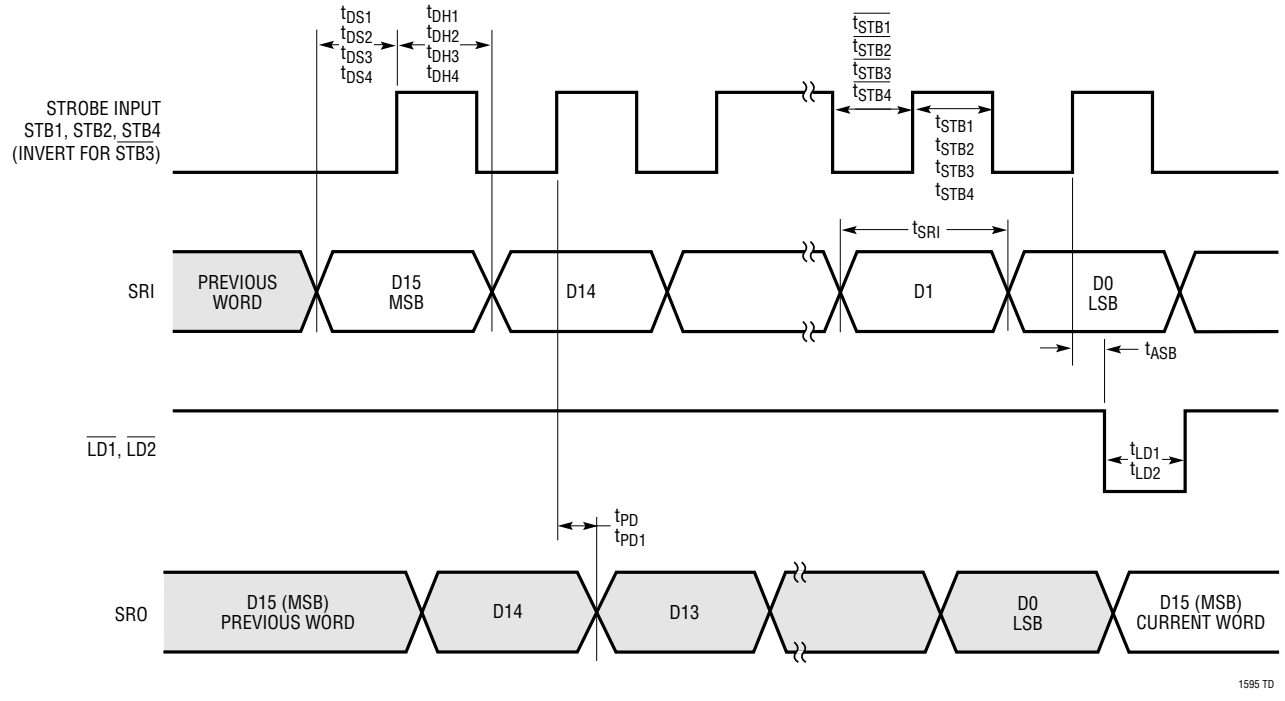
TIMING DIAGRAM (LTC1595)



BLOCK DIAGRAM (LTC1596)



TIMING DIAGRAM (LTC1596)



APPLICATIONS INFORMATION

Description

The LTC1595/LTC1596 are 16-bit multiplying DACs which have serial inputs and current outputs. They use precision R/2R technology to provide exceptional linearity and stability. The devices operate from a single 5V supply and provide ±10V reference input and voltage output ranges when used with an external op amp. These devices have a proprietary deglitcher that reduces glitch energy to below 2nV-s over a 0V to 10V output range.

Serial I/O

The LTC1595/LTC1596 have SPI/MICROWIRE™ compatible serial ports that accept 16-bit serial words. Data is accepted MSB first and loaded with a load pin.

The 8-pin LTC1595 has a 3-wire interface. Data is shifted into the SRI data input on the rising edge of the CLK pin. At the end of the data transfer, data is loaded into the DAC register by pulling the $\overline{LD}$ pin low (see LTC1595 Timing Diagram).

MICROWIRE is a trademark of National Semiconductor Corporation.

The 16-pin LTC1596 can operate in identical fashion to the LTC1595 but offers additional pins for flexibility. Four clock pins are available STB1, STB2, $\overline{STB3}$ and STB4. STB1, STB2 and STB4 operate like the CLK pin of the LTC1595, capturing data on their rising edges. $\overline{STB3}$ captures data on its falling edge (see Truth Table 1).

The LTC1596 has two load pins, $\overline{LD1}$ and $\overline{LD2}$. To load data, both pins must be taken low. If one of the pins is grounded, the other pin will operate identically to LTC1595's $\overline{LD}$ pin. An asynchronous clear input ($\overline{CLR}$) resets the LTC1596 to zero scale when pulled low (see Truth Table 2).

The LTC1596 also has a data output pin SRO that can be connected to the SRI input of another DAC to daisy-chain multiple DACs on one 3-wire interface (see LTC1596 Timing Diagram).

2-Quadrant Multiplying Mode (V_{OUT} = 0V to $-V_{REF}$)

The LTC1595/LTC1596 can be used with a single op amp to provide 2-quadrant multiplying operation as shown in Figure 1. With a fixed –10V reference, the circuits shown give a precision unipolar 0V to 10V output swing.

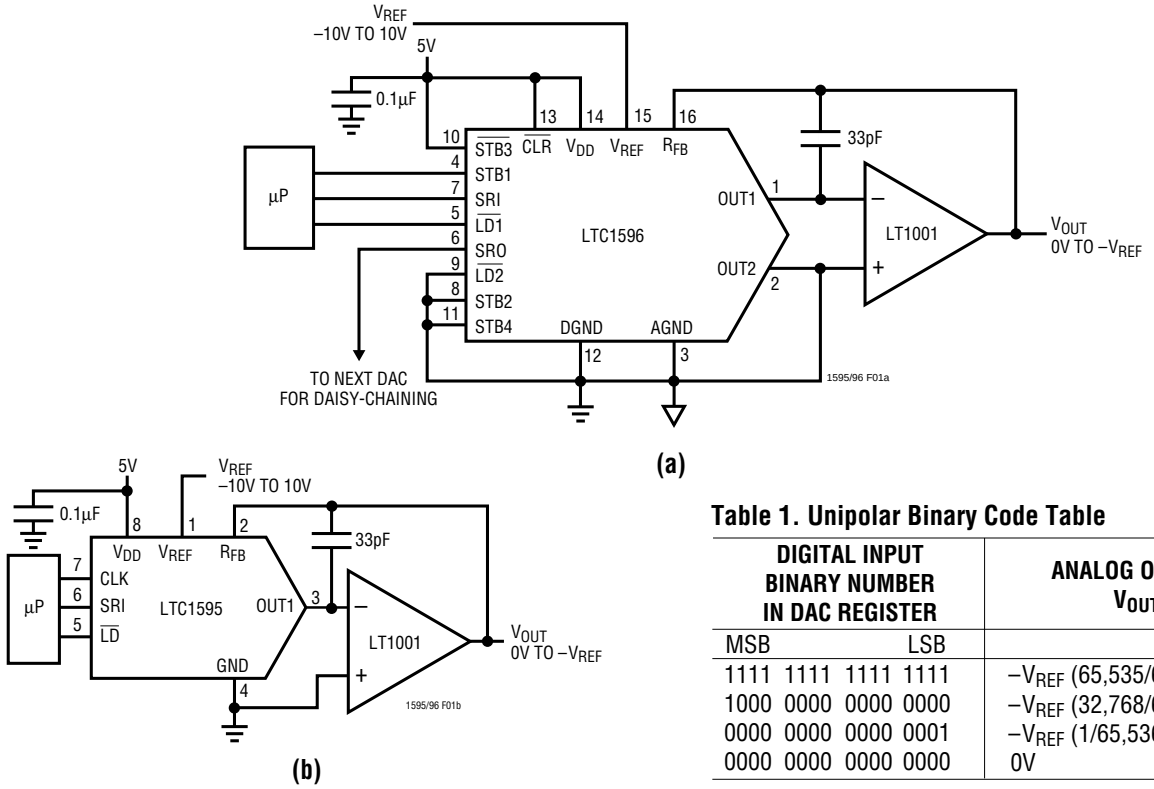


Table 1. Unipolar Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER	ANALOG OUTPUT V_{OUT}
MSB LSB	
1111 1111 1111 1111	$-V_{REF}$ (65,535/65,536)
1000 0000 0000 0000	$-V_{REF}$ (32,768/65,536) = $-V_{REF}/2$
0000 0000 0000 0001	$-V_{REF}$ (1/65,536)
0000 0000 0000 0000	0V

Figure 1. Unipolar Operation (2-Quadrant Multiplication) V_{OUT} = 0V to $-V_{REF}$

APPLICATIONS INFORMATION

4-Quadrant Multiplying Mode ($V_{OUT} = -V_{REF}$ to V_{REF})

The LTC1595/LTC1596 can be used with a dual op amp and three external resistors to provide 4-quadrant multiplying operation as shown in Figure 2. With a fixed 10V reference, the circuits shown give a precision bipolar –10V to 10V output swing.

Op Amp Selection

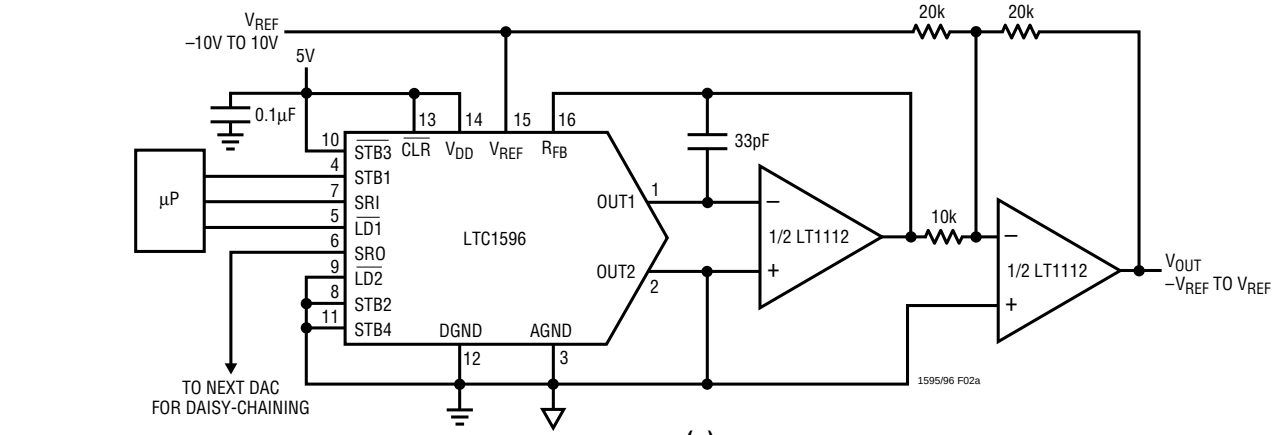
Because of the extremely high accuracy of the 16-bit LTC1595/LTC1596, thought should be given to op amp selection in order to achieve the exceptional performance of which the part is capable. Fortunately, the sensitivity of INL and DNL to op amp offset has been greatly reduced compared to previous generations of multiplying DACs.

Op amp offset will contribute mostly to output offset and gain and will have minimal effect on INL and DNL. For example, a 500µV op amp offset will cause about 0.55LSB INL degradation and 0.15LSB DNL degradation with a 10V full-scale range. The main effects of op amp offset will be a degradation of zero-scale error equal to the op amp offset, and a degradation of full-scale error equal to twice the op amp offset. For example, the same 500µV op amp offset will cause a 3.3LSB zero-scale error and a 6.5LSB full-scale error with a 10V full-scale range.

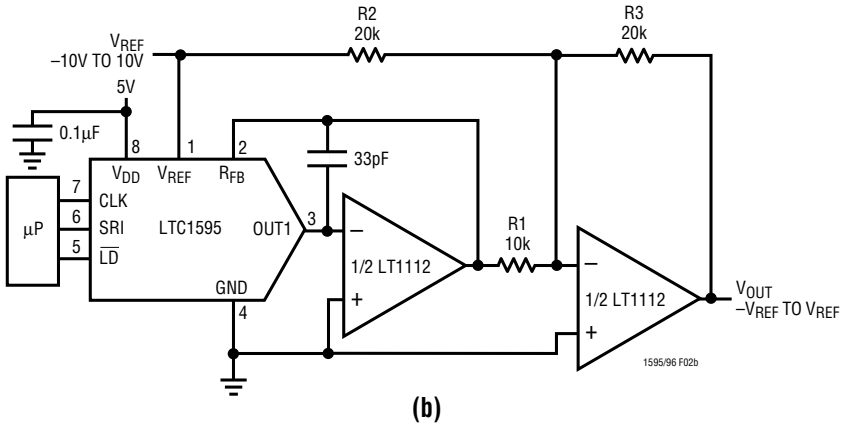
Op amp input bias current (I_{BIAS}) contributes only a zero-scale error equal to $I_{BIAS}(R_{FB}) = I_{BIAS}(R_{REF}) = I_{BIAS}(7k)$.

Grounding

As with any high resolution converter, clean grounding is important. A low impedance analog ground plane and star grounding should be used. I_{OUT2} (LTC1596) and GND (LTC1595) must be tied to the star ground with as low a resistance as possible.



(a)



(b)

Table 2. Bipolar Offset Binary Code Table

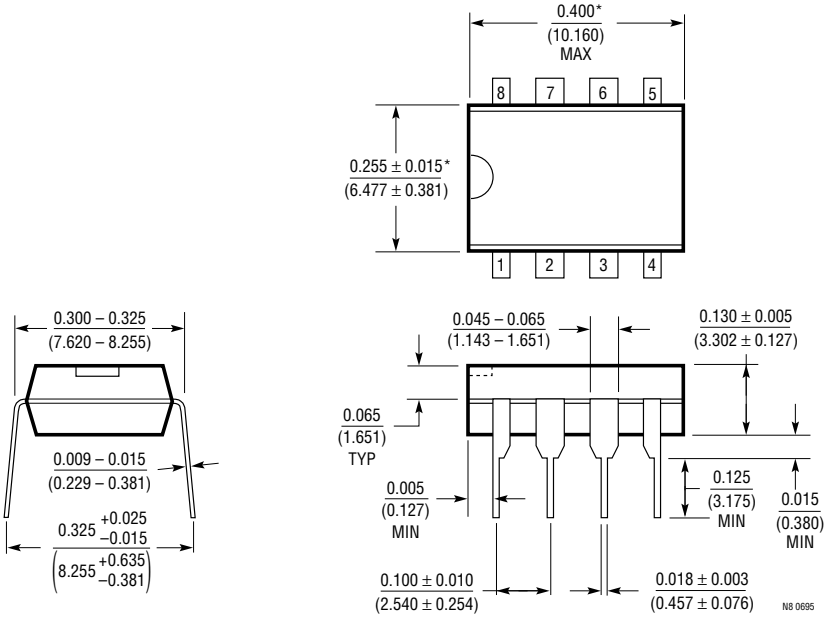
DIGITAL INPUT BINARY NUMBER IN DAC REGISTER	ANALOG OUTPUT V_{OUT}
MSB LSB	
1111 1111 1111 1111	V_{REF} (32,767/32,768)
1000 0000 0000 0000	V_{REF} (1/32,768)
1000 0000 0000 0001	0V
0111 1111 1111 1111	$-V_{REF}$ (1/32,768)
0000 0000 0000 0000	$-V_{REF}$

Figure 2. Bipolar Operation (4-Quadrant Multiplication) $V_{OUT} = -V_{REF}$ to V_{REF}

PACKAGE DESCRIPTION

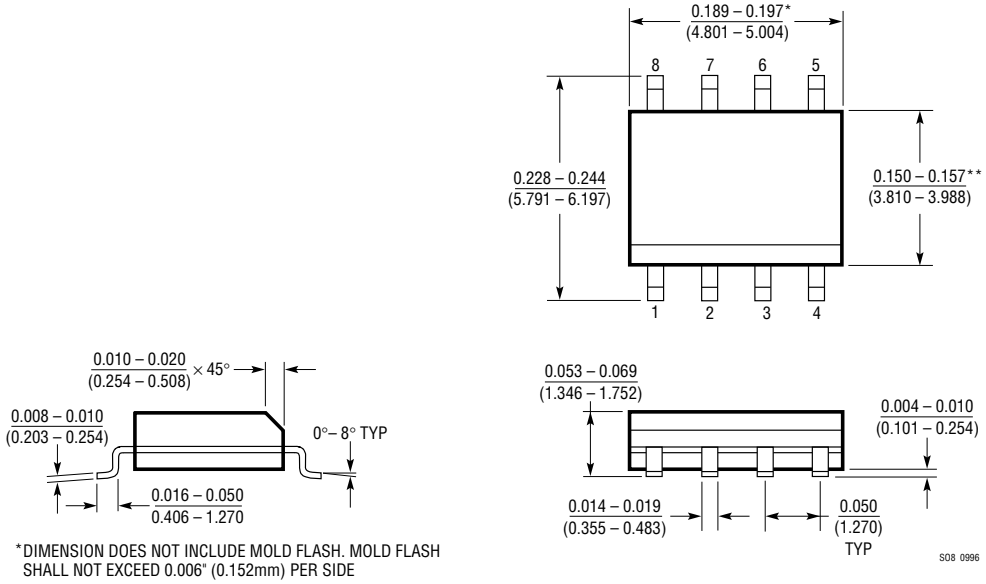
Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



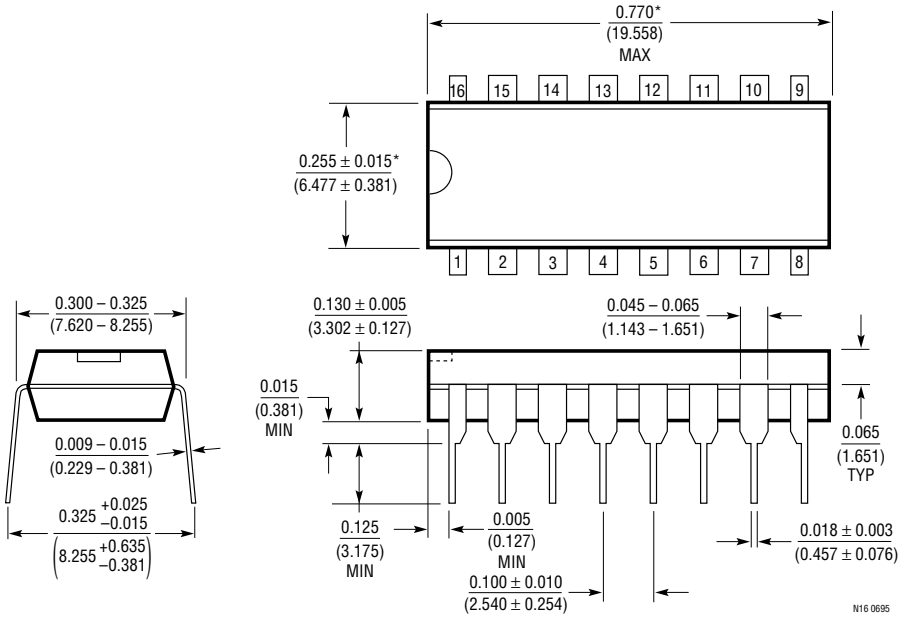
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION

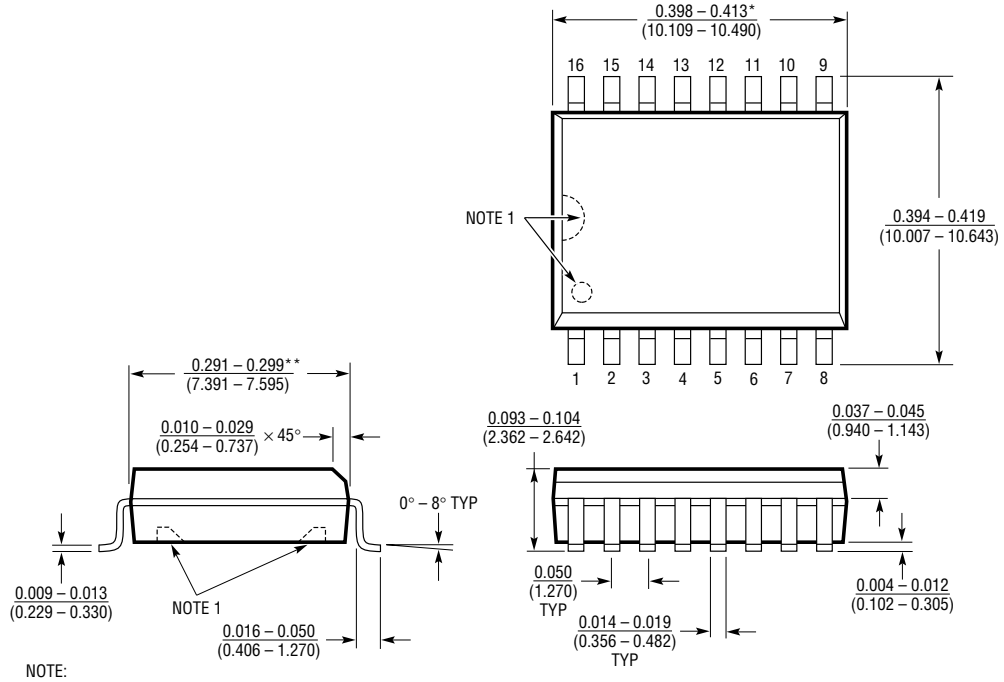
Dimensions in inches (millimeters) unless otherwise noted.

N Package
16-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

SW Package
16-Lead Plastic Small Outline (Wide 0.300)
(LTC DWG # 05-08-1620)



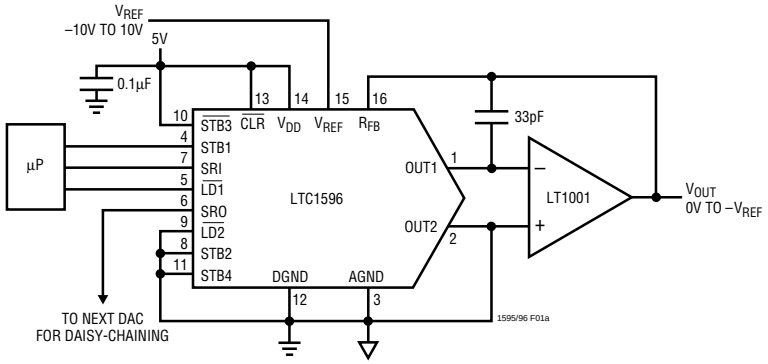
NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

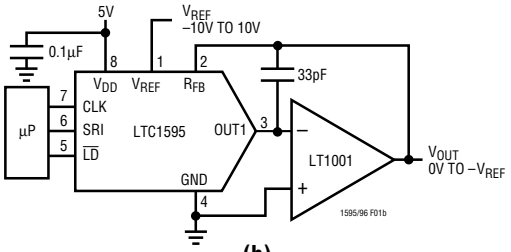
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATIONS

Unipolar Operation (2-Quadrant Multiplication) V_{OUT} = 0V to $-V_{REF}$

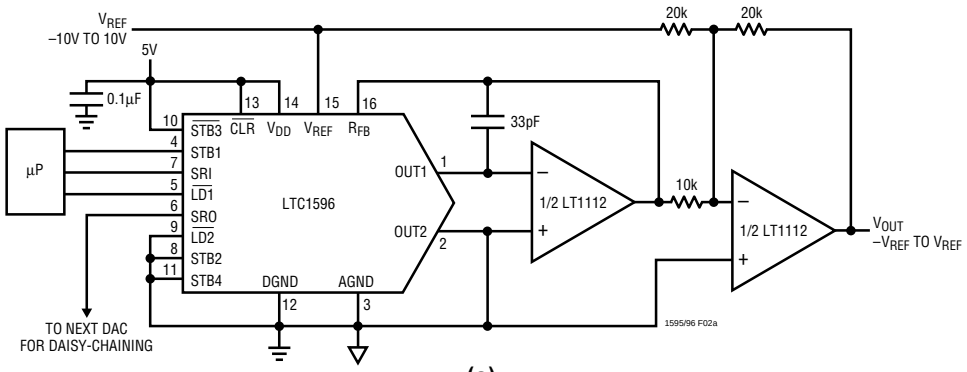


(a)

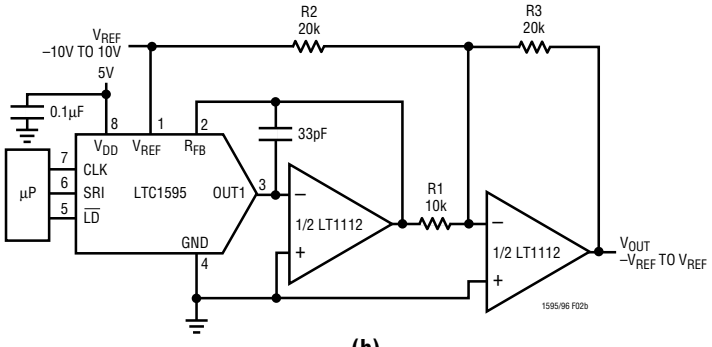


(b)

Bipolar Operation (4-Quadrant Multiplication) $V_{OUT} = -V_{REF}$ to V_{REF}



(a)



(b)

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1590	Dual Serial I/O Multiplying I_{OUT} 12-Bit DAC	16-Pin SO and PDIP, SPI Interface
LTC7541A	Parallel I/O Multiplying I_{OUT} 12-Bit DAC	12-Bit Wide Parallel Input
LTC7543/LTC8143	Serial I/O Multiplying I_{OUT} 12-Bit DACs	Clear Pin and Serial Data Output (LTC8143)
LTC7545A	Parallel I/O Multiplying I_{OUT} 12-Bit DAC	12-Bit Wide Latched Parallel Input
LTC8043	Serial I/O Multiplying I_{OUT} 12-Bit DAC	8-Pin SO and PDIP

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