

LH5324C00

CMOS 24M (1.5M × 16) MROM

FEATURES

- 1,572,864 × 16 bit organization
- Access time: 120 ns (MAX.)
- Supply current:
 - Operating: 80 mA (MAX.)
 - Standby: 100 μA (MAX.)
- TTL compatible I/O
- Three-state output
- Single +5 V Power supply
- Static operation
- When the address input at both A₁₉ and A₂₀ is high level, outputs become high impedance irrespective of \overline{CE} or \overline{OE} .
- Package:
 - 42-pin, 600-mil DIP
- Others:
 - Non programmable
 - Not designed or rated as radiation hardened
 - CMOS process (P type silicon substrate)

PIN CONNECTIONS

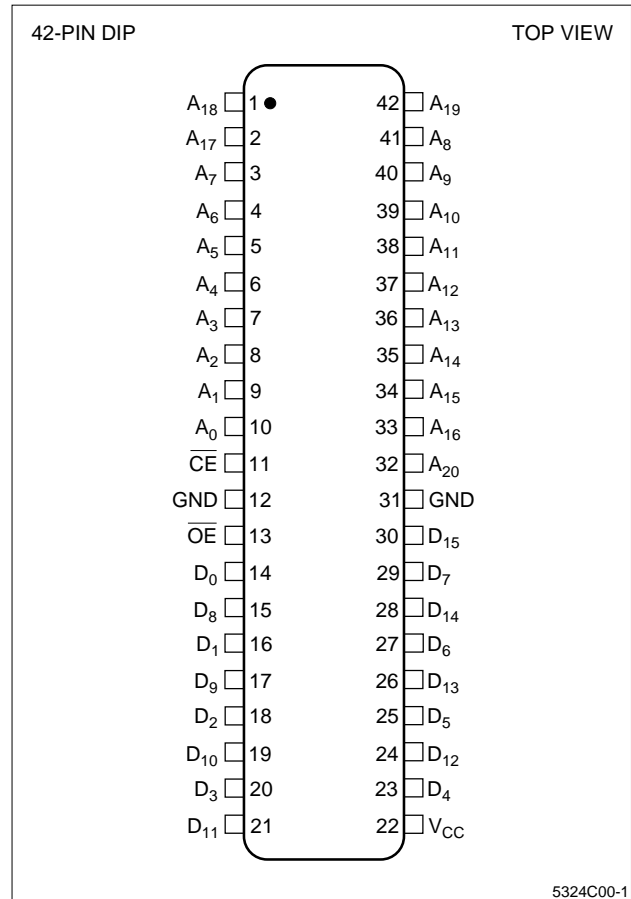
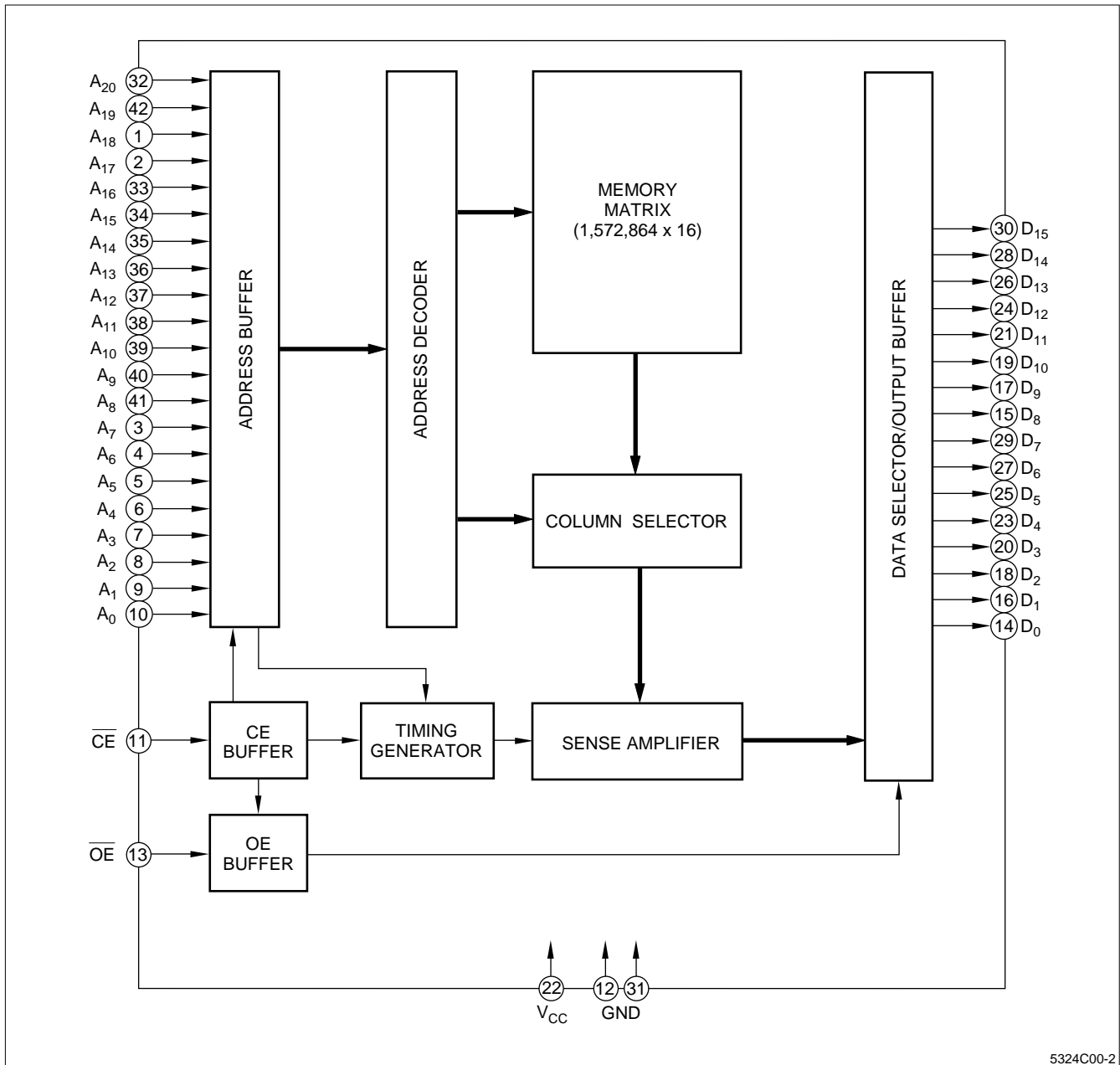


Figure 1. Pin Connections

DESCRIPTION

The LH5324C00 is a 24M-bit mask-programmable ROM organized as 1,572,864 × 16 bits. It is fabricated using silicon-gate CMOS process technology.



5324C00-2

Figure 2. LH5324C00 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A ₀ - A ₂₀	Address input
D ₀ - D ₁₅	Data output
CE	Chip enable input

SIGNAL	PIN NAME
OE	Output enable input
V _{CC}	Power supply (+5 V)
GND	Ground

TRUTH TABLE

\overline{CE}	\overline{OE}	A ₀ - A ₁₈	A ₁₉	A ₂₀	DATA OUTPUT	SUPPLY CURRENT
					D ₀ - D ₁₅	
H	X	X	X	X	High-Z	Standby (I _{SB})
L	H	X	X	X	High-Z	Operating (I _{CC})
L	L	X	L	L	Output	Operating (I _{CC})
L	L	X	L	H	Output	Operating (I _{CC})
L	L	X	H	L	Output	Operating (I _{CC})
L	L	X	H	H	High-Z	Operating (I _{CC})

NOTES:

1. X = Don't care; High-Z = High-impedance
2. When the address inputs become HIGH to both A₁₉ and A₂₀, the data does not exist in this address area, the data outputs become "High Impedance".

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V _{CC}	-0.3 to +7.0	V
Input voltage	V _{IN}	-0.3 to V _{CC} + 0.3	V
Output voltage	V _{OUT}	-0.3 to V _{CC} + 0.3	V
Operating temperature	T _{OPR}	0 to +70	°C
Storage temperature	T _{STG}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V _{CC}	4.5	5.0	5.5	V

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V _{IH}	—	2.2	V _{CC} + 0.3	V	—
Input 'Low' voltage	V _{IL}	—	-0.3	0.8	V	—
Output 'High' voltage	V _{OH}	I _{OH} = -400 μA	2.4	—	V	—
Output 'Low' voltage	V _{OL}	I _{OL} = 2.0 mA	—	0.4	V	—
Input leakage current	I _{LI}	V _{IN} = 0 V to V _{CC}	—	10	μA	—
Output leakage current	I _{LO}	V _{OUT} = 0 V to V _{CC}	—	10	μA	1
Operating current	I _{CC1}	t _{RC} = 120 ns	—	80	mA	2
	I _{CC2}	t _{RC} = 1 μs	—	70		
Standby current	I _{SB1}	$\overline{CE} = V_{IH}$	—	2	mA	—
	I _{SB2}	$\overline{CE} = V_{CC} - 0.2 V$	—	100		
Input capacitance	C _{IN}	f = 1 MHz, t _A = 25°C	—	10	pF	—
Output capacitance	C _{OUT}		—	10		

NOTES:

1. $\overline{CE} = V_{IH}$, $\overline{OE} = V_{IH}$
2. V_{IN} = V_{IH} or V_{IL}, $\overline{CE} = V_{IL}$, output is open

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = +5\text{ V} \pm 10\%$, $T_A = 0$ to $+70^\circ\text{C}$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	120	—	ns	—
Address access time	t_{AA}	—	120	ns	—
Chip enable access time	t_{ACE}	—	120	ns	—
Output enable delay time	t_{OE}	—	60	ns	—
Output hold time	t_{OH}	0	—	ns	—
Output floating time	t_{CHZ}	—	50	ns	1
	t_{OHZ}	—	50	ns	
	t_{AHZ}	—	60	ns	

NOTE:

1. Determined by the time for the output to be opened. (Irrespective of output voltage)

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input signal rise time	10 ns
Input signal fall time	10 ns
Input reference level	1.5 V
Output reference level	1.5 V
Output load condition	1TTL + 100 pF

NOTE:

It is recommended that a decoupling capacitor be connected between V_{CC} and GND-Pin.

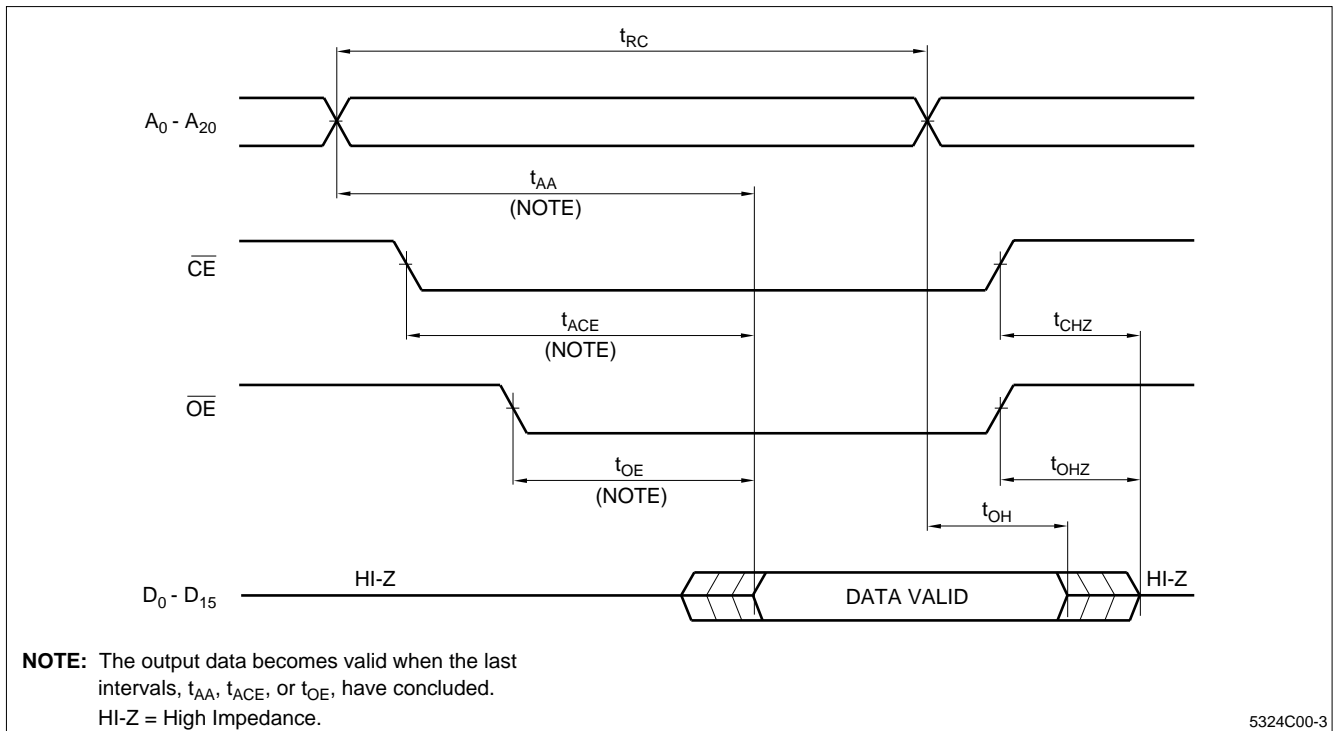


Figure 3. Byte Mode

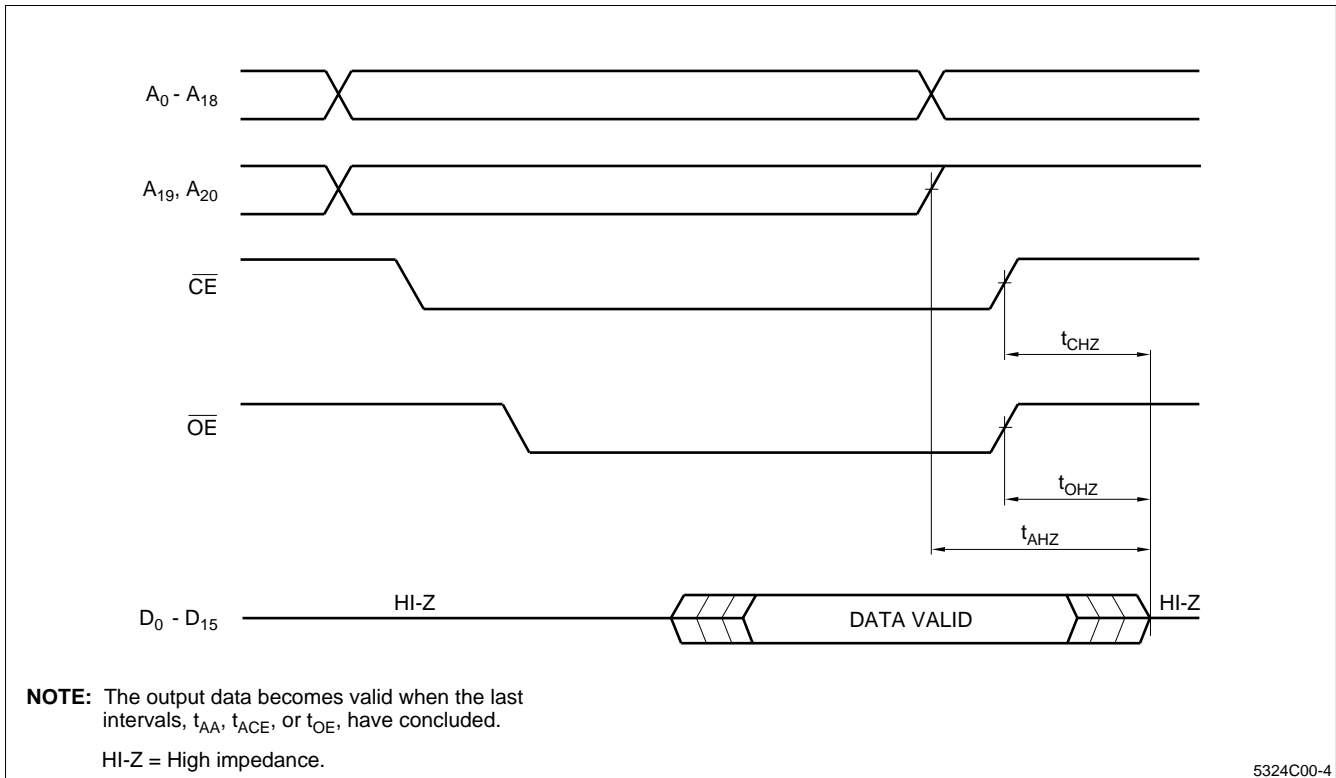
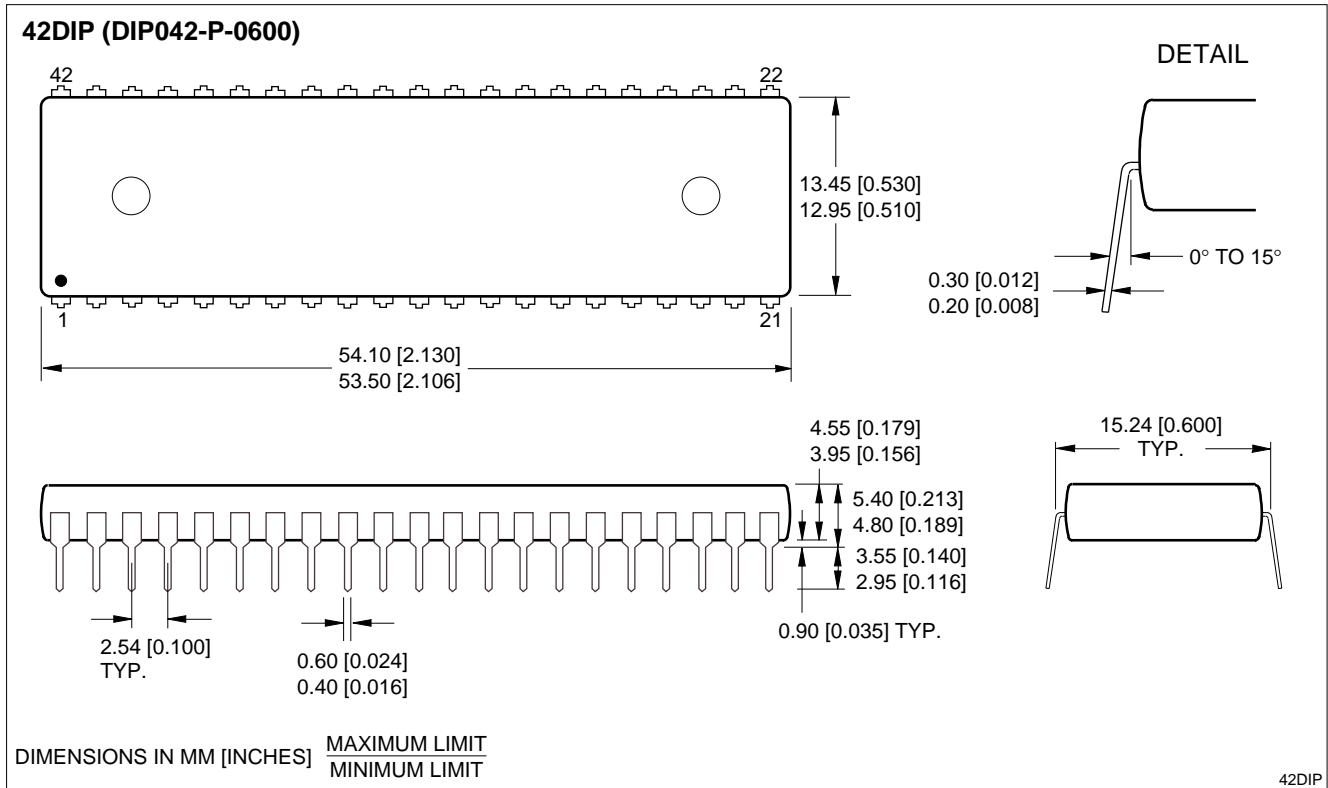


Figure 4. Word Mode

PACKAGE DIAGRAM



ORDERING INFORMATION

