KS0670

8 BIT 384 / 402 CHANNEL TFT-LCD SOURCE DRIVER

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Ver. 0.0

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KS0670 Specification Revision History		
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0.0	Original	Aug.1999

CONTENTS

INTRODUCTION

The KS0670 is a 384 / 402 channel output, TFT-LCD source driver for an 256 gray scale LCD panel. Data input is based on digital input consisting of 8 bits by 6 dots, which can realize a full-color display of 16,700,000 color by output of 256 values gamma-corrected.

This device has an internal D/A (Digital-to-Analog) converter for each output and 16 (8-by-2) reference voltages. Because the output dynamic range is as large as 7.8 - 14.8 Vp-p, it is unnecessary to operate level inversion of the LCD's common electrode. Besides, to be able to deal with dot-line inversion when mounted on a single-side, output gray scale voltages with different polarity can be output to the odd number output pins and the even output pins.

KS0670 can be adopted to larger panel, and SHL (shift direction selection) pin makes the use of the LCD panel connection conveniently. Maximum operation clock frequency is 75 MHz at 3.0 V logic operation, single edge and it can be applied to the TFT-LCD panel of UXGA standard.

FEATURES

- TFT active matrix LCD source driver LSI
- 256G/S is possible through 16 (8 by 2) reference voltages and D/A converter
- Both dot inversion display and N-line inversion display are possible
- CMOS level input
- Compatible with gamma-correction
- Input data inversion function (DATPOL1,2)
- Single edge, Double edge compatible (DEC)
- Logic supply voltage: 2.5 - 3.6 V
- LCD driver supply voltage: 8.0 - 15.0 V
- Output dynamic range: 7.8 - 14.8 Vp-p
- Maximum operating frequency: fMAX = 75 MHz
  (internal data transmission rate at 3.0 V operation, single edge)
- Output: 384 / 402 outputs
- TCP

BLOCK DIAGRAM

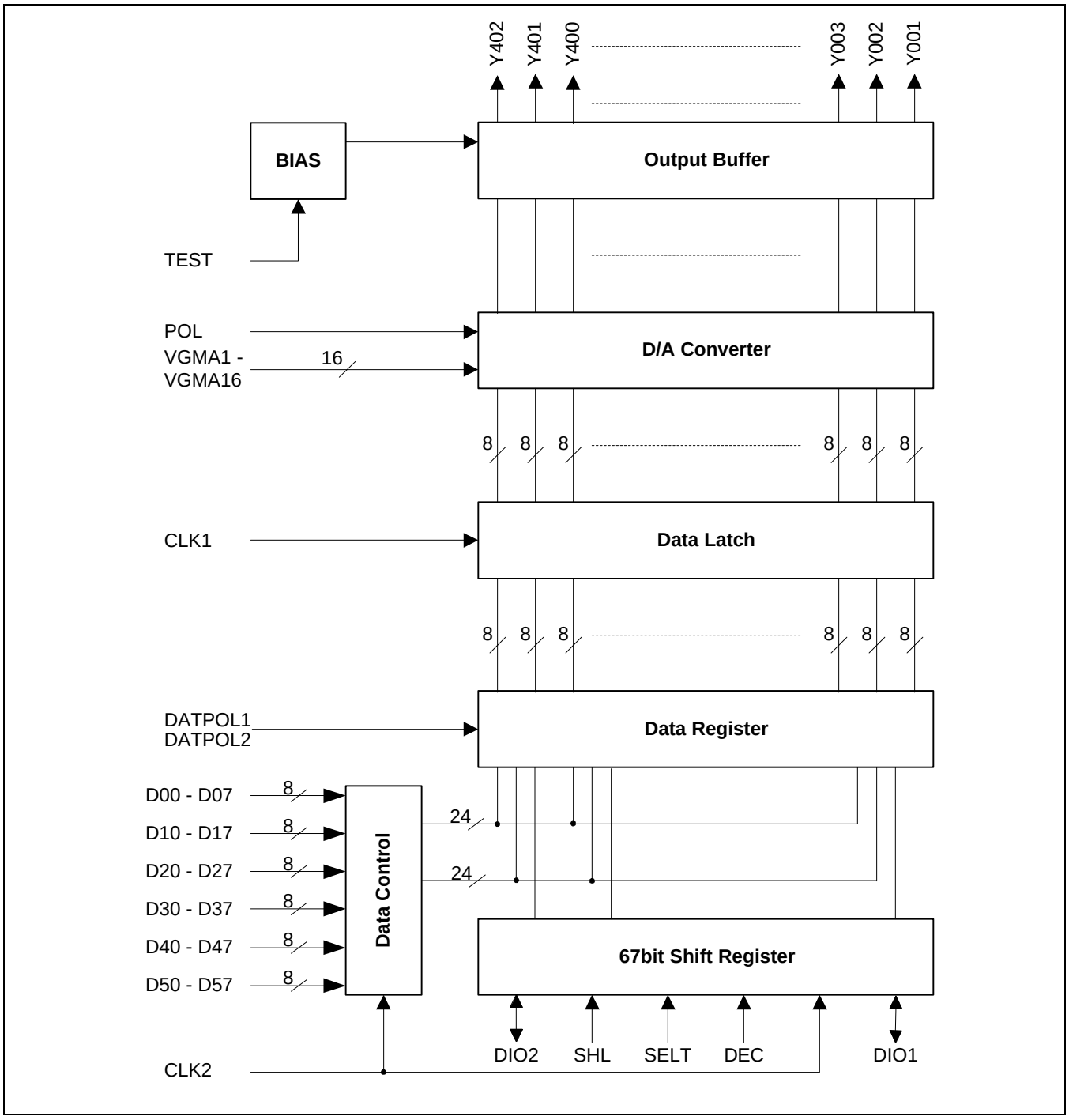

Figure 1. KS0670 Block Diagram

PIN ASSIGNMENTS

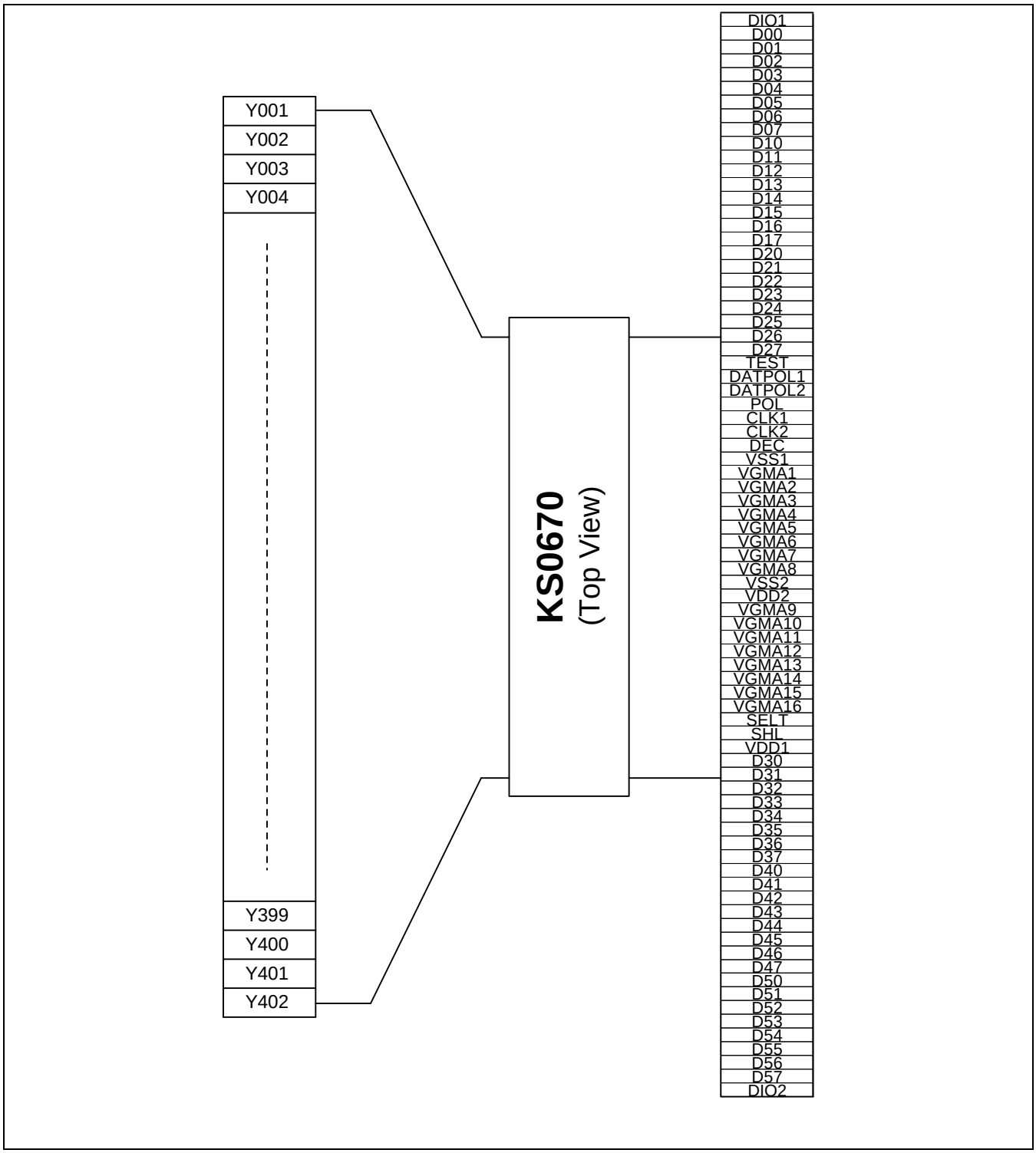

Figure 2. KS0670 Pin Assignments

PIN DESCRIPTIONS

Symbol	Pin Name	Description
VDD1	Logic power supply	2.5 - 3.6 V
VDD2	Driver power supply	8.0 - 15.0 V
VSS1	Logic ground	Ground (0 V)
VSS2	Driver ground	Ground (0 V)
Y1 - Y402	Driver outputs	The D/A converted 256 gray-scale analog voltage is output.
D0<0:7> - D5<0:7>	Display data input	The display data is input with a width of 48 bits, gray-scale data (8 bits) by 6 dots (R,G,B) DX0: LSB, DX7: MSB
SHL	Shift direction control input	This pin controls the direction of shift register in cascade connection. The shift direction of the shift registers is as follows. SHL = H: DIO1 input, Y1 → Y402, DIO2 output SHL = L: DIO2 input, Y402 → Y1, DIO1 output
DIO1	Start pulse input/output	SHL = H: Used as the start pulse input pin. SHL = L: Used as the start pulse output pin.
DIO2	Start pulse input/output	SHL = H: Used as the start pulse output pin. SHL = L: Used as the start pulse input pin.
DATPOL1 DATPOL2	Data inversion input	DATPOL1,2 = L: Display data is not inverted DATPOL1 = H: Display data of D0<0:7> - D2<0:7> is inverted DATPOL2 = H: Display data of D3<0:7> - D5<0:7> is inverted
POL	Polarity input	POL = H: The reference voltage for odd number outputs are VGMA9 – VGMA16 and those for even number outputs are VGMA1 – VGMA8. POL = L: The reference voltage for odd number outputs are VGMA1 – VGMA8 and those for even number outputs are VGMA9 – VGMA16.
CLK2	Shift clock input	Refer to the shift register's shift clock input. When DEC is Low, the display data is loaded to the data register at the rising edge of CLK2.When DEC is High, the display data is loaded to the data register at the rising and falling edge of CLK2.
CLK1	Latch input	Latches the contents of the data register at rising edge and transfers them to the D/A converter. Also, after CLK1 input, clears the internal shift register contents. After 1 pulse input on start, operates normally. CLK1 input timing refers to the "Relationships between CLK1 start pulse (DIO1, DIO2) and blanking period" of the switching characteristic waveform. Outputs the G/S data at falling edge.
VGMA1 – VGMA16	Gamma corrected power supplies	Input the gamma corrected power supplies from external source. VDD2 > VGMA1 > VGMA2 > …… > VGMA15 > VGMA16 > VSS2 Keep gray-scale power supply unchanged during the gray-scale voltage output.
SELT	Output selection input	SELT = L: 384 Output (Y193 - Y210 are disabled), SELT = H: 402 Output
DEC	Double edge selection input	DEC = L: Single Edge, the display data is loaded to the data register at the rising edge of CLK2. DEC = H: Double Edge, the display data is loaded to the data register at the rising and falling edge of CLK2.
TEST	Test input	TEST = L: Normal operation mode TEST = H: Test mode (OP AMP CUT-OFF, Rpd = 10kΩ)

OPERATION DESCRIPTION

DISPLAY DATA TRANSFER

(1) DEC = ”L”
When DIO1 (or DIO2) pulse is loaded into internal latch on the rising edge of CLK2, DIO1 (or DIO2) pulse enables the operation of data transfer, so display data is valid on the next rising edge of CLK2. Once all the data of 402 (or 384) channels is loaded into internal latch, it goes into stand-by state automatically, and any new data is not accepted even though CLK2 is provided until next DIO1 (or DIO2) input. When next DIO1 (or DIO2) is provided, new display data is valid on the 2nd rising edge of CLK2 after the rising edge of DIO1 (or DIO2).

(2) DEC = ”H”
When DIO1 (or DIO2) pulse is loaded into internal latch on the rising (or falling) edge of CLK2, DIO1 (or DIO2) pulse enables the operation of data transfer. display data is valid on the next falling (or rising) edge of CLK2. Once all the data of 402 (or 384) channels is loaded into internal latch, it goes into stand-by state automatically, and any new data is not accepted even though CLK2 is provided until next DIO1 (or DIO2) input. When next DIO1 (or DIO2) is provided, new display data is valid on the 2nd edge of CLK2 after the rising edge of DIO1 (or DIO2).

EXTENSION OF OUTPUT

Output pin can be adjusted to an extended screen by cascade connection.

(1) SHL = "L"
Connect DIO1 pin of previous stage to the DIO2 pin of next stage and all the input pins except DIO1 and DIO2 are connected together in each device.

(2) SHL = "H"
Connect DIO2 pin of previous stage to the DIO1 pin of next stage and all the input pins except DIO2 and DIO1 are connected together in each device.

RELATIONSHIP BETWEEN INPUT DATA VALUE AND OUTPUT VOLTAGE

The LCD drive output voltages are determined by the input data and 16 (8 by 2) gamma corrected power supplies (VGMA1 - VGMA16). Besides, to be able to deal with dot line inversion when mounted on a single-side, gradation voltages with different polarity can be output to the odd number output pins and the even number output pins. Among 8-by-2 gamma corrected voltages, input gray-scale voltages of the same polarity with respect to the common voltage, for the respective 8 gamma corrected voltages of VGMA1 - VGMA8 and VGMA9 - VGMA16.

SHL = H

OUTPUT	Y1	Y2	Y3	.....	Y400	Y401	Y402
-	First			→	Last		
DATA	D00 - D07	D10 - D17	D20 - D27	.....	D30 - D37	D40 - D47	D50 - D57

SHL = L

OUTPUT	Y1	Y2	Y3	.....	Y400	Y401	Y402
-	Last			←	First		
DATA	D00 - D07	D10 - D17	D20 - D27	.....	D30 - D37	D40 - D47	D50 - D57

Figure 3. Relationship between Shift Direction and Output Data

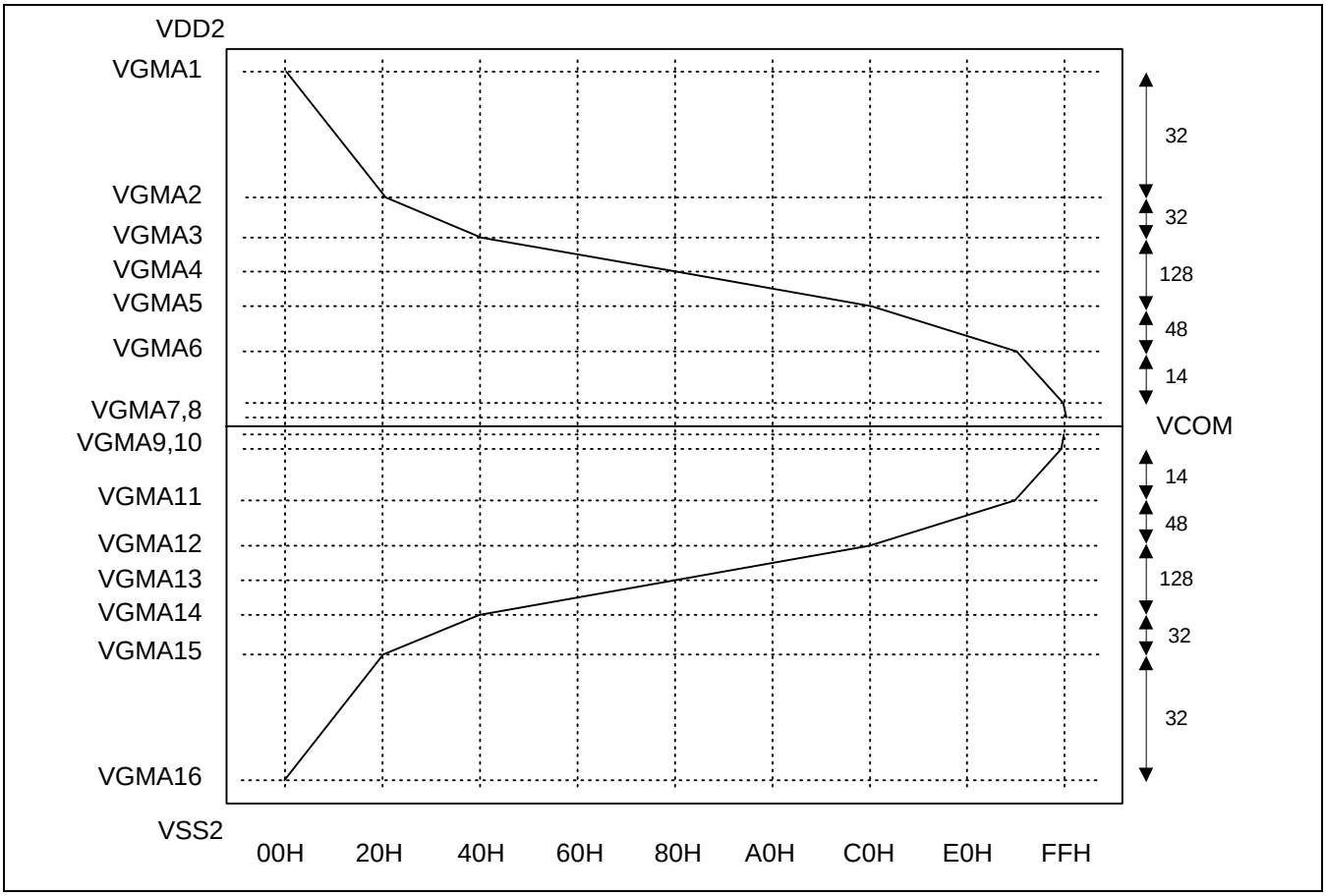

Figure 4. Gamma Correction Curve

Table 1. Resistor Strings (R0 - R254, unit: Ω)

Name	Value	Name	Value	Name	Value	Name	Value
R0	218	R32	70	R64	32	R96	32
R1	218	R33	70	R65	32	R97	32
R2	218	R34	70	R66	32	R98	32
R3	218	R35	70	R67	32	R99	32
R4	218	R36	70	R68	32	R100	32
R5	218	R37	70	R69	32	R101	32
R6	218	R38	70	R70	32	R102	32
R7	218	R39	70	R71	32	R103	32
R8	218	R40	70	R72	32	R104	32
R9	218	R41	70	R73	32	R105	32
R10	218	R42	70	R74	32	R106	32
R11	218	R43	70	R75	32	R107	32
R12	218	R44	70	R76	32	R108	32
R13	218	R45	70	R77	32	R109	32
R14	218	R46	70	R78	32	R110	32
R15	218	R47	70	R79	32	R111	32
R16	218	R48	70	R80	32	R112	32
R17	218	R49	70	R81	32	R113	32
R18	218	R50	70	R82	32	R114	32
R19	218	R15	70	R83	32	R115	32
R20	218	R52	70	R84	32	R116	32
R21	218	R53	70	R85	32	R117	32
R22	218	R54	70	R86	32	R118	32
R23	218	R55	70	R87	32	R119	32
R24	218	R56	70	R88	32	R120	32
R25	218	R57	70	R89	32	R121	32
R26	218	R58	70	R90	32	R122	32
R27	218	R59	70	R91	32	R123	32
R28	218	R60	70	R92	32	R124	32
R29	218	R61	70	R93	32	R125	32
R30	218	R62	70	R94	32	R126	32
R31	218	R63	70	R95	32	R127	32

Table 1. Resistor Strings (R0 - R254, unit: Ω) (Continued)

Name	Value	Name	Value	Name	Value	Name	Value
R128	32	R160	32	R192	50	R224	50
R129	32	R161	32	R193	50	R225	50
R130	32	R162	32	R194	50	R226	50
R131	32	R163	32	R195	50	R227	50
R132	32	R164	32	R196	50	R228	50
R133	32	R165	32	R197	50	R229	50
R134	32	R166	32	R198	50	R230	50
R135	32	R167	32	R199	50	R231	50
R136	32	R168	32	R200	50	R232	50
R137	32	R169	32	R201	50	R233	50
R138	32	R170	32	R202	50	R234	50
R139	32	R171	32	R203	50	R235	50
R140	32	R172	32	R204	50	R236	50
R141	32	R173	32	R205	50	R237	50
R142	32	R174	32	R206	50	R238	50
R143	32	R175	32	R207	50	R239	50
R144	32	R176	32	R208	50	R240	200
R145	32	R177	32	R209	50	R241	200
R146	32	R178	32	R210	50	R242	200
R147	32	R179	32	R211	50	R243	200
R148	32	R180	32	R212	50	R244	200
R149	32	R181	32	R213	50	R245	200
R150	32	R182	32	R214	50	R246	200
R151	32	R183	32	R215	50	R247	200
R152	32	R184	32	R216	50	R248	200
R153	32	R185	32	R217	50	R249	200
R154	32	R186	32	R218	50	R250	200
R155	32	R187	32	R219	50	R251	200
R156	32	R188	32	R220	50	R252	200
R157	32	R189	32	R221	50	R253	200
R158	32	R190	32	R222	50	R254	930
R159	32	R191	32	R223	50		

Table 2. Relationship between Input Data and Output Voltage Value

Input data	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
00H	0	0	0	0	0	0	0	0	VH0	VGMA1
01H	0	0	0	0	0	0	0	1	VH1	VGMA1 + (VGMA2 - VGMA1) × 218 / 6976
:				:					:	:
18H	0	0	0	1	1	0	0	0	VH24	VGMA1 + (VGMA2 - VGMA1) × (218 × 24) / 6976
:				:					:	:
1FH	0	0	0	1	1	1	1	1	VH31	VGMA1 + (VGMA2 - VGMA1) × (218 × 31) / 6976
20H	0	0	1	0	0	0	0	0	VH32	VGMA2
21H	0	0	1	0	0	0	0	1	VH33	VGMA2 + (VGMA3 - VGMA2) × (70 × 1) / 2240
:				:					:	:
28H	0	0	1	0	1	0	0	0	VH40	VGMA2 + (VGMA3 - VGMA2) × (70 × 8) / 2240
29H	0	0	1	0	1	0	0	1	VH41	VGMA2 + (VGMA3 - VGMA2) × (70 × 9) / 2240
:				:					:	:
3FH	0	0	1	1	1	1	1	1	VH63	VGMA2 + (VGMA3 - VGMA2) × (70 × 31) / 2240
40H	0	1	0	0	0	0	0	0	VH64	VGMA3
41H	0	1	0	0	0	0	0	1	VH65	VGMA3 + (VGMA4 - VGMA3) × (32 × 1) / 2048
:				:					:	:
60H	0	1	1	0	0	0	0	0	VH96	VGMA3 + (VGMA4 - VGMA3) × (32 × 32) / 2048
61H	0	1	1	0	0	0	0	1	VH97	VGMA3 + (VGMA4 - VGMA3) × (32 × 33) / 2048
:				:					:	:
7FH	0	1	1	1	1	1	1	1	VH127	VGMA3 + (VGMA4 – VGMA3) × (32 × 63) / 2048
80H	1	0	0	0	0	0	0	0	VH128	VGMA4
81H	1	0	0	0	0	0	0	1	VH129	VGMA4 + (VGMA5 - VGMA4) × (32 × 1) / 2048
:				:					:	:
A0H	1	0	1	0	0	0	0	0	VH160	VGMA4 + (VGMA5 - VGMA4) × (32 × 32) / 2048
A1H	1	0	1	0	0	0	0	1	VH161	VGMA4 + (VGMA5 - VGMA4) × (32 × 33) / 2048
:				:					:	:
BFH	1	0	1	1	1	1	1	1	VH191	VGMA4 + (VGMA5 - VGMA4) × (32 × 63) / 2048
C0H	1	1	0	0	0	0	0	0	VH192	VGMA5
C1H	1	1	0	0	0	0	0	1	VH193	VGMA5 + (VGMA6 - VGMA5) × (50 × 1) / 2400
:				:					:	:
D8H	1	1	0	1	1	0	0	0	VH216	VGMA5 + (VGMA6 - VGMA5) × (50 ×24) / 2400
D9H	1	1	0	1	1	0	0	1	VH217	VGMA5 + (VGMA6 - VGMA5) × (50 × 25) / 2400
:				:					:	:
EFH	1	1	1	0	1	1	1	1	VH239	VGMA5 + (VGMA6 - VGMA5) × (50 × 47) / 2400
F0H	1	1	1	1	0	0	0	0	VH240	VGMA6
F1H	1	1	1	1	0	0	0	1	VH241	VGMA6 + (VGMA7 - VGMA6) × (200 × 1) / 2800
:				:					:	:
F9H	1	1	1	1	1	0	0	1	VH249	VGMA6 + (VGMA7 – VGMA6) × (200 × 9) / 2800
:				:					:	:
FDH	1	1	1	1	1	1	0	1	VH253	VGMA6 + (VGMA7 - VGMA6) × (200 × 13) / 2800
FEH	1	1	1	1	1	1	1	0	VH254	VGMA7
FFH	1	1	1	1	1	1	1	1	VH255	VGMA8

NOTE: VDD2 > VGMA1 > VGMA2 > VGMA3 > VGMA4 > VGMA5 > VGMA6 > VGMA7 > VGMA8

Table 2. Relationship between Input Data and Output Voltage Value (Continued)

Input data	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
00H	0	0	0	0	0	0	0	0	VL0	VGMA16
01H	0	0	0	0	0	0	0	1	VL1	VGMA16 + (VGMA15 - VGMA16) × (218 × 1) / 6976
:				:					:	:
18H	0	0	0	1	1	0	0	0	VL24	VGMA16 + (VGMA15 - VGMA16) × (218 × 24) / 6976
:				:					:	:
1FH	0	0	0	1	1	1	1	1	VL31	VGMA16 + (VGMA15 - VGMA16) × (218 × 31) / 6976
20H	0	0	1	0	0	0	0	0	VL32	VGMA15
21H	0	0	1	0	0	0	0	1	VL33	VGMA15 + (VGMA14 - VGMA15) × (70 × 1) / 2240
:				:					:	:
28H	0	0	1	0	1	0	0	0	VL40	VGMA15 + (VGMA14 - VGMA15) × (70 × 8) / 2240
29H	0	0	1	0	1	0	0	1	VL41	VGMA15 + (VGMA14 - VGMA15) × (70 × 9) / 2240
:				:					:	:
3FH	0	0	1	1	1	1	1	1	VL63	VGMA15 + (VGMA14 - VGMA15) × (70 × 31) / 2240
40H	0	1	0	0	0	0	0	0	VL64	VGMA14
41H	0	1	0	0	0	0	0	1	VL65	VGMA14 + (VGMA13 - VGMA14) × (32 × 1) / 2048
:				:					:	:
60H	0	1	1	0	0	0	0	0	VL96	VGMA14 + (VGMA13 - VGMA14) × (32 × 32) / 2048
61H	0	1	1	0	0	0	0	1	VL97	VGMA14 + (VGMA13 - VGMA14) × (32 × 33) / 2048
:				:					:	:
7FH	0	1	1	1	1	1	1	1	VL127	VGMA14 + (VGMA13 - VGMA14) × (32 × 63) / 2048
80H	1	0	0	0	0	0	0	0	VL128	VGMA13
81H	1	0	0	0	0	0	0	1	VL129	VGMA13 + (VGMA12 - VGMA13) × (32 × 1) / 2048
:				:					:	:
A0H	1	0	1	0	0	0	0	0	VL160	VGMA13 + (VGMA12 - VGMA13) × (32 × 32) / 2048
A1H	1	0	1	0	0	0	0	1	VL161	VGMA13 + (VGMA12 - VGMA13) × (32 × 33) / 2048
:				:					:	:
BFH	1	0	1	1	1	1	1	1	VL191	VGMA13 + (VGMA12 - VGMA13) × (32 × 63) / 2048
C0H	1	1	0	0	0	0	0	0	VL192	VGMA12
C1H	1	1	0	0	0	0	0	1	VL193	VGMA12 + (VGMA11 - VGMA12) × (50 × 1) / 2400
:				:					:	:
D8H	1	1	0	1	1	0	0	0	VL216	VGMA12 + (VGMA11 - VGMA12) × (50 × 24) / 2400
D9H	1	1	0	1	1	0	0	1	VL217	VGMA12 + (VGMA11 - VGMA12) × (50 × 25) / 2400
:				:					:	:
EFH	1	1	1	0	1	1	1	1	VL239	VGMA12 + (VGM11 - VGMA12) × (50 × 47) / 2400
F0H	1	1	1	1	0	0	0	0	VL240	VGMA11
F1H	1	1	1	1	0	0	0	1	VL241	VGMA11 + (VGMA10 - VGMA11) × (200 × 1) / 2800
:				:					:	:
F9H	1	1	1	1	1	0	0	1	VL249	VGMA11 + (VGMA10 - VGMA11) × (200 × 9) / 2800
:				:					:	:
FDH	1	1	1	1	1	1	0	1	VL253	VGMA11 + (VGMA10 - VGMA11) × (200 × 13) / 2800
FEH	1	1	1	1	1	1	1	0	VL254	VGMA10
FFH	1	1	1	1	1	1	1	1	VL255	VGMA9

NOTE: VSS2 < VGMA16 < VGMA15 < VGMA14 < VGMA13 < VGMA12 < VGMA11 < VGMA10 < VGMA9

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings (VSS1 = VSS2 = 0 V)

Parameter	Symbol	Ratings	Unit
Logic supply voltage	VDD1	-0.3 to 5.0	V
Driver supply voltage	VDD2	-0.3 to 16	V
Input voltage	VGMA1 - 16	-0.3 to VDD2+0.3	V
	Others	-0.3 to VDD1+0.3	
Output voltage	DIO1, 2	-0.3 to VDD1+0.3	V
	Y1 – Y402	-0.3 to VDD2+0.3	
Operating power dissipation	Pd	300 (1)	mW
Operation temperature	Top	-20 to 75	°C
Storage temperature	Tstg	-55 to 125	°C

CAUTIONS:

If LSIs are stressed beyond those listed above “absolute maximum ratings”, they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Turn on power order: VDD1 → control signal input → VDD2 → VGMA1 - VGMA16 Turn off power order: VGMA1 - VGMA16 → VDD2 → control signal input → VDD1

RECOMMENDED OPERATION CONDITIONS

Table 4. Recommended Operation Conditions (Ta = -20 to 75 °C, VSS1 = VSS2 = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic supply voltage	VDD1	2.5	3.3	3.6	V
Driver supply voltage	VDD2 (1)	8.0	12.0	15.0	V
Gamma corrected voltage	VGMA1 – VGMA8	0.5 VDD2	-	VDD2 - 0.1	V
	VGMA9 – VGMA16	VSS2 + 0.1	-	0.5 VDD2	V
Driver part output voltage	Vyo	VSS2 + 0.1	-	VDD2 - 0.1	V
Maximum clock frequency (Single edge/Double edge)	fmax	VDD1 = 2.5 V		55 / 40	MHz
		VDD1 = 3.0 V		75 / 55	
Output load capacitance	CL(1)	-	-	200	pF / PIN

NOTE: 1. Relationship between TFT-LCD panel and Pd (Pd ∝ CL * $(VDD2)^2$ * fCLK1)

TFT-LCD panel standard	CL = 140pF	CL = 200pF
SXGA	max. VDD2 = 15 V	max. VDD2 = 13 V
UXGA & WUXGA	max. VDD2 = 14 V	max. VDD2 = 12 V

DC CHARACTERISTICS

Table 5. DC Characteristics (Ta = -20 to 75 °C, VDD1 = 2.5 to 3.6 V, VDD2 = 8 to 15 V, VSS1 = VSS2 = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	VIH	SHL, CLK2, D00 - D57, CLK1, SELT, DATPOL1, DATPOL2, DEC, POL, DIO1 (DIO2)	0.8 VDD1	-	VDD1	V
Low level input voltage	VIL		0	-	0.2 VDD1	
Input leakage current	IL		-1	-	1	µA
High level output voltage	VOH	DIO1 (DIO2), IO = -1.0 mA	VDD1 - 0.5	-	-	V
Low level output voltage	VOL	DIO1 (DIO2), IO = +1.0 mA	-	-	0.5	
Resistor	R0 - R254	Refer to Table 1. Resistor Strings	Rn × 0.7		Rn × 1.3	Ω
Driver output current	IVOH	VDD2 = 10.0 V, Vx = 3.5 V, Vyo = 9.5 V(1)	-	-2.0	-1.0	mA
	IVOL	VDD2 = 10.0 V, Vx = 6.5 V, Vyo = 0.5 V(1)	1.0	2.0	-	mA
Output voltage deviation	ΔVO	VSS2 + 0.1 V to VDD2 - 1.5 V	-	±7	±15	mV
		VDD2 - 1.5 V to VDD2 - 0.1 V	-	±10	±20	
Output RMS voltage deviation	dVrms(2)	Input data: 00H to FFH	-	±3	±10	
Output voltage range	Vyo	Input data: 00H to FFH	VSS2 + 0.1	-	VDD2 – 0.1	V
Logic part dynamic current	IDD1	VDD1 = 3.0 V (3)	-	4.0	7.0	mA
Driver part dynamic current	IDD2	VDD2 = 10 V (4)	-	10.0	15.0	

NOTES:

1. Vyo is the output voltage of analog output pins Y1 to Y402.
   Vx is the voltage applied to analog output pins Y1 to Y402.
2. dVrms is a maximum deviation value from ideal difference between high output and low output at the same gray scale.
3. CLK1 period is defined to be 15.6 µs at fCLK2 = 54 MHz, DEC = L, data pattern = 10101010 (checkerboard pattern), Ta = 25 °C.
4, Yout Load Condition

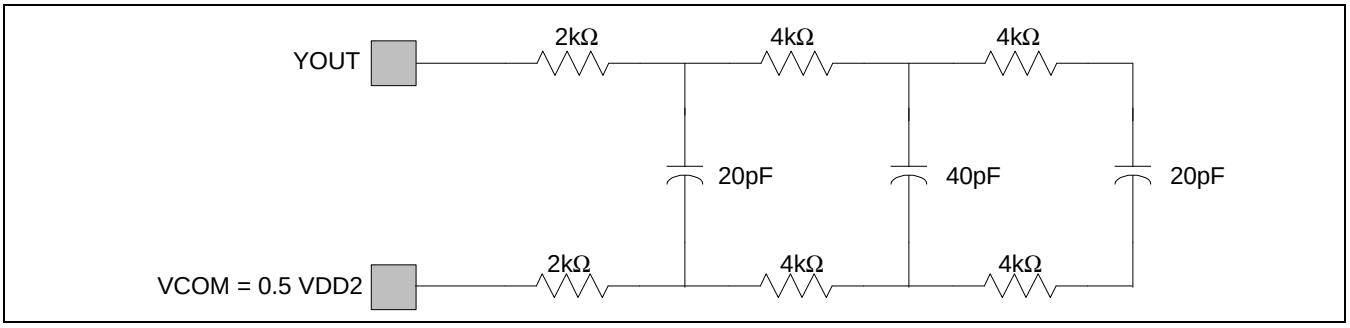

Figure 5. Yout Load Condition

SINGLE EDGE AC CHARACTERISTICS

Table 6. AC Characteristics (Ta = -20 to 75 °C, VDD2 = 8 to 15 V, VSS1 = VSS2 = 0 V, DEC = L)

Parameter	Symbol	Condition	VDD1 = 2.5 to 3.0 V		VDD1 = 3.0 to 3.6 V		Unit
			Min.	Max.	Min.	Max.	
Clock pulse width	PWCLK	-	18	-	13	-	ns
Clock pulse low period	PWCLK(L)	-	3	-	2	-	
Clock pulse high period	PWCLK(H)	-	3	-	2	-	
Data setup time	tSETUP1	-	3	-	2	-	
Data hold time	tHOLD1	-	0	-	0	-	
Start pulse setup time	tSETUP2	-	3	-	2	-	
Start pulse hold time	tHOLD2	-	0	-	0	-	
DATPOL-CLK2 setup time	tSETUP4	-	3	-	2	-	
DATPOL-CLK2 hold time	tHOLD4	-	0	-	0	-	
Start pulse delay time	tPLH1	CL = 20 pF	-	15	-	11	
CLK1 setup time	tSETUP3	-	2	-	2	-	CLK2 period
Driver output delay time1	tPHL1	PWCLK1 = 1 µs, Refer Figure 5. Yout Load Condition	-	4	-	4	µs
Driver output delay time2	tPHL2		-	8	-	8	
CLK1 pulse high period	PWCLK1	-	0.5	2	0.5	2	
Data invalid period	tINV	-	1	-	1	-	CLK2 period
Last data timing	tLDT	-	1	-	1	-	
CLK1-CLK2 time	tCLK1-CLK2	CLK1↑ or ↓ → CLK2↑	8	-	6	-	ns
POL-CLK1 time	tPOL-CLK1	POL↑ or ↓ → CLK1↑	8	-	6	-	ns

DOUBLE EDGE AC CHARACTERISTICS

Table 7. AC Characteristics (Ta = -20 to 75 °C, VDD2 = 8 to 15 V, VSS1 = VSS2 = 0 V, DEC = H)

Parameter	Symbol	Condition	VDD1 = 2.5 to 3.0 V		VDD1 = 3.0 to 3.6 V		Unit
			Min.	Max.	Min.	Max.	
Clock pulse width	PWCLK	-	25	-	18	-	ns
Clock pulse low period	PWCLK(L)	-	4	-	3	-	
Clock pulse high period	PWCLK(H)	-	4	-	3	-	
Data setup time	tSETUP1	-	4	-	3	-	
Data hold time	tHOLD1	-	0	-	0	-	
Start pulse setup time	tSETUP2	-	4	-	3	-	
Start pulse hold time	tHOLD2	-	0	-	0	-	
DATPOL-CLK2 setup time	tSETUP4	-	4	-	3	-	
DATPOL-CLK2 hold time	tHOLD4	-	0	-	0	-	
Start pulse delay time	tPLH1	CL = 20 pF	-	15	-	15	
CLK1 setup time	tSETUP3	-	1	-	1	-	CLK2 period
Driver output delay time1	tPHL1	PWCLK1 = 1 µs , Figure 5. Yout Load Condition	-	4	-	4	µs
Driver output delay time2	tPHL2		-	8	-	8	
CLK1 pulse high period	PWCLK1	-	0.5	2	0.5	2	
Data invalid period	tINV	-	0.5	-	0.5	-	CLK2 period
Last data timing	tLDT		1	-	1	-	
CLK1-CLK2 time	tCLK1-CLK2	CLK1↑ or ↓ → CLK2↑	8	-	6	-	ns
POL-CLK1 time	tPOL-CLK1	POL↑ or ↓ → CLK1↑	8	-	6	-	ns

SINGLE EDGE WAVEFORMS (VIH = 0.8 VDD1, VIL = 0.2 VDD1)

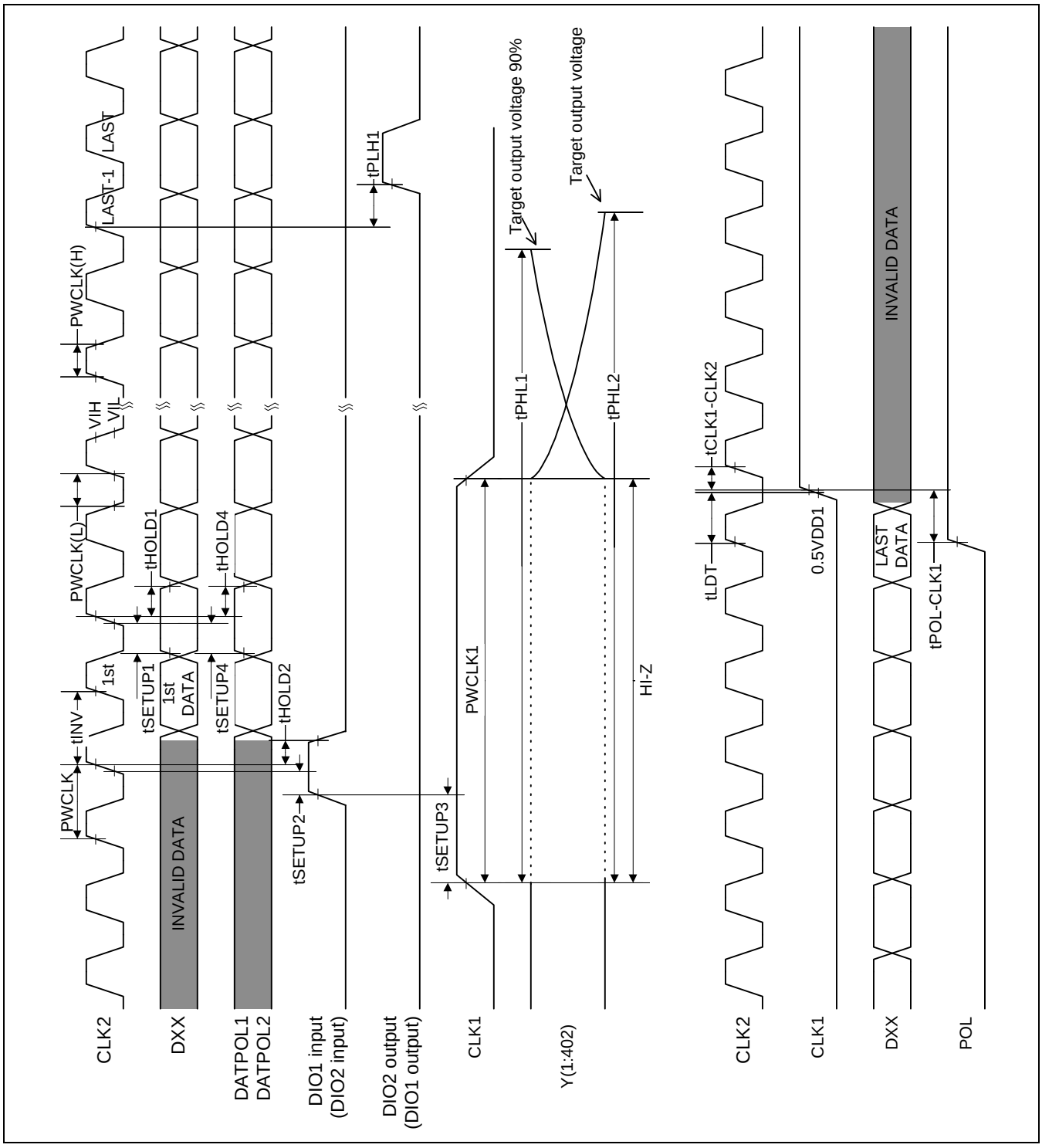

Figure 6. Waveforms, DEC = L

DOUBLE EDGE WAVEFORMS (VIH = 0.8 VDD1, VIL = 0.2 VDD1)

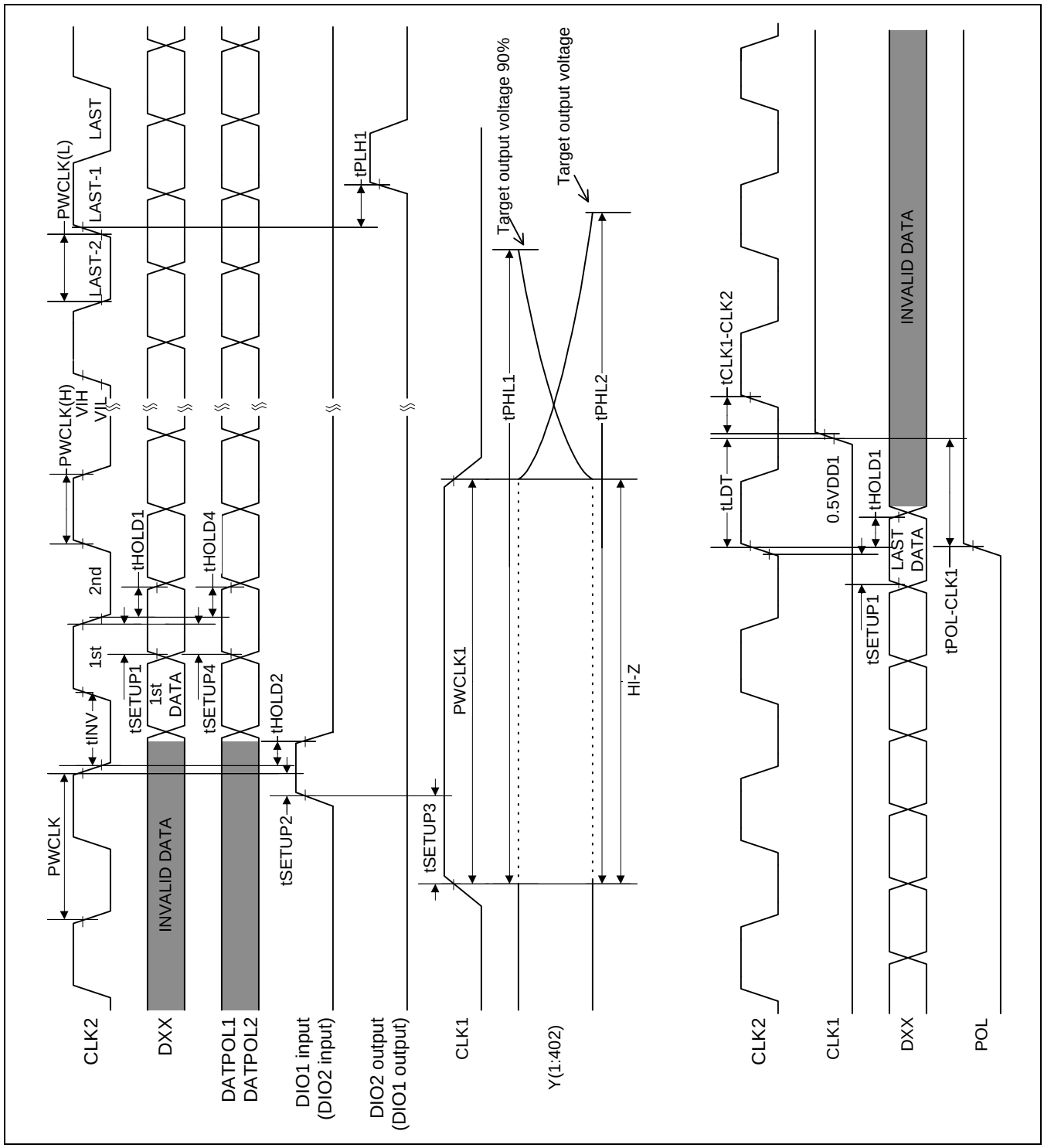

Figure 7. Waveforms, DEC = H

RELATIONSHIPS BETWEEN CLK1, START PULSE (DIO1, DIO2) AND BLANKING PERIOD

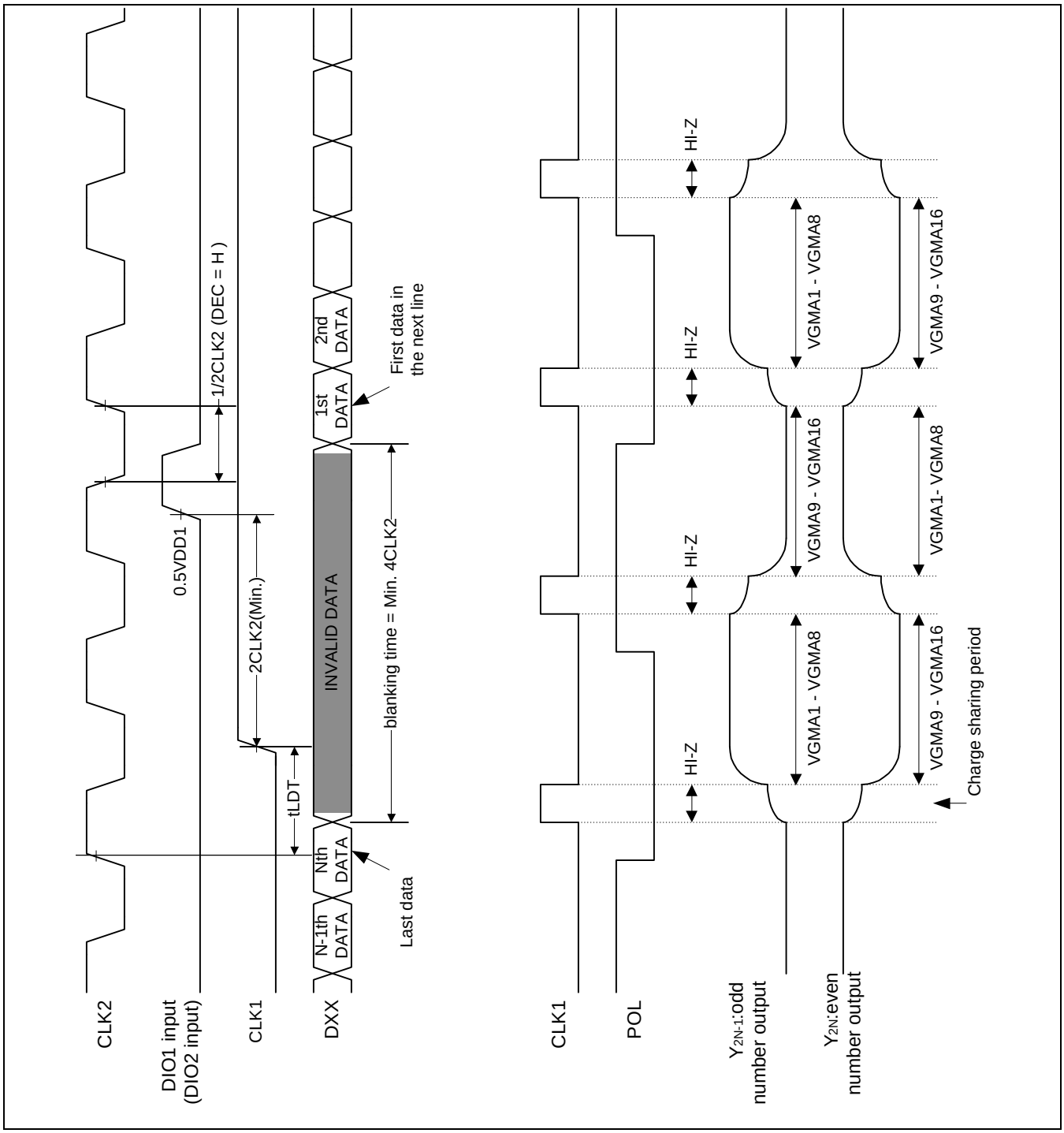

Figure 8. Waveforms