HN27C101AP/AFP/ATT Series
HN27C301AP/AFP Series

131072-word × 8-bit CMOS One Time Electrically Programmable ROM

HITACHI

Description

The HN27C101AP/AFP/ATT series are 131072-word × 8-bit one time electrically programmable ROM. Initially, all bits of the HN27C101AP/AFP/ATT, HN27C301AP /AFP series are in the "1" state (output high). Data is introduced by selectively programming "0" into the desired bit location. This device is packaged in 32-pin plastic package, therefore, this device cannot be rewritten and erased. The packages of the HN27C101ATT series are surface mount thin and small outline packages. They are suitable for hand-held equipment such as a memory card.

Features

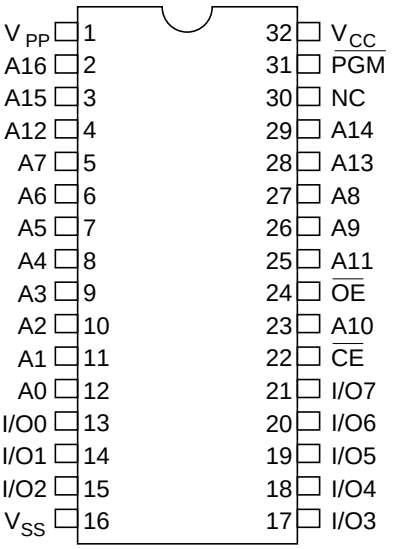
- Single power supply: +5 V ± 10%
- Fast high-reliability programming mode and fast high-reliability page programming mode
  - — Programming voltage: +12.5 V DC
  - — Fast high-reliability page programming: 14 sec typ
- High speed inputs and outputs TTL compatible during both read and program modes
- Low power dissipation: 50 mW/MHz typ (active)
  5 μW typ (standby)
- Pin arrangement: 32-pin JEDEC standard except HN27C301A series replaceable 32 pin Mask ROM (HN27C301AP/AFP Series)
- Package
  - — Surface mount thin and small outline package (TSOP) type II: HN27C101ATT series
- Device identifier mode: manufacturer code and device code
- Fully compatible with HN27C101P/FP, 301P/FP series

Ordering Information

Type No.	Access Time	Package
HN27C101AP-12	120 ns	600-mil 32-pin plastic DIP (DP-32)
HN27C101AP-15	150 ns	
HN27C101AP-20	200 ns	
HN27C101AP-25	250 ns	
HN27C301AP-12	120 ns	
HN27C301AP-15	150 ns	
HN27C301AP-20	200 ns	
HN27C301AP-25	250 ns	
HN27C101AFP-12	120 ns	32-pin plastic SOP (FP-32D)
HN27C101AFP-15	150 ns	
HN27C101AFP-20	200 ns	
HN27C101AFP-25	250 ns	
HN27C301AFP-12	120 ns	
HN27C301AFP-15	150 ns	
HN27C301AFP-20	200 ns	
HN27C301AFP-25	250 ns	
HN27C101ATT-12	120 ns	32-pin plastic TSOP-(II) (TTP-32D)
HN27C101ATT-15	150ns	

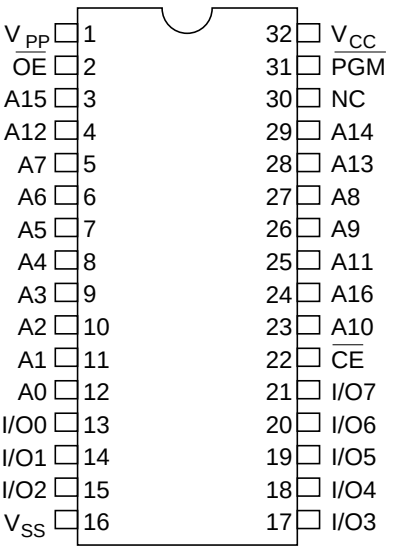
Pin Arrangement

HN27C101AP/AFP Series



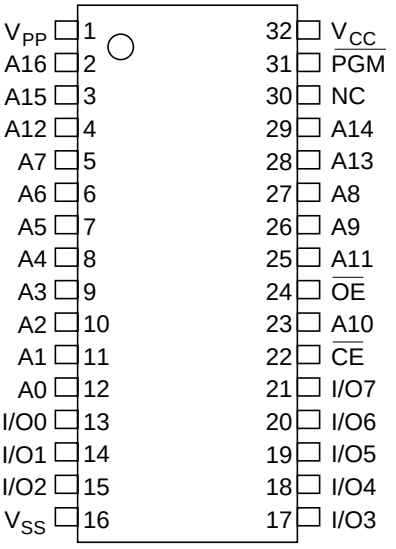
(Top view)

HN27C301AP/AFP Series



(Top view)

HN27C101ATT Series

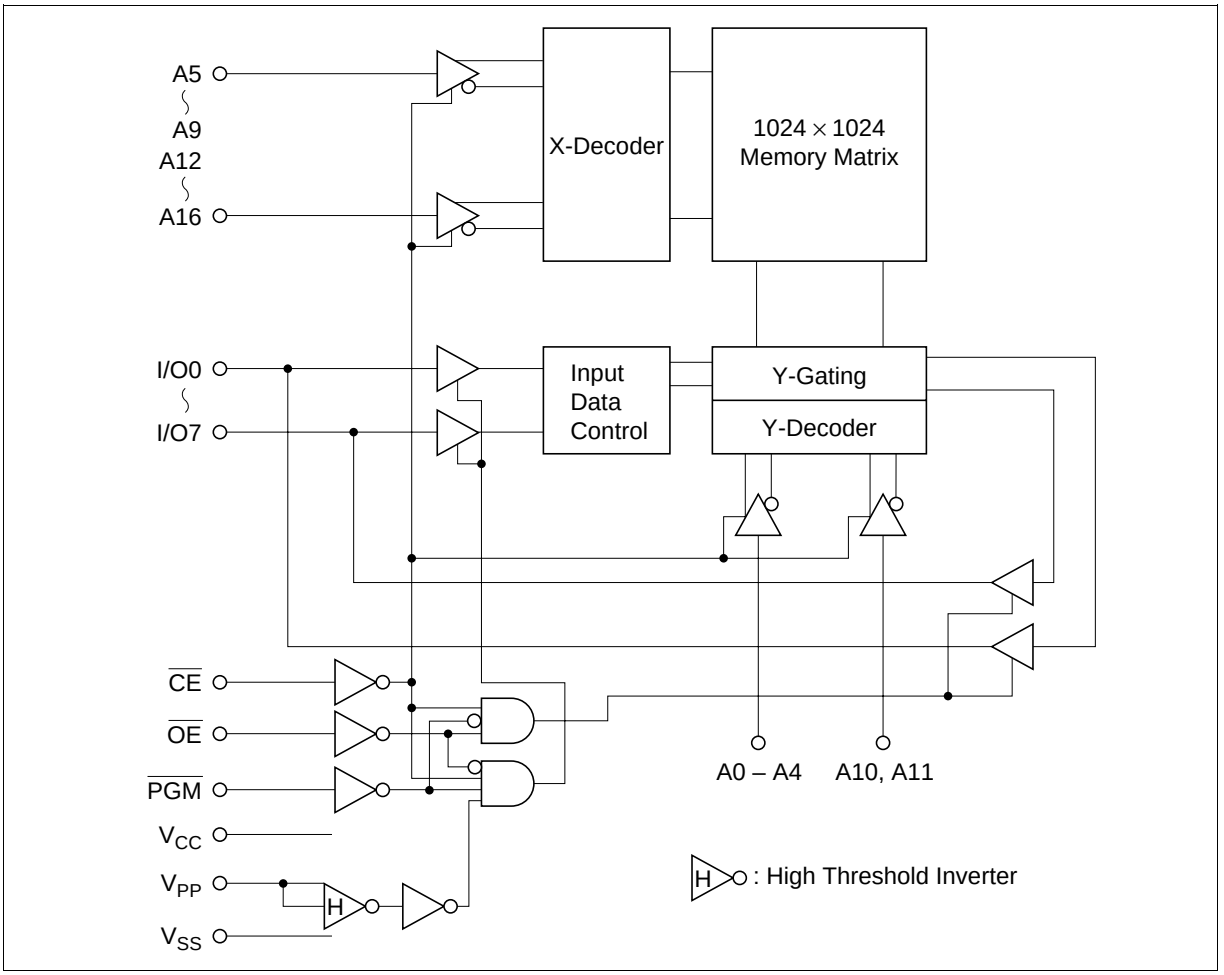


(Top view)

Pin Description

Pin Name	Function
A0 – A16	Address
I/O0 – I/O7	Input/output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{PP}	Programming power supply
V_{SS}	Ground
$\overline{PGM}$	Programming enable
NC	No connection

Block Diagram



Mode Selection

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	$\overline{A9}$	V_{PP}	V_{CC}	I/O
HN27C101A	**(22)**	**(24)**	**(31)**	**(26)**	**(1)**	**(32)**	**(13 – 15, 17 – 21)**
HN27C301A	**(22)**	**(2)**	**(31)**	**(26)**	**(1)**	**(32)**	**(13 – 15, 17 – 21)**
Read	V_{IL}	V_{IL}	V_{IH}	X	V_{CC}	V_{CC}	Dout
Output disable	V_{IL}	V_{IH}	V_{IH}	X	V_{CC}	V_{CC}	High-Z
Standby	V_{IH}	X	X	X	V_{CC}	V_{CC}	High-Z
Program	V_{IL}	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	Din
Program verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	Dout
Page data latch	V_{IH}	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	Din
Page program	V_{IH}	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	High-Z
Program inhibit	V_{IL}	V_{IL}	V_{IL}	X	V_{PP}	V_{CC}	High-Z
	V_{IL}	V_{IH}	V_{IH}				
	V_{IH}	V_{IL}	V_{IL}				
	V_{IH}	V_{IH}	V_{IH}				
Identifier	V_{IL}	V_{IL}	V_{IH}	V_H	V_{CC}	V_{CC}	Code

Notes: 1. X: Don't care
2. V_H: 12.0 V ± 0.5 V

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
A11 input and output voltages*[1]	Vin, Vout	–0.6*[2] to +7.0	V
A9 input voltage*[1]	V_{ID}	–0.6*[2] to +13.5	V
V_{PP} voltage*[1]	V_{PP}	–0.6 to +13.5	V
V_{CC} voltage*[1]	V_{CC}	–0.6 to +7.0	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C
Storage temperature range under bias	Tbias	–10 to +80	°C

Notes: 1. Relative to V_{SS}
2. Vin, Vout and V_{ID} min = –1.0 V for pulse width ≤ 50 ns

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	10	pF	Vin = 0 V
Output capacitance	Cout	—	—	15	pF	Vout = 0 V

Read Operation

DC Characteristics (V_{CC} = 5 V ± 10%, V_{PP} = V_{CC}, Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = 0 V to V_{CC}
Output leakage current	I_{LO}	—	—	2	µA	Vout = 0 V to V_{CC}
V_{PP} current	I_{PP1}	—	1	20	µA	V_{PP} = 5.5 V
Standby V_{CC} current	I_{SB1}	—	—	1	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}	—	1	20	mA	$\overline{CE}$ = V_{CC} ± 0.3 V
Operating V_{CC} current	I_{CC1}	—	—	30	mA	$\overline{CE}$ = V_{IL}, Iout = 0 mA
	I_{CC2}	—	—	30	mA	f = 5 MHz, Iout = 0 mA
		—	—	45	mA	f = 8.4 MHz, Iout = 0 mA
Input low voltage	V_{IL}	–0.3*[1]	—	0.8	V	
Input high voltage	V_{IH}	2.2	—	V_{CC} + 1.0*[2]	V	
Output low voltage	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –1 mA
		V_{CC} – 0.7	—	—	V	I_{OH} = –0.1 mA

Notes: 1. V_{IL} min = –1.0 V for pulse width ≤ 50 ns.
2. V_{IH} max = V_{CC} +1.5 V for pulse width ≤ 20 ns.
If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

AC Characteristics (V_{CC} = 5 V ± 10%, V_{PP} = V_{CC}, Ta = 0 to +70°C)

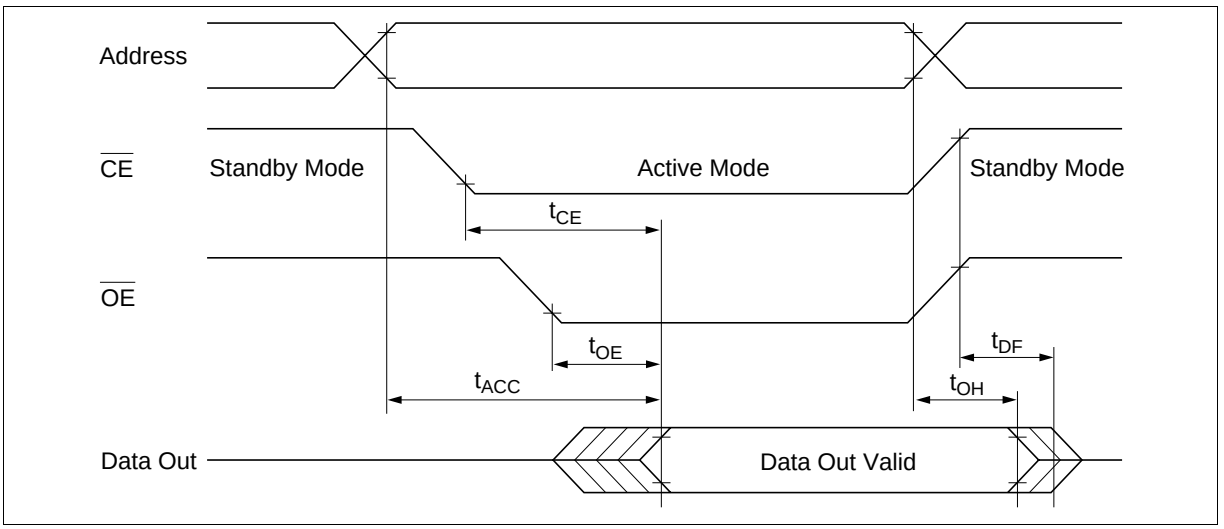
Test Conditions

- Input pulse levels: 0.45 V to 2.4 V
- Input rise and fall time: ≤ 20 ns
- Output load: 1 TTL Gate +100 pF
- Reference levels for measuring timing: Inputs; 0.8 V and 2.0 V
  Outputs; 0.8 V and 2.0 V

		HN27C101AP/AFP/ATT HN27C301AP/AFP				HN27C101AP/AFP HN27C301AP/AFP					
		-12		-15		-20		-25			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Address to output delay	t_{ACC}	—	120	—	150	—	200	—	250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}	—	120	—	150	—	200	—	250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to output delay	t_{OE}	—	60	—	70	—	70	—	100	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ high to output float	t_{DF}	0	50	0	50	0	50	0	60	ns	$\overline{CE}$ = V_{IL}
Address to output hold	t_{OH}	0	—	0	—	0	—	0	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

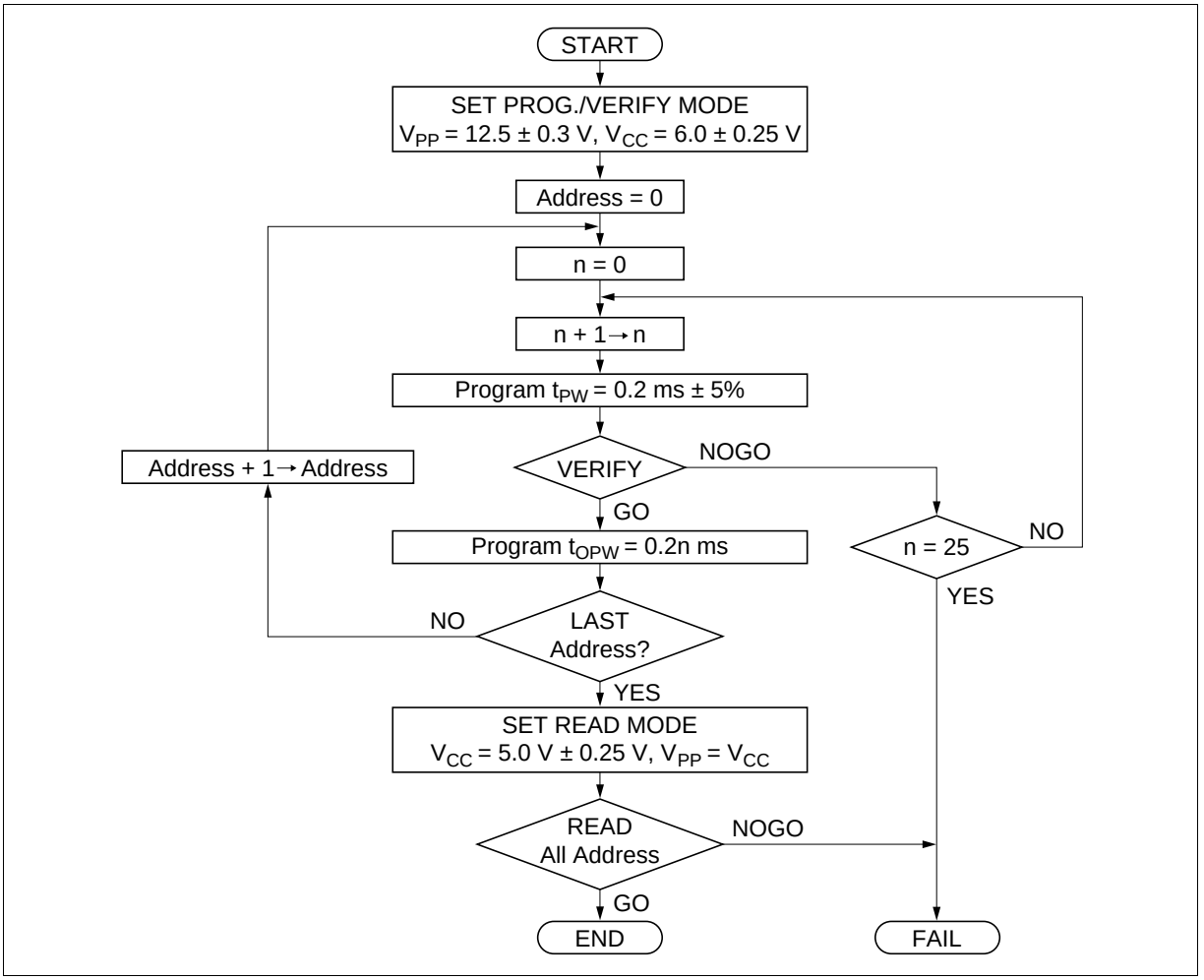
Note: t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Read Timing Waveform



Fast High-Reliability Programming

This device can be applied the programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Programming Flowchart

DC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = 0 V to V_{CC}
V_{PP} supply current	I_{PP}	—	—	40	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}
Operating V_{CC} current	I_{CC}	—	—	30	mA	
Input low level	V_{IL}	–0.1*[5]	—	0.8	V	
Input high level	V_{IH}	2.2	—	V_{CC} + 0.5*[6]	V	
Output low voltage during verify	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
Output high voltage during verify	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} must not exceed 13.5 V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5 V.
4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = Low.
5. V_{IL} min = –0.6 V for pulse width ≤ 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V)

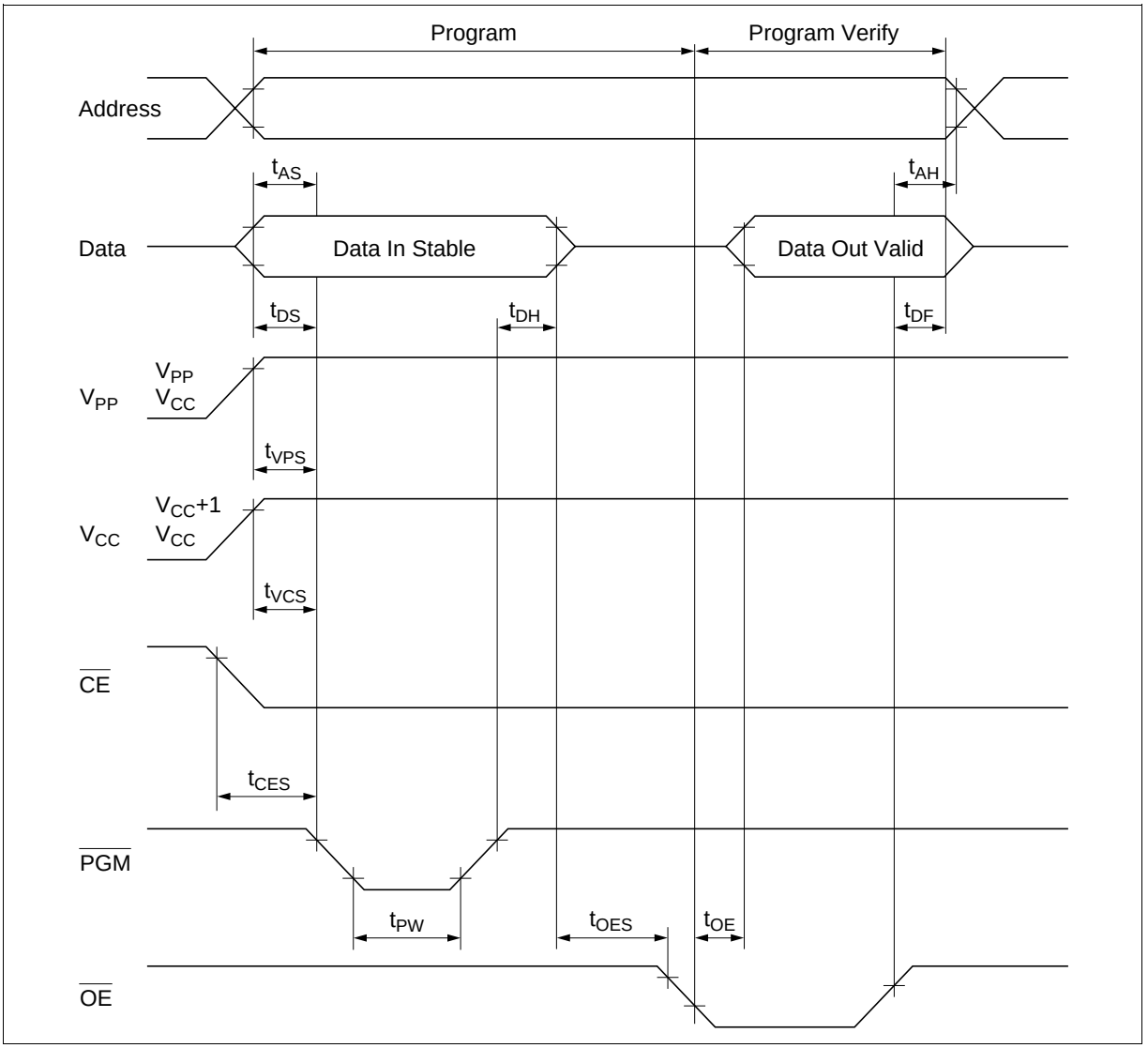
Test Conditions

- Input pulse levels: 0.45 V to 2.4 V
- Input rise and fall time: ≤ 20 ns
- Reference levels for measuring timing: Inputs; 0.8 V and 2.0 V
  Outputs; 0.8 V and 2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address setup time	t_{AS}	2	—	—	µs	
$\overline{OE}$ setup time	t_{OES}	2	—	—	µs	
Data setup time	t_{DS}	2	—	—	µs	
Address hold time	t_{AH}	0	—	—	µs	
Data hold time	t_{DH}	2	—	—	µs	
$\overline{OE}$ to output float delay	t_{DF}*1	0	—	130	ns	
V_{PP} setup time	t_{VPS}	2	—	—	µs	
V_{CC} setup time	t_{VCS}	2	—	—	µs	
$\overline{PGM}$ initial programming pulse width	t_{PW}	0.19	0.2	0.21	ms	
$\overline{PGM}$ overprogramming pulse width	t_{OPW}*2	0.19	—	5.25	ms	
$\overline{CE}$ setup time	t_{CES}	2	—	—	µs	
Data valid from $\overline{OE}$	t_{OE}	0	—	150	ns	

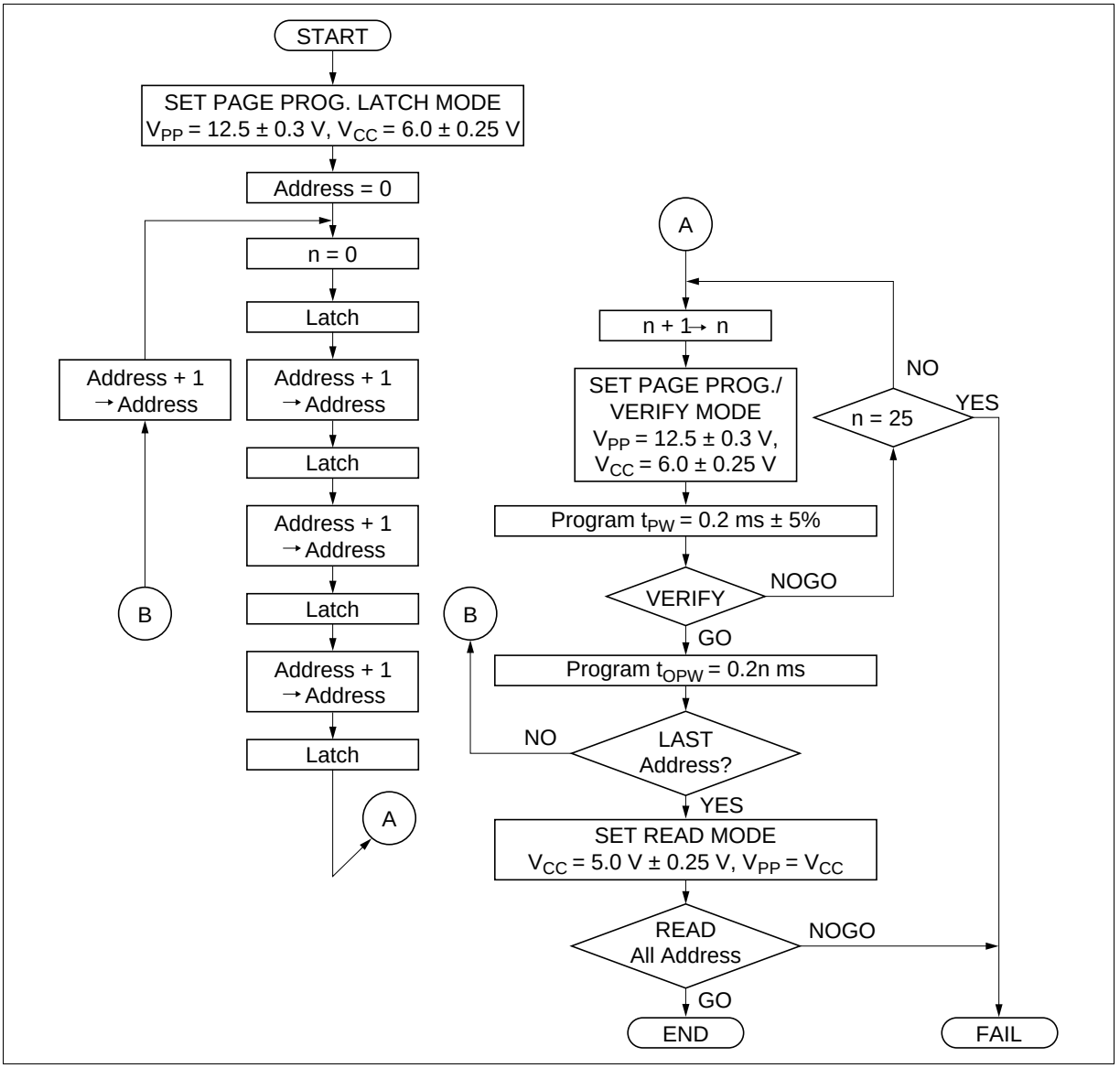
Notes: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
2. Refer to the programming flowchart for t_{OPW}.

Fast High-Reliability Programming Timing Waveform



Fast High-Reliability Page Programming

This device can be applied the high performance page programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Page Programming Flowchart

DC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = 0 V to V_{CC}
V_{PP} supply current	I_{PP}	—	—	50	mA	$\overline{CE}$ = $\overline{OE}$= V_{IH}, $\overline{PGM}$ = V_{IL}
Operating V_{CC} current	I_{CC}	—	—	30	mA	
Input low level	V_{IL}	–0.1*[5]	—	0.8	V	
Input high level	V_{IH}	2.2	—	V_{CC} + 0.5*[6]	V	
Output low voltage during verify	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
Output high voltage during verify	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} must not exceed 13.5 V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5 V.
4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = Low.
5. V_{IL} min = –0.6 V for pulse width ≤ 20 ns
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V)

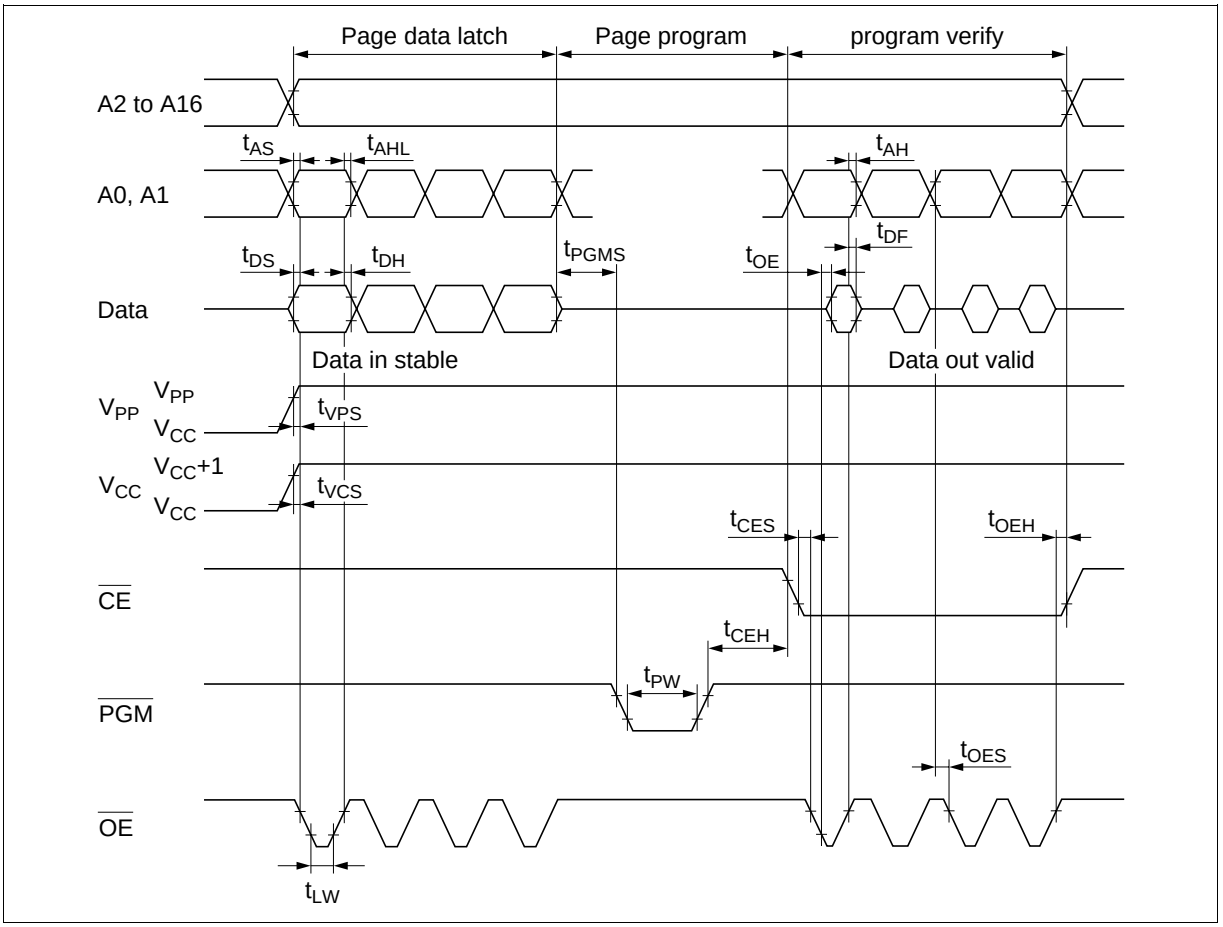
Test Conditions

- Input pulse levels: 0.45 V to 2.4 V
- Input rise and fall time: ≤ 20 ns
- Reference levels for measuring timing: Inputs; 0.8 V and 2.0 V
  Outputs; 0.8 V and 2.0 V

Parameter	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	2	—	—	µs
$\overline{OE}$ setup time	t_{OES}	2	—	—	µs
Data setup time	t_{DS}	2	—	—	µs
Address hold time	t_{AH}	0	—	—	µs
	t_{AHL}	2	—	—	µs
Data hold time	t_{DH}	2	—	—	µs
$\overline{OE}$ to output float delay	t_{DF}*[1]	0	—	130	ns
V_{PP} setup time	t_{VPS}	2	—	—	µs
V_{CC} setup time	t_{VCS}	2	—	—	µs
$\overline{PGM}$ initial programming pulse width	t_{PW}	0.19	0.2	0.21	ms
$\overline{PGM}$ overprogramming pulse width	t_{OPW}*[2]	0.19	—	5.25	ms
$\overline{CE}$ setup time	t_{CES}	2	—	—	µs
Data valid from $\overline{OE}$	t_{OE}	0	—	150	ns
$\overline{OE}$ pulse width during data latch	t_{LW}	1	—	—	µs
$\overline{PGM}$ setup time	t_{PGMS}	2	—	—	µs
$\overline{CE}$ hold time	t_{CEH}	2	—	—	µs
$\overline{OE}$ hold time	t_{OEH}	2	—	—	µs

Notes: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
2. Refer to the programming flowchart for t_{OPW}.

Fast High-Reliability Page Programming Timing Waveform



Mode Description

Device Identifier Mode

The device identifier mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of OTPROM. By this mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

HN27C101AP/AFP/ATT Identifier Code

Identifier	A0 (12)	A9 (26)	I/O7 (21)	I/O6 (20)	I/O5 (19)	I/O4 (18)	I/O3 (17)	I/O2 (15)	I/O1 (14)	I/O0 (13)	Hex Data
Manufacturer code	V_{IL}	V_H	0	0	0	0	0	1	1	1	07
Device code	V_{IH}	V_H	0	0	1	1	1	0	0	0	38

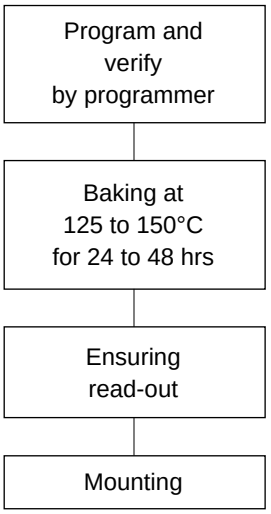
HN27C301AP/AFP Identifier Code

Identifier	A0 (12)	A9 (26)	I/O7 (21)	I/O6 (20)	I/O5 (19)	I/O4 (18)	I/O3 (17)	I/O2 (15)	I/O1 (14)	I/O0 (13)	Hex Data
Manufacturer code	V_{IL}	V_H	0	0	0	0	0	1	1	1	07
Device code	V_{IH}	V_H	1	0	1	1	1	0	0	1	B9

Notes: 1. $V_H = 12.0\ V \pm 0.5\ V$
2. A1 – A8, A10 – A16, $\overline{CE}$, $\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$

Recommended Screening Conditions

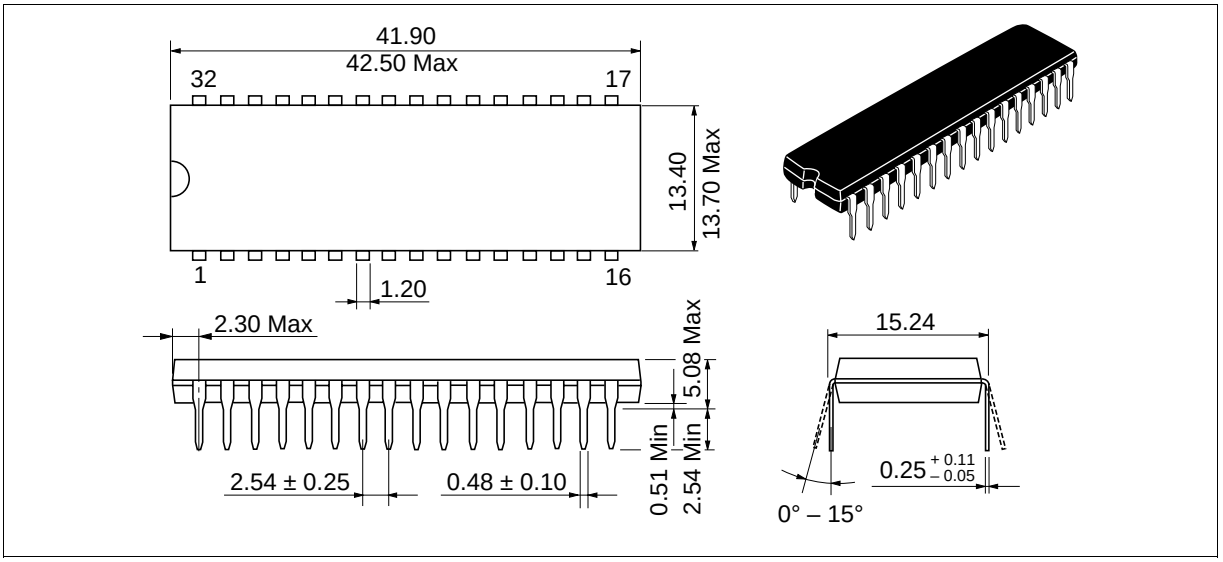
Before mounting, please make the screening (baking without bias) shown in the right.



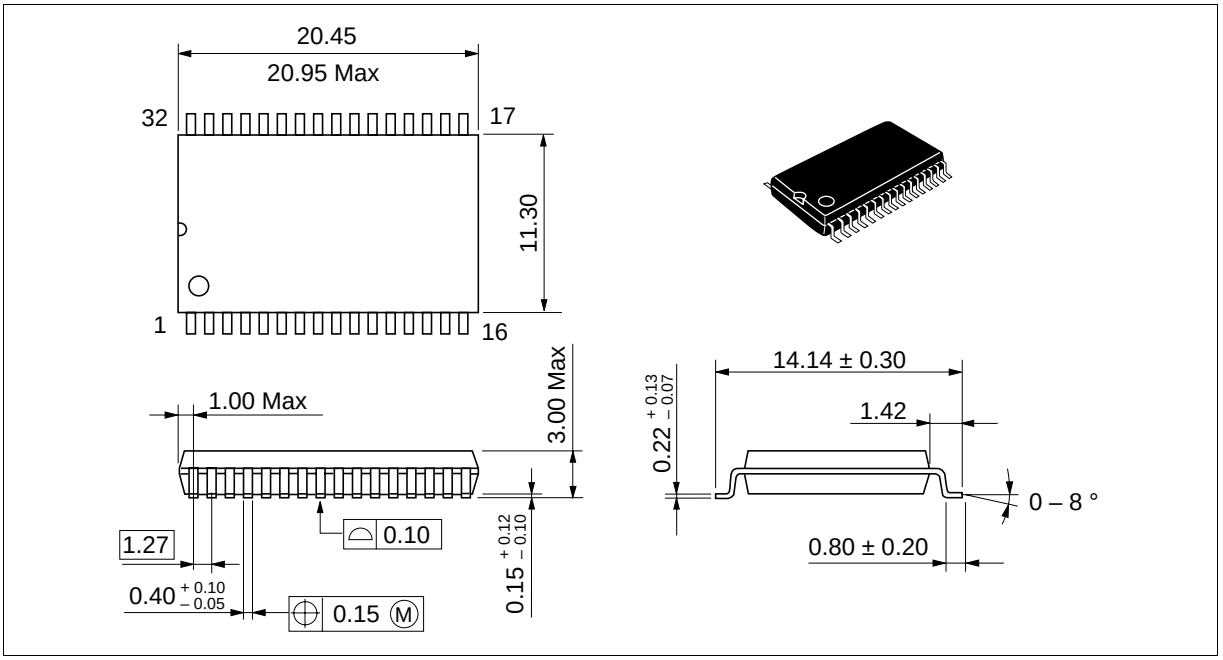
Recommended Screening Conditions

Package Dimensions

HN27C101AP/HN27C301AP Series (DP-32) Unit: mm



HN27C101AFP/HN27C301AFP Series (FP-32D) Unit: mm



HN27C101ATT Series (TTP-32D) Unit: mm