

100V/2A Peak, Low Cost, High Frequency Half Bridge Driver

The HIP2100 is a high frequency, 100V Half Bridge N-Channel MOSFET driver IC, available in 8 lead plastic SOIC. The low-side and high-side gate drivers are independently controlled and matched to 8ns. This gives the user maximum flexibility in dead-time selection and driver protocol. Undervoltage protection on both the low-side and high-side supplies force the outputs low. An on-chip diode eliminates the discrete diode required with other driver ICs. A new level-shifter topology yields the low-power benefits of pulsed operation with the safety of DC operation. Unlike some competitors, the high-side output returns to its correct state after a momentary undervoltage of the high-side supply.

Ordering Information

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE | PKG. NO. |
|-------------|------------------|---------------|----------|
| HIP2100IB | -40°C to 85°C | 8 Ld SOIC (N) | M8.15 |

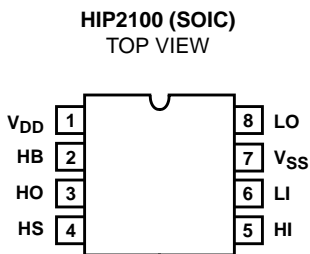
Features

- Drives N-Channel MOSFET Half Bridge
- Space Saving SO8 Package
- Bootstrap Supply Max Voltage to 116VDC
- On-Chip 1Ω Bootstrap Diode
- Fast Propagation Times Needed for Multi-MHz Circuits
- Drives 1000pF Load at 1MHz with Rise and Fall Times of Typically 10ns
- CMOS Input Thresholds for Improved Noise Immunity
- Independent Inputs for Non-Half Bridge Topologies
- No Start-Up Problems
- Outputs Unaffected by Supply Glitches, HS Ringing Below Ground, or HS Slewing at High dv/dt
- Low Power Consumption
- Wide Supply Range
- Supply Undervoltage Protection
- 3Ω Output Resistance

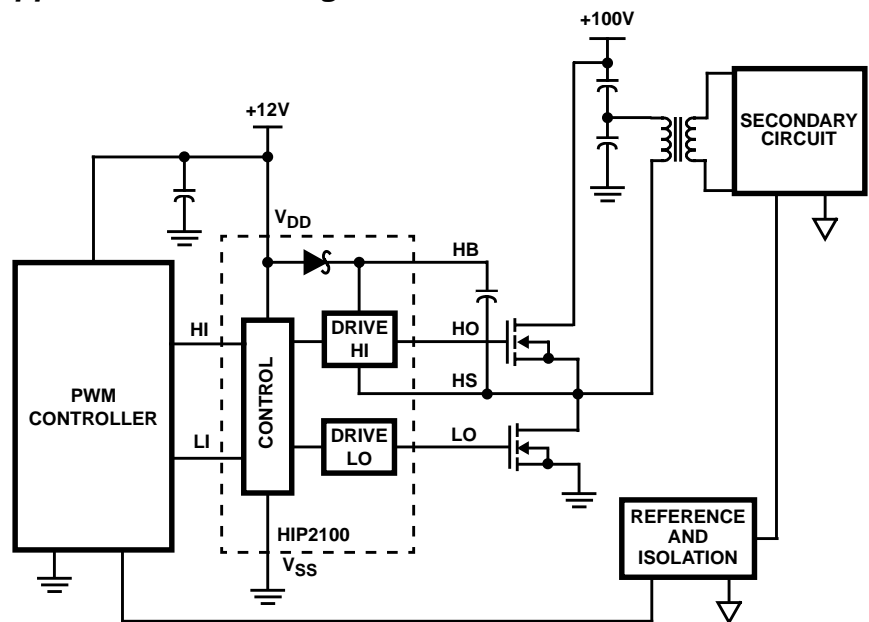
Applications

- Telecom Half Bridge Power Supplies
- Avionic DC-DC Converters
- Two-Switch Forward Converters
- Active Clamp Forward Converters

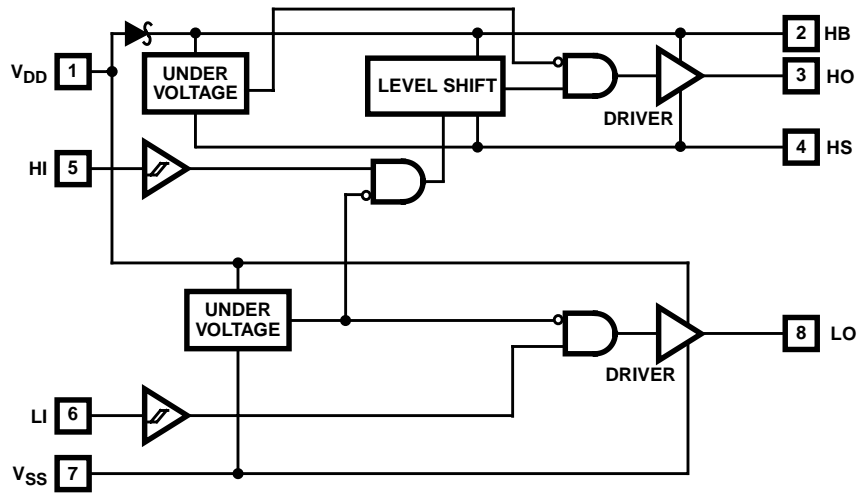
Pinout



Application Block Diagram



Functional Block Diagram



Other Applications

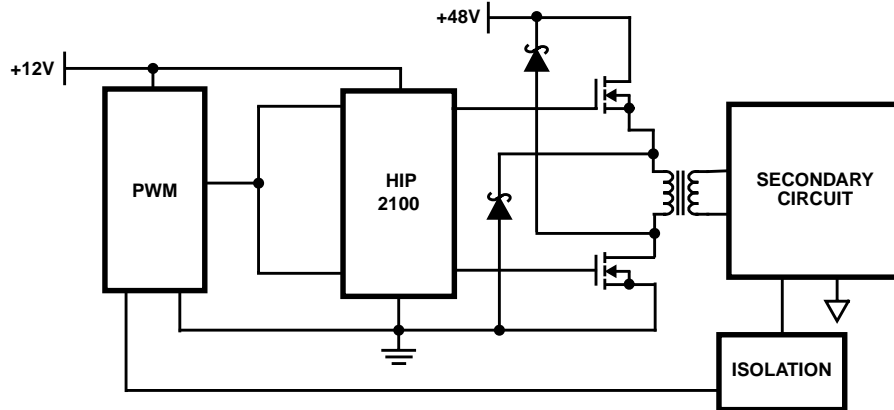


FIGURE 1. TWO-SWITCH FORWARD CONVERTER

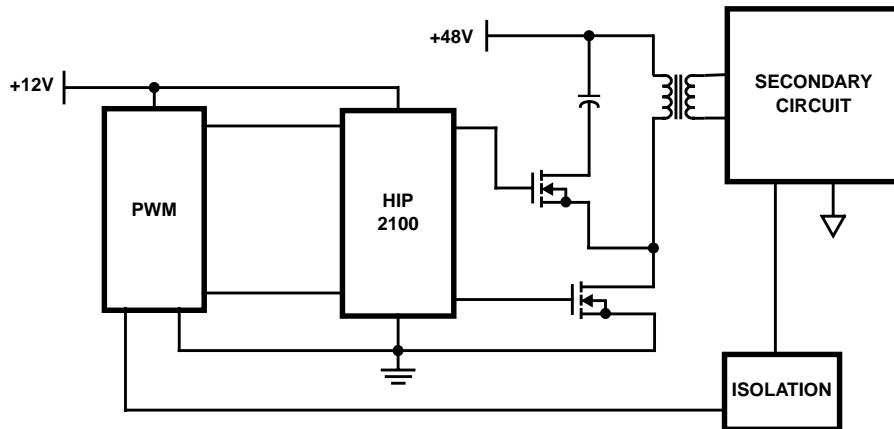


FIGURE 2. FORWARD CONVERTER WITH AN ACTIVE CLAMP

Absolute Maximum Ratings

Supply Voltage, V_{DD} , V_{HB} - V_{HS} -0.3V to 18V
 LI and HI Voltages -3V to V_{DD} +0.3V
 Voltage on LO -0.3V to V_{DD} +0.3V
 Voltage on HO V_{HS} -0.3V to V_{HB} +0.3V
 Voltage on HS (Continuous) -1V to 110V
 Voltage on HB +118V
 Average Current in V_{DD} to HB diode 100mA
 ESD Classification Class 1 (1kV)
 NOTE: All Voltages Relative to Pin 7, V_{SS} Unless Otherwise Specified

Thermal Information

Thermal Resistance
 SOIC θ_{JA} 160°C/W θ_{JC} N/A
 SOIC in Thermal Conductive Media 70°C/W
 HS Slew Rate 10V/ns
 Storage Temperature Range -65°C to 150°C
 Junction Temperature Range -55°C to 150°C
 Lead Temperature (Soldering 10s - Lead Tips Only) 300°C
 Maximum Power Dissipation at +25°C in Free Air 780mW

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the recommended operating conditions of this specification is not implied.

Recommended Operating Conditions

Supply Voltage, V_{DD} +9V to +16.5V
 Voltage on HS (Repetitive Transient) -5V to 105V
 Voltage on HB V_{HS} +8V to V_{HS} +16.5V and V_{DD} -1V to V_{DD} +100V

Electrical Specifications $V_{DD} = V_{HB} = 12V$, $V_{SS} = V_{HS} = 0V$, No Load on LO or HO, Unless Otherwise Specified

| PARAMETERS | SYMBOL | TEST CONDITIONS | $T_J = 25^\circ C$ | | | $T_J = -40^\circ C$ TO $125^\circ C$ | | UNITS |
|------------------------------------|------------|---|--------------------|------|------|---|-----|------------|
| | | | MIN | TYP | MAX | MIN | MAX | |
| SUPPLY CURRENTS | | | | | | | | |
| V_{DD} Quiescent Current | I_{DD} | LI = HI = 0V | - | 0.1 | 0.15 | - | 0.2 | mA |
| V_{DD} Operating Current | I_{DDO} | f = 500kHz | - | 1.5 | 2.5 | - | 3 | mA |
| Total HB Quiescent Current | I_{HB} | LI = HI = 0V | - | 0.1 | 0.15 | - | 0.2 | mA |
| Total HB Operating Current | I_{HBO} | f = 500kHz | - | 1.5 | 2.5 | - | 3 | mA |
| HB to V_{SS} Current, Quiescent | I_{HBS} | $V_{HS} = V_{HB} = 116.5V$ | - | 0.05 | 1 | - | 10 | μA |
| HB to V_{SS} Current, Operating | I_{HBSO} | f = 500kHz | - | 0.7 | - | - | - | mA |
| INPUT PINS | | | | | | | | |
| Low Level Input Voltage Threshold | V_{IL} | | 4 | 5.4 | - | 3 | - | V |
| High Level Input Voltage Threshold | V_{IH} | | - | 5.8 | 7 | - | 8 | V |
| Input Voltage Hysteresis | V_{IHYS} | | - | 0.4 | - | - | - | V |
| Input Pulldown Resistance | R_I | | - | 200 | - | 100 | 500 | k Ω |
| UNDER VOLTAGE PROTECTION | | | | | | | | |
| V_{DD} Rising Threshold | V_{DDR} | | 7 | 7.3 | 7.8 | 6.5 | 8 | V |
| V_{DD} Threshold Hysteresis | V_{DDH} | | - | 0.5 | - | - | - | V |
| HB Rising Threshold | V_{HBR} | | 6.5 | 6.9 | 7.5 | 6 | 8 | V |
| HB Threshold Hysteresis | V_{HBH} | | - | 0.4 | - | - | - | V |
| BOOT STRAP DIODE | | | | | | | | |
| Low-Current Forward Voltage | V_{DL} | $I_{VDD-HB} = 100\mu A$ | - | 0.45 | 0.55 | - | 0.7 | V |
| High-Current Forward Voltage | V_{DH} | $I_{VDD-HB} = 100mA$ | - | 0.7 | 0.8 | - | 1 | V |
| Dynamic Resistance | R_D | $I_{VDD-HB} = 100mA$ | - | 0.8 | 1 | - | 1.5 | Ω |
| LO GATE DRIVER | | | | | | | | |
| Low Level Output Voltage | V_{OLL} | $I_{LO} = 100mA$ | - | 0.25 | 0.3 | - | 0.4 | V |
| High Level Output Voltage | V_{OHL} | $I_{LO} = -100mA$, $V_{OHL} = V_{DD} - V_{LO}$ | - | 0.25 | 0.3 | - | 0.4 | V |
| Peak Pullup Current | I_{OHL} | $V_{LO} = 0V$ | - | 2 | - | - | - | A |
| Peak Pulldown Current | I_{OLL} | $V_{LO} = 12V$ | - | 2 | - | - | - | A |
| HO GATE DRIVER | | | | | | | | |
| Low Level Output Voltage | V_{OLH} | $I_{HO} = 100mA$ | - | 0.25 | 0.3 | - | 0.4 | V |
| High Level Output Voltage | V_{OHH} | $I_{HO} = -100mA$, $V_{OHH} = V_{HB} - V_{HO}$ | - | 0.25 | 0.3 | - | 0.4 | V |
| Peak Pullup Current | I_{OHH} | $V_{HO} = 0V$ | - | 2 | - | - | - | A |
| Peak Pulldown Current | I_{OLH} | $V_{HO} = 12V$ | - | 2 | - | - | - | A |

HIP2100

Switching Specifications

$V_{DD} = V_{HB} = 12V$, $V_{SS} = V_{HS} = 0V$, No Load on LO or HO, Unless Otherwise Specified

| PARAMETERS | SYMBOL | TEST CONDITIONS | $T_J = 25^\circ C$ | | | $T_J = -40^\circ C$ TO $125^\circ C$ | | UNITS |
|---|------------------|------------------|---|------------|-----|---|-----|-------|
| | | | MIN | TYP | MAX | MIN | MAX | |
| | | | Lower Turn-Off Propagation Delay (LI Falling to LO Falling) | t_{LPHL} | | - | 20 | |
| Upper Turn-Off Propagation Delay (HI Falling to HO Falling) | t_{HPHL} | | - | 20 | 35 | - | 45 | ns |
| Lower Turn-On Propagation Delay (LI Rising to LO Rising) | t_{LPLH} | | - | 20 | 35 | - | 45 | ns |
| Upper Turn-On Propagation Delay (HI Rising to HO Rising) | t_{HPLH} | | - | 20 | 35 | - | 45 | ns |
| Delay Matching: Lower Turn-On and Upper Turn-Off | t_{MON} | | - | 2 | 8 | - | 10 | ns |
| Delay Matching: Lower Turn-Off and Upper Turn-On | t_{MOFF} | | - | 2 | 8 | - | 10 | ns |
| Either Output Rise/Fall Time | t_{RC}, t_{FC} | $C_L = 1000pF$ | - | 10 | - | - | - | ns |
| Either Output Rise/Fall Time (3V to 9V) | t_R, t_F | $C_L = 0.1\mu F$ | - | 0.5 | 0.6 | - | 0.8 | us |
| Either Output Rise Time Driving DMOS | t_{RD} | $C_L = IRFR120$ | - | 20 | - | - | - | ns |
| Either Output Fall Time Driving DMOS | t_{FD} | $C_L = IRFR120$ | - | 10 | - | - | - | ns |
| Minimum Input Pulse Width that Changes the Output | t_{PW} | | - | - | - | - | 50 | ns |
| Bootstrap Diode Turn-On or Turn-Off Time | t_{BS} | | - | 10 | - | - | - | ns |

Pin Descriptions

| PIN NUMBER | SYMBOL | DESCRIPTION |
|------------|----------|---|
| 1 | V_{DD} | Positive Supply to lower gate drivers. De-couple this pin to V_{SS} (Pin 7). Bootstrap diode connected to HB (pin 2). |
| 2 | HB | High-Side Bootstrap supply. External bootstrap capacitor is required. Connect positive side of bootstrap capacitor to this pin. Bootstrap diode is on-chip. |
| 3 | HO | High-Side Output. Connect to gate of High-Side power MOSFET. |
| 4 | HS | High-Side Source connection. Connect to source of High-Side power MOSFET. Connect negative side of bootstrap capacitor to this pin. |
| 5 | HI | High-Side input. |
| 6 | LI | Low-Side input. |
| 7 | V_{SS} | Chip negative supply, generally will be ground. |
| 8 | LO | Low-Side Output. Connect to gate of Low-Side power MOSFET. |

Timing Diagrams

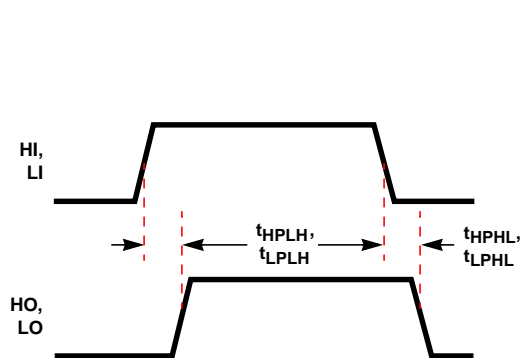


FIGURE 3.

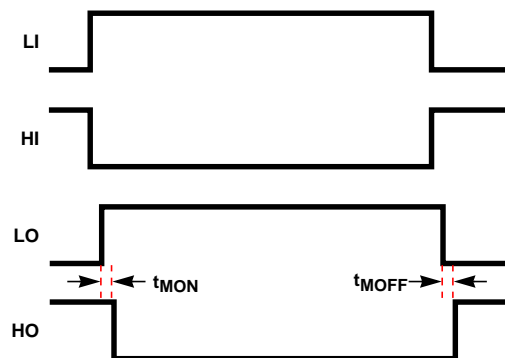


FIGURE 4.

Typical Performance Curves

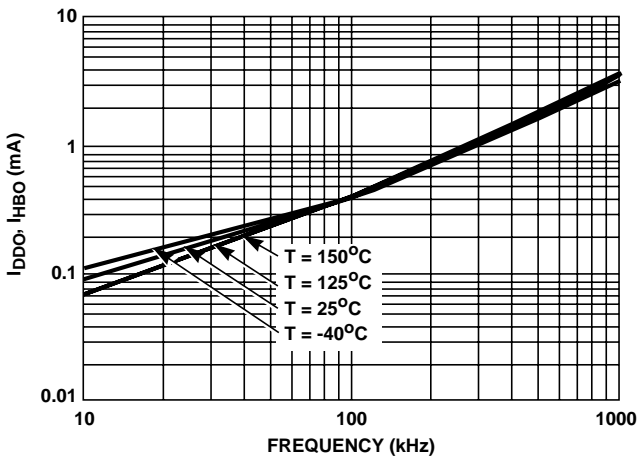


FIGURE 5. OPERATING CURRENT vs FREQUENCY

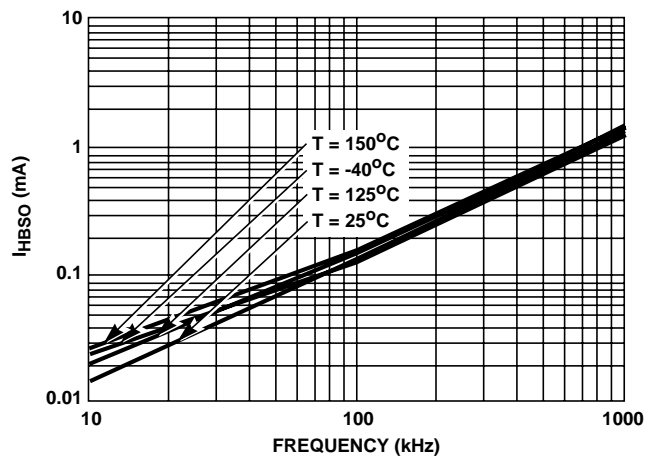


FIGURE 6. LEVEL SHIFTER CURRENT vs FREQUENCY

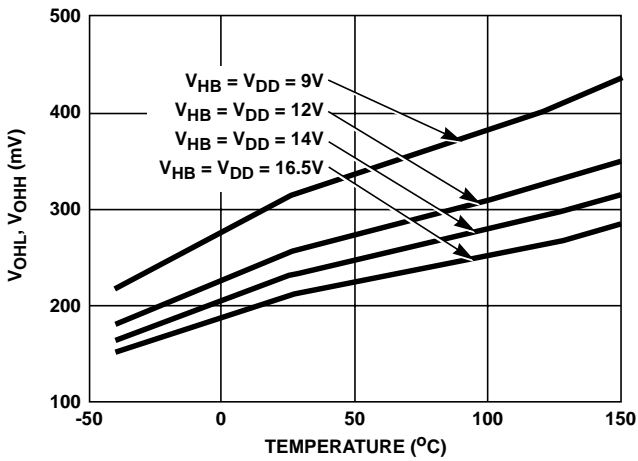


FIGURE 7. HIGH LEVEL OUTPUT VOLTAGE vs TEMPERATURE

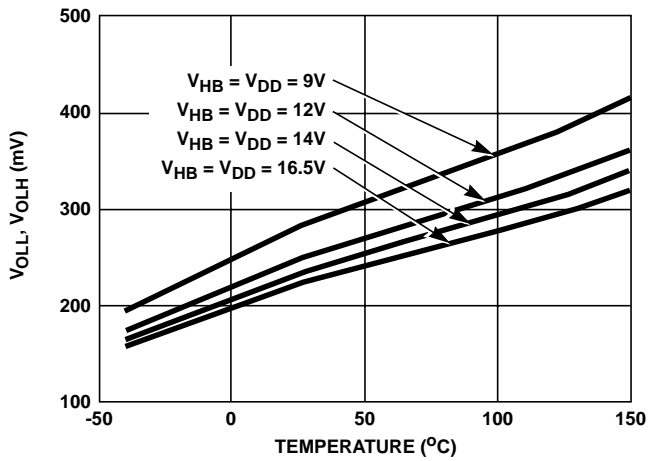


FIGURE 8. LOW LEVEL OUTPUT VOLTAGE vs TEMPERATURE

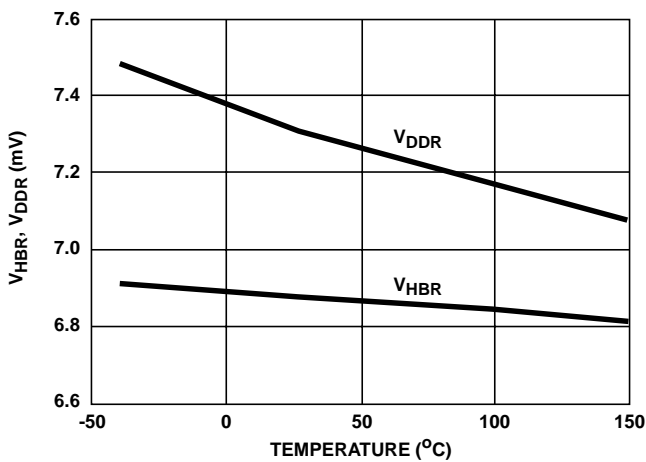


FIGURE 9. UNDERVOLTAGE LOCKOUT THRESHOLD vs TEMPERATURE

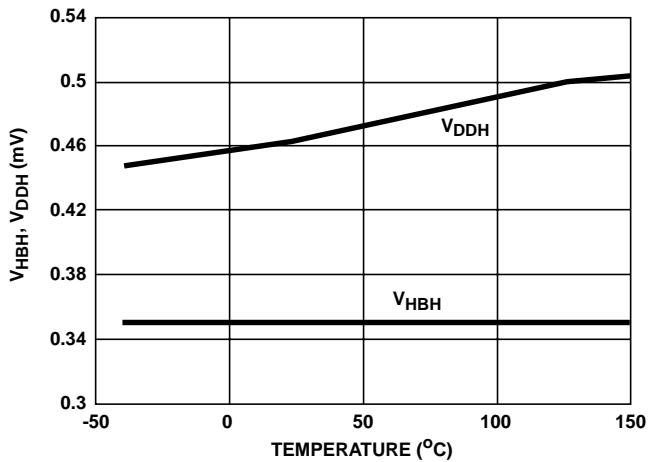


FIGURE 10. UNDERVOLTAGE LOCKOUT HYSTERESIS vs TEMPERATURE

Typical Performance Curves (Continued)

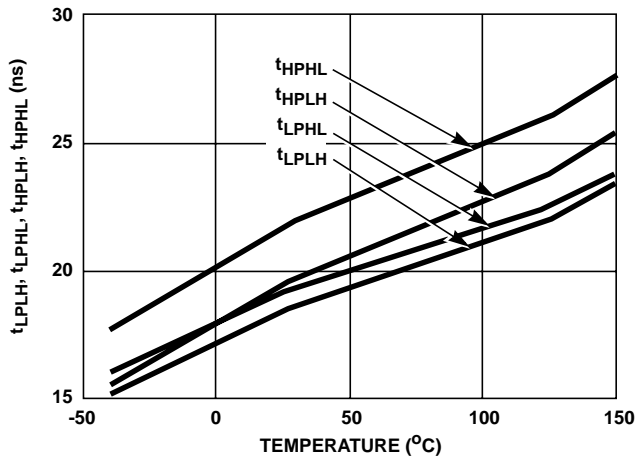


FIGURE 11. PROPAGATION DELAYS vs TEMPERATURE

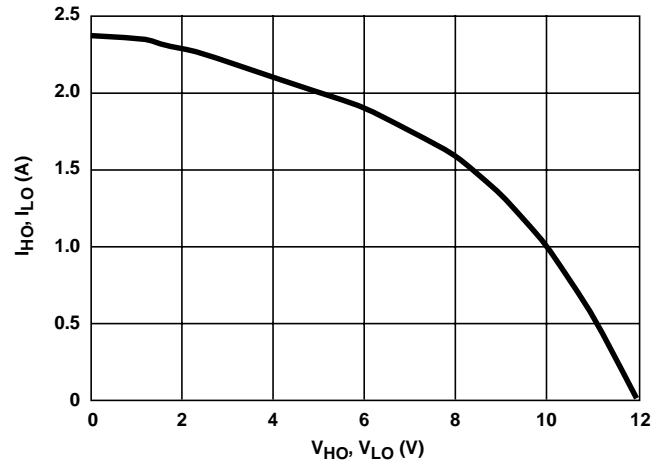


FIGURE 12. PULLUP CURRENT vs OUTPUT VOLTAGE

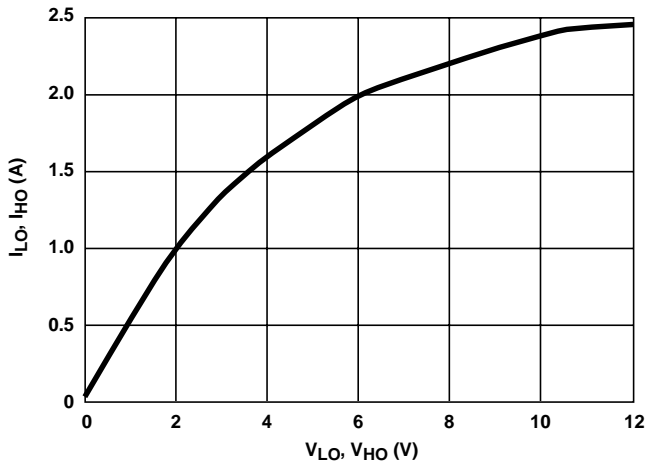


FIGURE 13. PULLDOWN CURRENT vs OUTPUT VOLTAGE

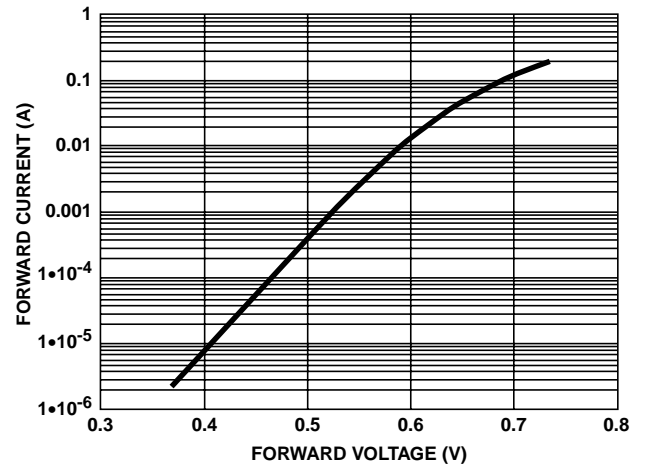


FIGURE 14. BOOTSTRAP DIODE I-V CHARACTERISTICS

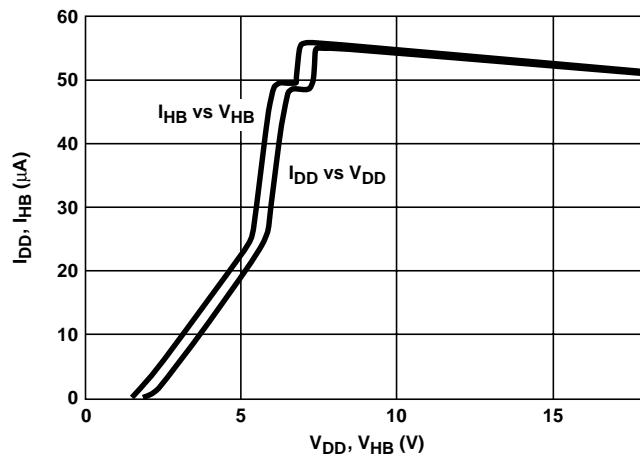


FIGURE 15. BIAS CURRENT vs VOLTAGE

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