



512K x 32 Static RAM

Features

- High speed
 - $t_{AA} = 8, 10, 12$ ns
- Low active power
 - 1080 mW (max.)
- Operating voltages of $3.3 \pm 0.3V$
- 2.0V data retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with \overline{CE}_1 , \overline{CE}_2 , and \overline{CE}_3 features

Functional Description

The CY7C1062AV33 is a high-performance CMOS Static RAM organized as 524,288 words by 32 bits.

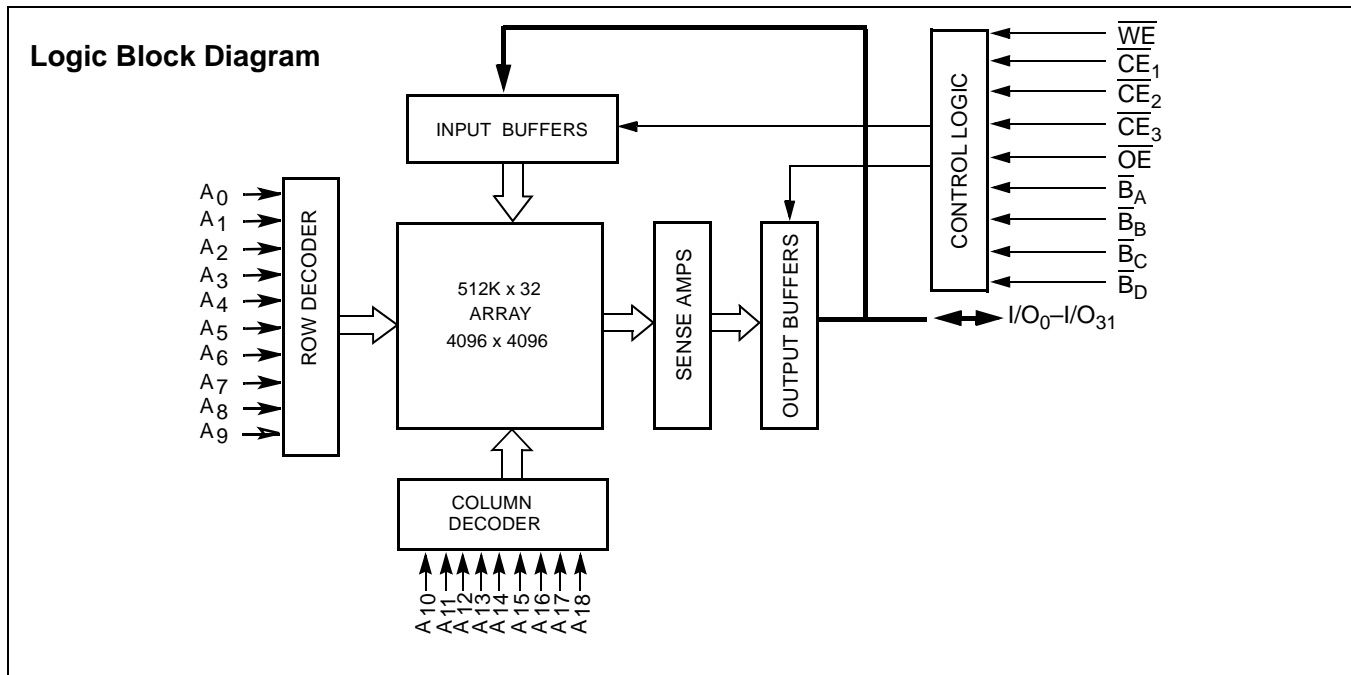
Writing to the device is accomplished by enabling the chip (\overline{CE}_1 , \overline{CE}_2 and \overline{CE}_3 LOW) and forcing the Write Enable (WE) input LOW. If Byte Enable A (\overline{B}_A) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on

the address pins (A_0 through A_{18}). If Byte Enable B (\overline{B}_B) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{18}). Likewise, \overline{B}_C and \overline{B}_D correspond with the I/O pins I/O_{16} to I/O_{23} and I/O_{24} to I/O_{31} , respectively.

Reading from the device is accomplished by enabling the chip (\overline{CE}_1 , \overline{CE}_2 , and \overline{CE}_3 LOW) while forcing the Output Enable (OE) LOW and Write Enable (WE) HIGH. If the first Byte Enable (\overline{B}_A) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7 . If Byte Enable B (\overline{B}_B) is LOW, then data from memory will appear on I/O_8 to I/O_{15} . Similarly, \overline{B}_C and \overline{B}_D correspond to the third and fourth bytes. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O_0 through I/O_{31}) are placed in a high-impedance state when the device is deselected (\overline{CE}_1 , \overline{CE}_2 or \overline{CE}_3 HIGH), the outputs are disabled (OE HIGH), the byte selects are disabled (\overline{B}_{A-D} HIGH), or during a write operation (\overline{CE}_1 , \overline{CE}_2 , and \overline{CE}_3 LOW, and WE LOW).

The CY7C1062AV33 is available in a 119-ball pitch ball grid array (PBGA) package.



Selection Guide

| | | -8 | -10 | -12 | Unit |
|------------------------------|-------------|-----|-----|-----|------|
| Maximum Access Time | | 8 | 10 | 12 | ns |
| Maximum Operating Current | Com'l | 300 | 275 | 260 | mA |
| | Ind'l | 300 | 275 | 260 | |
| Maximum CMOS Standby Current | Com'l/Ind'l | 50 | 50 | 50 | mA |

Pin Configuration
**119-ball PBGA
(Top View)**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|----------|-------------------|------------------|-------------------|-------------------|-------------------|------------------|-------------------|
| A | I/O ₁₆ | A | A | A | A | A | I/O ₀ |
| B | I/O ₁₇ | A | A | \overline{CE}_1 | A | A | I/O ₁ |
| C | I/O ₁₈ | \overline{B}_c | \overline{CE}_2 | NC | \overline{CE}_3 | \overline{B}_a | I/O ₂ |
| D | I/O ₁₉ | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | I/O ₃ |
| E | I/O ₂₀ | V _{SS} | V _{DD} | V _{SS} | V _{DD} | V _{SS} | I/O ₄ |
| F | I/O ₂₁ | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | I/O ₅ |
| G | I/O ₂₂ | V _{SS} | V _{DD} | V _{SS} | V _{DD} | V _{SS} | I/O ₆ |
| H | I/O ₂₃ | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | I/O ₇ |
| J | NC | V _{SS} | V _{DD} | V _{SS} | V _{DD} | V _{SS} | DNU |
| K | I/O ₂₄ | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | I/O ₈ |
| L | I/O ₂₅ | V _{SS} | V _{DD} | V _{SS} | V _{DD} | V _{SS} | I/O ₉ |
| M | I/O ₂₆ | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | I/O ₁₀ |
| N | I/O ₂₇ | V _{SS} | V _{DD} | V _{SS} | V _{DD} | V _{SS} | I/O ₁₁ |
| P | I/O ₂₈ | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | I/O ₁₂ |
| R | I/O ₂₉ | A | \overline{B}_d | NC | \overline{B}_b | A | I/O ₁₃ |
| T | I/O ₃₀ | A | A | \overline{WE} | A | A | I/O ₁₄ |
| U | I/O ₃₁ | A | A | \overline{OE} | A | A | I/O ₁₅ |

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with
 Power Applied -55°C to +125°C
 Supply Voltage on V_{CC} to Relative GND^[1] -0.5V to +4.6V
 DC Voltage Applied to Outputs
 in High-Z State^[1] -0.5V to V_{CC} + 0.5V

DC Input Voltage^[1] -0.5V to V_{CC} + 0.5V
 Current into Outputs (LOW) 20 mA

Operating Range

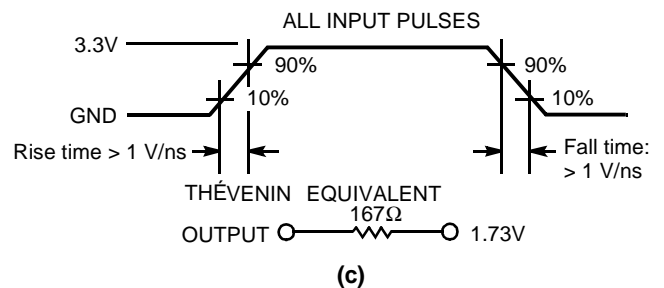
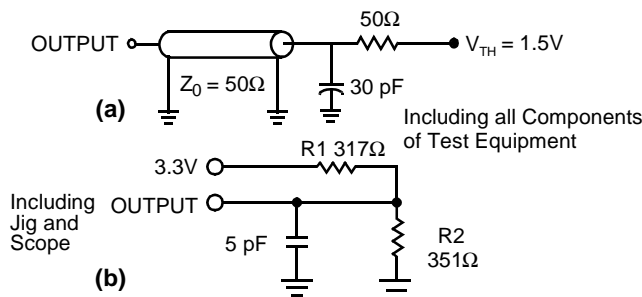
| Range | Ambient Temperature | V _{CC} |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C | 3.3V ± 0.3V |
| Industrial | -40°C to +85°C | |

DC Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | -8 | | -10 | | -12 | | Unit |
|------------------|--|---|-------------|-----------------------|------|-----------------------|------|-----------------------|------|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| V _{OH} | Output HIGH Voltage | V _{CC} = Min., I _{OH} = -4.0 mA | 2.4 | | 2.4 | | 2.4 | | V |
| V _{OL} | Output LOW Voltage | V _{CC} = Min., I _{OL} = 8.0 mA | | 0.4 | | 0.4 | | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | 2.0 | V _{CC} + 0.3 | 2.0 | V _{CC} + 0.3 | 2.0 | V _{CC} + 0.3 | V |
| V _{IL} | Input LOW Voltage ^[1] | | -0.3 | 0.8 | -0.3 | 0.8 | -0.3 | 0.8 | V |
| I _{IX} | Input Load Current | GND ≤ V _I ≤ V _{CC} | -1 | +1 | -1 | +1 | -1 | +1 | μA |
| I _{OZ} | Output Leakage Current | GND ≤ V _{OUT} ≤ V _{CC} , Output Disabled | -1 | +1 | -1 | +1 | -1 | +1 | μA |
| I _{CC} | V _{CC} Operating Supply Current | V _{CC} = Max., f = f _{MAX} = 1/t _{RC} | Com'l | | 275 | | 260 | | mA |
| | | | Ind'l | | 300 | | 260 | | mA |
| I _{SB1} | Automatic CE Power-down Current —TTL Inputs | Max. V _{CC} , CE ≥ V _{IH} V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX} | | 70 | | 70 | | 70 | mA |
| I _{SB2} | Automatic CE Power-down Current —CMOS Inputs | Max. V _{CC} , CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0 | Com'l/Ind'l | | 50 | | 50 | | mA |

Capacitance^[2]

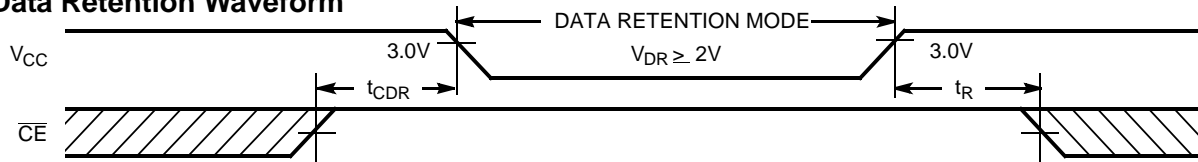
| Parameter | Description | Test Conditions | Max. | Unit |
|------------------|-------------------|--|------|------|
| C _{IN} | Input Capacitance | T _A = 25°C, f = 1 MHz, V _{CC} = 3.3V | 8 | pF |
| C _{OUT} | I/O Capacitance | | 10 | pF |

AC Test Loads and Waveforms^[3]

Notes:

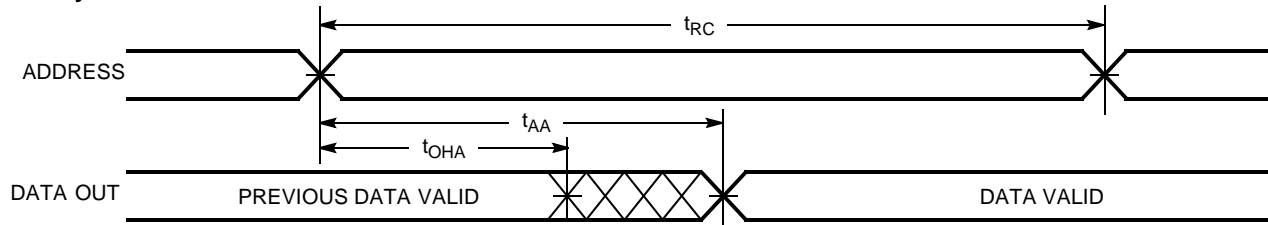
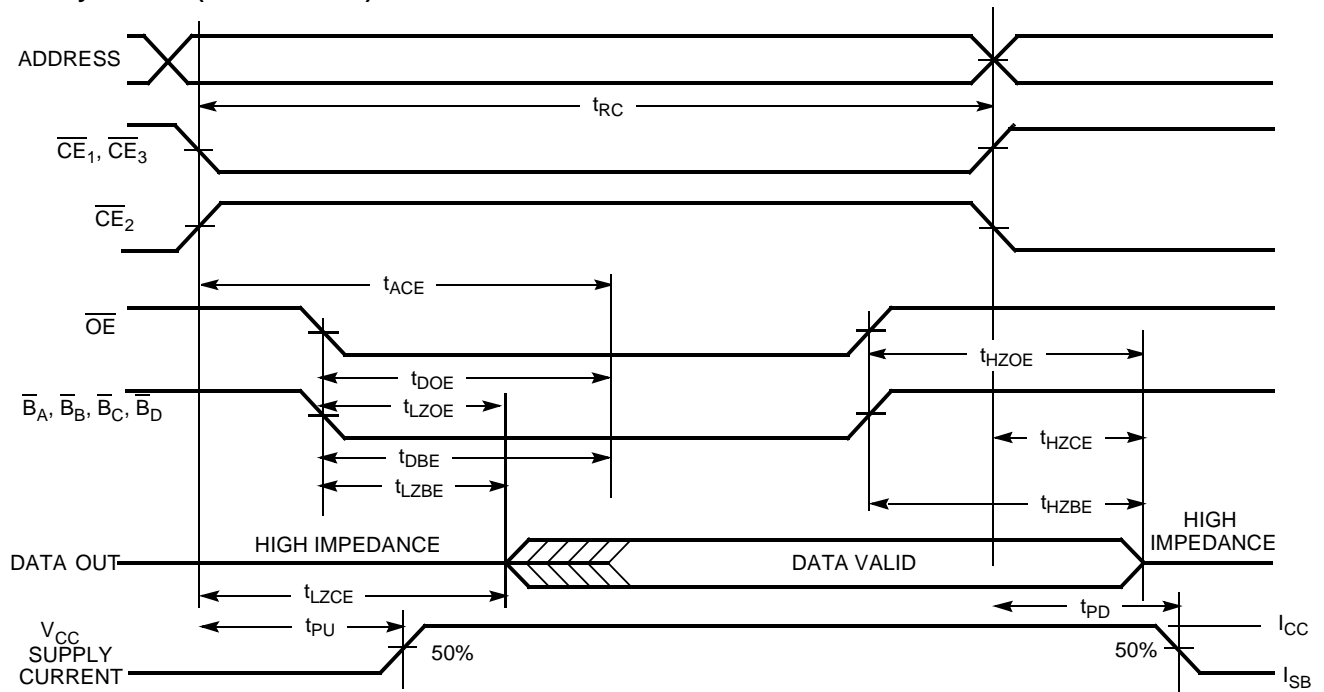
- V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.
- Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (3.0V). As soon as 1ms (T_{power}) after reaching the minimum operating V_{DD}, normal SRAM operation can begin including reduction in V_{DD} to the data retention (V_{CCDR}, 2.0V) voltage.

AC Switching Characteristics Over the Operating Range^[4]

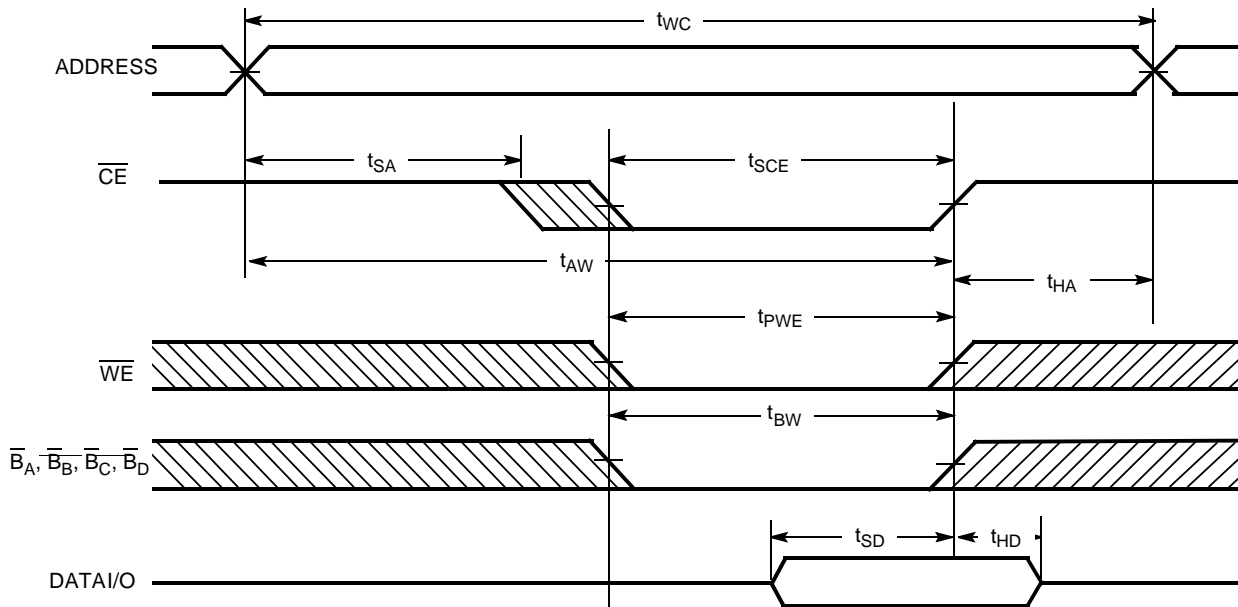
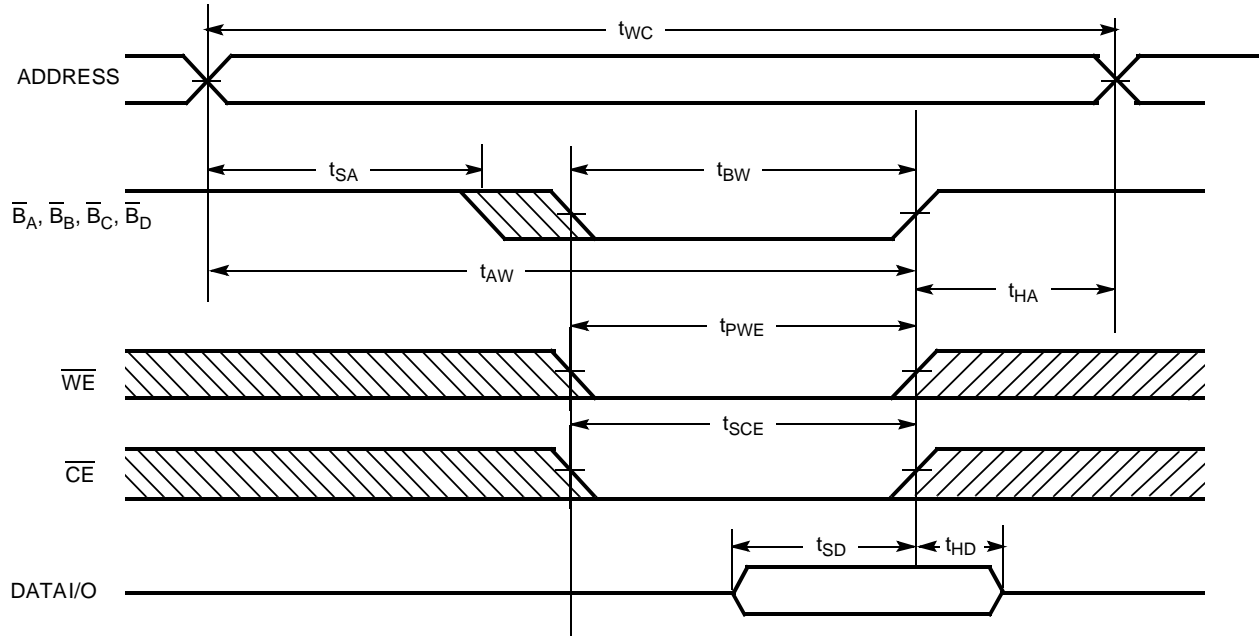
| Parameter | Description | -8 | | -10 | | -12 | | Unit |
|-------------------------------------|--|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Read Cycle | | | | | | | | |
| t_{power} | V_{CC} (typical) to the first access ^[5] | 1 | | 1 | | 1 | | ms |
| t_{RC} | Read Cycle Time | 8 | | 10 | | 12 | | ns |
| t_{AA} | Address to Data Valid | | 8 | | 10 | | 12 | ns |
| t_{OHA} | Data Hold from Address Change | 3 | | 3 | | 3 | | ns |
| t_{ACE} | \overline{CE}_1 , \overline{CE}_2 , or \overline{CE}_3 LOW to Data Valid | | 8 | | 10 | | 12 | ns |
| t_{DOE} | \overline{OE} LOW to Data Valid | | 5 | | 5 | | 6 | ns |
| t_{LZOE} | \overline{OE} LOW to Low-Z ^[6] | 1 | | 1 | | 1 | | ns |
| t_{HZOE} | \overline{OE} HIGH to High-Z ^[6] | | 5 | | 5 | | 6 | ns |
| t_{LZCE} | \overline{CE}_1 , \overline{CE}_2 , or \overline{CE}_3 LOW to Low-Z ^[6] | 3 | | 3 | | 3 | | ns |
| t_{HZCE} | \overline{CE}_1 , \overline{CE}_2 , or \overline{CE}_3 HIGH to High-Z ^[6] | | 5 | | 5 | | 6 | ns |
| t_{PU} | \overline{CE}_1 , \overline{CE}_2 , or \overline{CE}_3 LOW to Power-up ^[7] | 0 | | 0 | | 0 | | ns |
| t_{PD} | \overline{CE}_1 , \overline{CE}_2 , or \overline{CE}_3 HIGH to Power-down ^[7] | | 8 | | 10 | | 12 | ns |
| t_{DBE} | Byte Enable to Data Valid | | 5 | | 5 | | 6 | ns |
| t_{LZBE} | Byte Enable to Low-Z ^[6] | 1 | | 1 | | 1 | | ns |
| t_{HZBE} | Byte Disable to High-Z ^[6] | | 5 | | 5 | | 6 | ns |
| Write Cycle^[8, 9] | | | | | | | | |
| t_{WC} | Write Cycle Time | 8 | | 10 | | 12 | | ns |
| t_{SCE} | \overline{CE}_1 , \overline{CE}_2 , or \overline{CE}_3 LOW to Write End | 6 | | 7 | | 8 | | ns |
| t_{AW} | Address Set-up to Write End | 6 | | 7 | | 8 | | ns |
| t_{HA} | Address Hold from Write End | 0 | | 0 | | 0 | | ns |
| t_{SA} | Address Set-up to Write Start | 0 | | 0 | | 0 | | ns |
| t_{PWE} | \overline{WE} Pulse Width | 6 | | 7 | | 8 | | ns |
| t_{SD} | Data Set-up to Write End | 5 | | 5.5 | | 6 | | ns |
| t_{HD} | Data Hold from Write End | 0 | | 0 | | 0 | | ns |
| t_{LZWE} | \overline{WE} HIGH to Low-Z ^[6] | 3 | | 3 | | 3 | | ns |
| t_{HZWE} | \overline{WE} LOW to High-Z ^[6] | | 5 | | 5 | | 6 | ns |
| t_{BW} | Byte Enable to End of Write | 6 | | 7 | | 8 | | ns |

Data Retention Waveform

Notes:

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and transmission line loads. Test conditions for the read cycle use output loading as shown in (a) of AC Test Loads, unless specified otherwise.
- This part has a voltage regulator that steps down the voltage from 3V to 2V internally. t_{power} time has to be provided initially before a read/write operation is started.
- t_{HZOE} , t_{HZCE} , t_{HZWE} , t_{HZBE} , and t_{LZOE} , t_{LZCE} , t_{LZWE} , and t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
- These parameters are guaranteed by design and are not tested.
- The internal write time of the memory is defined by the overlap of \overline{CE}_1 LOW, \overline{CE}_2 HIGH, \overline{CE}_3 LOW, and \overline{WE} LOW. The chip enables must be active and \overline{WE} must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 (\overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

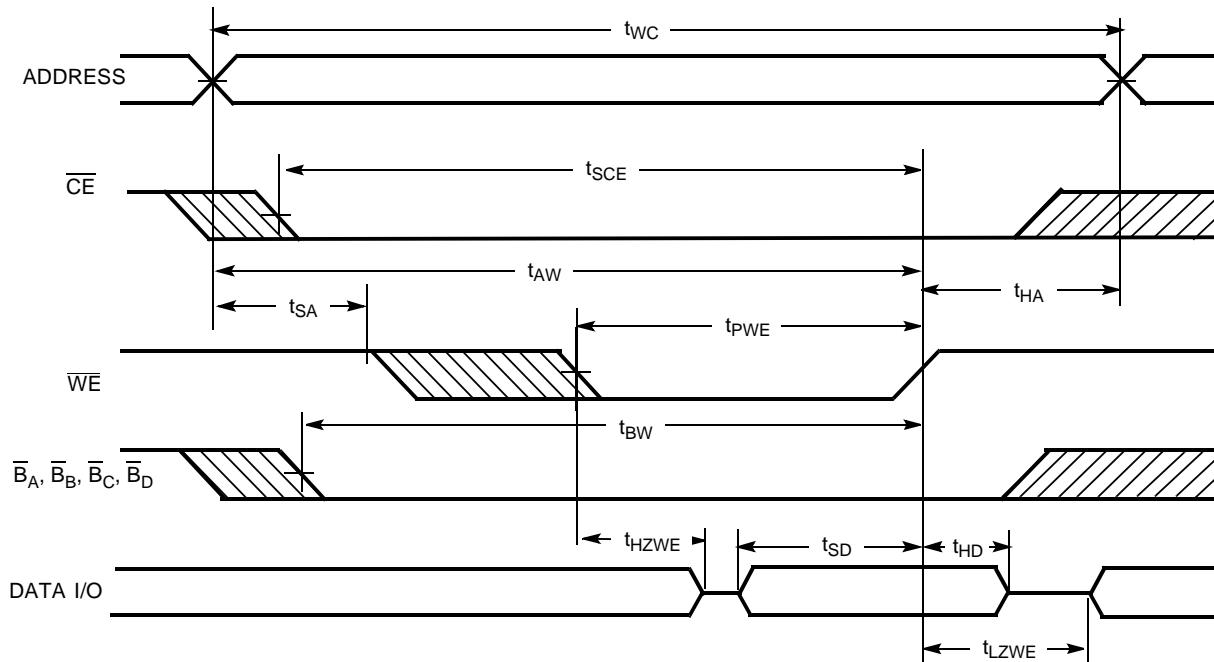
Switching Waveforms
Read Cycle No. 1 [10, 11]

Read Cycle No. 2 (\overline{OE} Controlled) [11, 12]

Notes:

10. Device is continuously selected. $\overline{OE}, \overline{CE}, \overline{BA}, \overline{BB}, \overline{BC}, \overline{BD} = V_{IL}$.
11. WE is HIGH for read cycle.
12. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)
Write Cycle No. 1 (\overline{CE} Controlled)^[13, 14, 15]

Write Cycle No. 2 (\overline{BLE} or \overline{BHE} Controlled)^[13, 14, 15]

Notes:

13. \overline{CE} indicates a combination of all three chip enables. When ACTIVE LOW, \overline{CE} indicates the \overline{CE}_1 , \overline{CE}_2 and \overline{CE}_3 are LOW.
14. Data I/O is high-impedance if \overline{OE} or $\overline{B_A}, \overline{B_B}, \overline{B_C}, \overline{B_D} = V_{IH}$.
15. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.

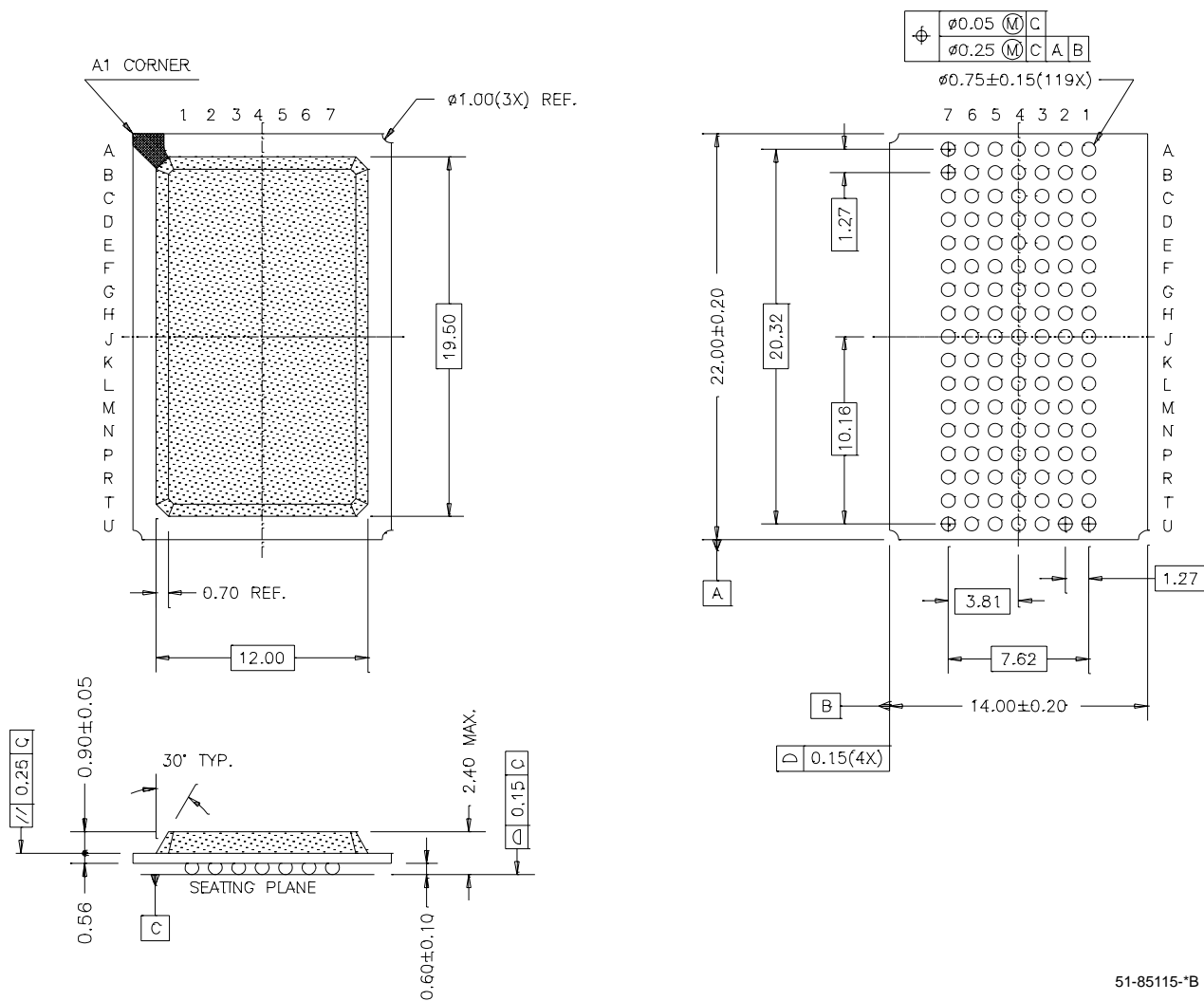
Switching Waveforms (continued)

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)

Truth Table

| \overline{CE}_1 | \overline{CE}_2 | \overline{CE}_3 | \overline{OE} | \overline{WE} | \overline{B}_A | \overline{B}_B | \overline{B}_C | \overline{B}_D | I/O ₀ ⁻ I/O ₇ | I/O ₈ ⁻ I/O ₁₅ | I/O ₁₆ ⁻ I/O ₂₃ | I/O ₂₄ ⁻ I/O ₃₁ | Mode | Power |
|-------------------|-------------------|-------------------|-----------------|-----------------|------------------|------------------|------------------|------------------|---|--|---|---|----------------------------|--------------------|
| H | L | H | X | X | X | X | X | X | High-Z | High-Z | High-Z | High-Z | Power Down | (I _{SB}) |
| L | H | L | X | X | X | X | X | X | High-Z | High-Z | High-Z | High-Z | Power Down | (I _{SB}) |
| L | L | L | L | H | L | L | L | L | Data Out | Data Out | Data Out | Data Out | Read All Bits | (I _{CC}) |
| L | L | L | L | H | L | H | H | H | Data Out | High-Z | High-Z | High-Z | Read Byte A Bits Only | (I _{CC}) |
| L | L | L | L | H | H | L | H | H | High-Z | Data Out | High-Z | High-Z | Read Byte B Bits Only | (I _{CC}) |
| L | L | L | L | H | H | H | L | H | High-Z | High-Z | Data Out | High-Z | Read Byte C Bits Only | (I _{CC}) |
| L | L | L | L | H | H | H | H | L | High-Z | High-Z | High-Z | Data Out | Read Byte D Bits Only | (I _{CC}) |
| L | L | L | X | L | L | L | L | L | Data In | Data In | Data In | Data In | Write All Bits | (I _{CC}) |
| L | L | L | X | L | L | H | H | H | Data In | High-Z | High-Z | High-Z | Write Byte A Bits Only | (I _{CC}) |
| L | L | L | X | L | H | L | H | H | High-Z | Data In | High-Z | High-Z | Write Byte B Bits Only | (I _{CC}) |
| L | L | L | X | L | H | H | L | H | High-Z | High-Z | Data In | High-Z | Write Byte C Bits Only | (I _{CC}) |
| L | L | L | X | L | H | H | H | L | High-Z | High-Z | High-Z | Data In | Write Byte D Bits Only | (I _{CC}) |
| L | L | L | H | H | X | X | X | X | High-Z | High-Z | High-Z | High-Z | Selected, Outputs Disabled | (I _{CC}) |

Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|--------------------|--------------|--------------------------|-----------------|
| 8 | CY7C1062AV33-8BGC | BG119 | 14 x 22 mm 119-ball PBGA | Commercial |
| | CY7C1062AV33-8BGI | | | Industrial |
| 10 | CY7C1062AV33-10BGC | | | Commercial |
| | CY7C1062AV33-10BGI | | | Industrial |
| 12 | CY7C1062AV33-12BGC | | | Commercial |
| | CY7C1062AV33-12BGI | | | Industrial |

Package Diagram
119-ball PBGA (14 x 22 x 2.4 mm) BG119


51-85115-B

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Document History Page

| Document Title: CY7C1062AV33 512K x 32 Static RAM | | | | |
|---|---------|------------|-----------------|--|
| Document Number: 38-05137 | | | | |
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 109752 | 02/27/02 | HGK | New Data Sheet |
| *A | 117059 | 09/19/02 | DFP | Removed 15-ns bin and added 8-ns bin. Changed CE ₂ TO CE ₂ . Changed C _{IN} – input capacitance – from 6 pF to 8 pF. Changed C _{OUT} – output capacitance – from 8 pF to 10 pF. |
| *B | 119389 | 10/07/02 | DFP | Updated I _{CC} , T _{sd} , and T _{doe} parameters. Removed note 7 (I _Z /h _Z comment). |
| *C | 120384 | 11/13/02 | DFP | Final Data Sheet. Removed note 2. Added note 3 to “AC Test Loads and Waveforms” and note 7 to t _{pu} and t _{pd} . |
| *D | 124440 | 2/25/03 | MEG | Changed ISB1 from 100 mA to 70 mA |