



# Pentium®/II, 6x86, K6 Clock Synthesizer/Driver for Desktop PCs with Intel 82430TX, 82440LX or ALI IV/IV+, AGP and 3 DIMMs

## Features

- Mixed 2.5V and 3.3V operation
- Complete clock solution for Pentium®, Pentium® II, Cyrix, and AMD processor-based motherboards
  - Four CPU clocks at 2.5V or 3.3V
  - Up to twelve 3.3V SDRAM clocks
  - Seven synchronous PCI clocks, one free-running
  - One 3.3V 48 MHz USB clock
  - One 2.5V IOAPIC clock (-3 option only)
  - Two AGP clocks at 60 or 66.6MHz (-2 option only)
  - One 3.3V Ref. clock at 14.318 MHz
- I<sup>2</sup>C™ Serial Configuration Interface
- Factory-EPROM programmable output drive and slew rate for EMI customization
- Factory-EPROM programmable CPU clock frequencies for custom configurations
- Power-down, CPU stop and PCI stop pins
- Available in space-saving 48-pin SSOP package

## Functional Description

The CY2273A is a clock synthesizer/driver for a Pentium, Pentium II, Cyrix, or AMD processor-based PC using Intel's 82430TX, 82440LX, ALI Aladdin IV or Aladdin IV+ chipsets.

The CY2273A-1 outputs four CPU clocks at 2.5V or 3.3V with up to 83.3MHz operation. There are seven PCI clocks, running at 30 and 33.3MHz. One of the PCI clocks is free-running. Additionally, the part outputs up to twelve 3.3V SDRAM clocks, one 3.3V USB clock at 48 MHz, and one 3.3V reference clock at 14.318 MHz. The CY2273A-2 is similar, except that PCICLK4 and PCICLK5 are now AGP clocks. The CY2273A-3 is more suited to Pentium II systems, as it outputs one 2.5V IOAPIC clock. Finally, the CY2273A-4 is similar to the CY2273A-1 except that it supports 0-ns CPU-PCI delay.

The CY2273A possesses power-down, CPU stop, and PCI stop pins for power management control. These inputs are multiplexed with SDRAM clock outputs, and are selected when the MODE pin is driven low. Additionally, the signals are synchronized on-chip, and ensure glitch-free transitions on the outputs. When the CPU\_STOP input is asserted, the CPU clock outputs are driven LOW. When the PCI\_STOP input is asserted, the PCI clock outputs (except the free-running PCI clock) are driven LOW. When the PWR\_DWN pin is asserted, the reference oscillator and PLLs are shut down, and all outputs are driven LOW.

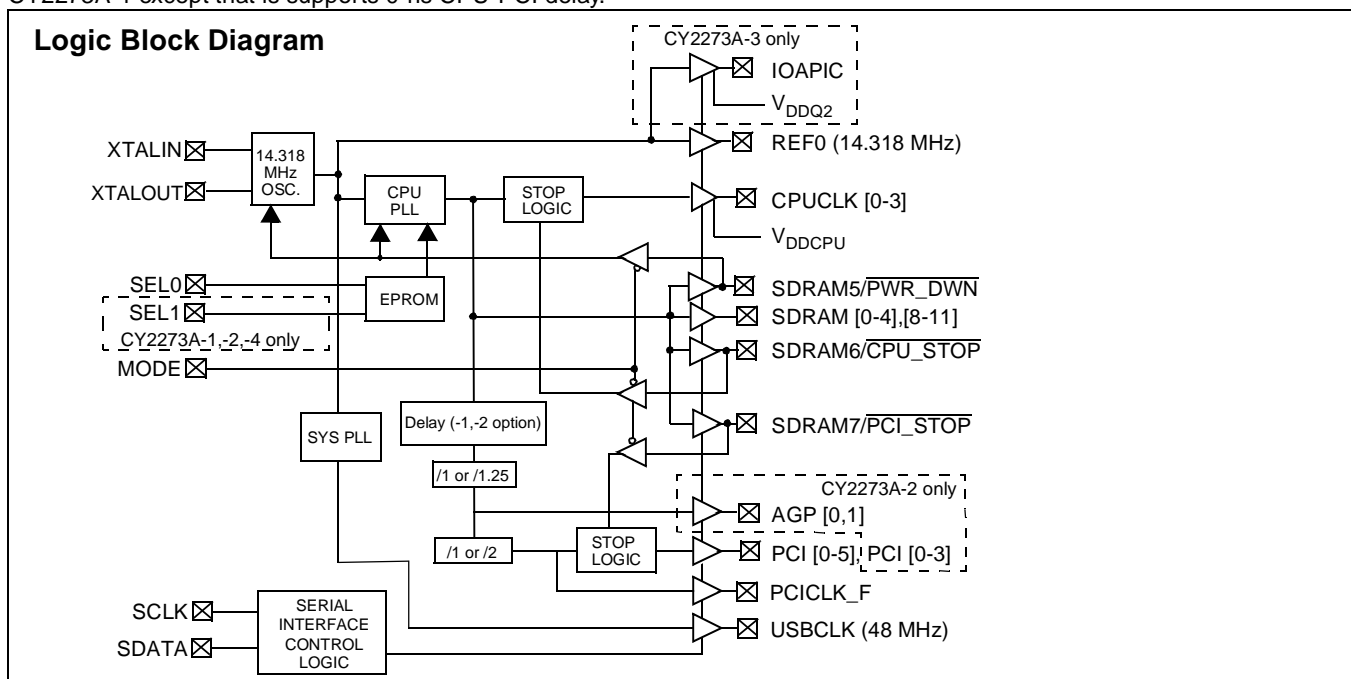
The CY2273A outputs are designed for low EMI emissions. Controlled rise and fall times, unique output driver circuits and factory-EPROM programmable output drive and slew-rate enable optimal configurations for EMI control.

## CY2273A Selector Guide

Clocks Outputs	-1	-2	-3	-4
CPU (60, 66.6, 75, 83.3 MHz)	4	4	--	4
CPU (60, 66.6 MHz)	--	--	4	--
SDRAM	9/12	9/12	9/12	9/12
PCI (30, 33.3MHz)	7 <sup>[1]</sup>	5 <sup>[1]</sup>	7 <sup>[1]</sup>	7 <sup>[1]</sup>
USB/IR (48MHz)	1	1	1	1
AGP (60 or 66MHz)	--	2	--	--
IOAPIC (14.318MHz)	--	--	1	--
Ref (14.318MHz)	1	1	1	1
CPU-PCI delay	1–5.5 ns	1–5.5 ns	0 ns	0 ns

### Note:

1. One free-running PCI clock.



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**Pin Configurations**
**CY2273A-1,-4**  
**SSOP**  
**Top View**

AVDD	1	48	VDDQ3
REF0	2	47	USBCLK
VSS	3	46	SEL1
XTALIN	4	45	VSS
XTALOUT	5	44	CPUCLK0
VDDQ3	6	43	CPUCLK1
PCICLK_F	7	42	VDDCPU
PCICLK0	8	41	CPUCLK2
VSS	9	40	CPUCLK3
PCICLK1	10	39	VSS
PCICLK2	11	38	SDRAM0
PCICLK3	12	37	SDRAM1
PCICLK4	13	36	VDDQ3
VDDQ3	14	35	SDRAM2
PCICLK5	15	34	SDRAM3
VSS	16	33	VSS
SDRAM11	17	32	SDRAM4
SDRAM10	18	31	SDRAM5/PWR_DWN
VDDQ3	19	30	VDDQ3
SDRAM9	20	29	SDRAM6/CPU_STOP
SDRAM8	21	28	SDRAM7/PCI_STOP
VSS	22	27	VSS
SDATA	23	26	SEL0
SCLK	24	25	MODE

**CY2273A-2**  
**SSOP**  
**Top View**

AVDD	1	48	VDDQ3
REF0	2	47	USBCLK
VSS	3	46	SEL1
XTALIN	4	45	VSS
XTALOUT	5	44	CPUCLK0
VDDQ3	6	43	CPUCLK1
PCICLK_F	7	42	VDDCPU
PCICLK0	8	41	CPUCLK2
VSS	9	40	CPUCLK3
PCICLK1	10	39	VSS
PCICLK2	11	38	SDRAM0
PCICLK3	12	37	SDRAM1
AGP0	13	36	VDDQ3
VDDQ3	14	35	SDRAM2
AGP1	15	34	SDRAM3
VSS	16	33	VSS
SDRAM11	17	32	SDRAM4
SDRAM10	18	31	SDRAM5/PWR_DWN
VDDQ3	19	30	VDDQ3
SDRAM9	20	29	SDRAM6/CPU_STOP
SDRAM8	21	28	SDRAM7/PCI_STOP
VSS	22	27	VSS
SDATA	23	26	SEL0
SCLK	24	25	MODE

**CY2273A-3**  
**SSOP**  
**Top View**

USBCLK	1	48	VDDQ2
REF0	2	47	IOAPIC
VSS	3	46	SEL0
XTALIN	4	45	VSS
XTALOUT	5	44	CPUCLK0
VDDQ3	6	43	CPUCLK1
PCICLK_F	7	42	VDDCPU
PCICLK0	8	41	CPUCLK2
VSS	9	40	CPUCLK3
PCICLK1	10	39	VSS
PCICLK2	11	38	SDRAM0
PCICLK3	12	37	SDRAM1
PCICLK4	13	36	VDDQ3
VDDQ3	14	35	SDRAM2
PCICLK5	15	34	SDRAM3
VSS	16	33	VSS
SDRAM11	17	32	SDRAM4
SDRAM10	18	31	SDRAM5/PWR_DWN
VDDQ3	19	30	VDDQ3
SDRAM9	20	29	SDRAM6/CPU_STOP
SDRAM8	21	28	SDRAM7/PCI_STOP
VSS	22	27	VSS
AVDD	23	26	MODE
SDATA	24	25	SCLK

**Pin Summary**

Name	Pins (-1, -4)	Pins (-2)	Pins (-3)	Description
V <sub>DDQ3</sub>	6, 14, 19, 30, 36, 48	6, 14, 19, 30, 36, 48	6, 14, 19, 30, 36	3.3V Digital voltage supply
V <sub>DDQ2</sub>	N/A	N/A	48	IOAPIC Digital voltage supply, 2.5V
V <sub>DDCPU</sub>	42	42	42	CPU Digital voltage supply, 2.5V or 3.3V
AV <sub>DD</sub>	1	1	23	Analog voltage supply, 3.3V
V <sub>SS</sub>	3, 9, 16, 22, 27, 33, 39, 45	3, 9, 16, 22, 27, 33, 39, 45	3, 9, 16, 22, 27, 33, 39, 45	Ground
XTALIN <sup>[2]</sup>	4	4	4	Reference crystal input
XTALOUT <sup>[2]</sup>	5	5	5	Reference crystal feedback
SDRAM7/ PCI_STOP	28	28	28	SDRAM clock output. Also, active low control input to stop PCI clocks, enabled when MODE is LOW.
SDRAM6/ CPU_STOP	29	29	29	SDRAM clock output. Also, active low control input to stop CPU clocks, enabled when MODE is LOW.
SDRAM5/ PWR_DWN	31	31	31	SDRAM clock output. Also, active low control input to power down device, enabled when MODE is LOW.
SDRAM[0:4], [8:11]	38, 37, 35, 34, 32, 21, 20, 18, 17	38, 37, 35, 34, 32, 21, 20, 18, 17	38, 37, 35, 34, 32, 21, 20, 18, 17	SDRAM clock outputs
SEL0	26	26	46	CPU frequency select input, bit 0 (See table below.)
SEL1	46	46	N/A	CPU frequency select input, bit 0 (See table below.)
CPUCLK[0:3]	44, 43, 41, 40	44, 43, 41, 40	44, 43, 41, 40	CPU clock outputs
PCICLK[0:5]or PCICLK[0:3]	8, 10, 11, 12, 13, 15	8, 10, 11, 12	8, 10, 11, 12, 13, 15	PCI clock outputs, at 30 or 33.33 MHz
PCICLK_F	7	7	7	Free-running PCI clock output
AGPCLK[0:1]	N/A	13, 15	N/A	AGP clock outputs at 60 or 66.66 MHz
IOAPIC	N/A	N/A	47	IOAPIC clock output
REF0	2	2	2	3.3V Reference clock output
USBCLK	47	47	1	USB Clock output at 48 MHz
SDATA	23	23	24	Serial data input for serial configuration port
SCLK	24	24	25	Serial clock input for serial configuration port
MODE	25	25	26	Mode Select pin for enabling power management features

**Note:**

2. For best accuracy, use a parallel-resonant crystal, C<sub>LOAD</sub> = 18 pF.

**Function Table (-1, -2 and -4)**

SEL1	SEL0	CPU/PCI Ratio	CPUCLK[0:3] SDRAM[0:11]	PCICLK[0:5] PCICLK_F	AGP (-2 Only)	REF0 IOAPIC	USBCLK
0	0	2	60.0 MHz	30.0 MHz	60.0 MHz	14.318 MHz	48 MHz
0	1	2	66.67 MHz	33.33 MHz	66.66 MHz	14.318 MHz	48 MHz
1	0	2.5	75.0 MHz	30.0 MHz	60.0 MHz	14.318 MHz	48 MHz
1	1	2.5	83.33 MHz	33.33 MHz	66.66 MHz	14.318 MHz	48 MHz

**Function Table (-3)**

SEL0	CPU/PCI Ratio	CPUCLK[0:3]/SDRAM[0:11]	PCICLK[0:5],PCICLK_F	REF0/IOAPIC	USBCLK
0	2	60.0 MHz	30.0 MHz	14.318 MHz	48 MHz
1	2	66.67 MHz	33.33 MHz	14.318 MHz	48 MHz

**Actual Clock Frequency Values**

Clock Output	Target Frequency (MHz)	Actual Frequency (MHz)	PPM
CPUCLK	66.67	66.654	-195
CPUCLK	60.0	60.0	0
CPUCLK	75.0	75.0	0
CPUCLK	83.33	83.138	-1947
USBCLK	48.0	48.008	167

- Output impedance: 25Ω (typical) measured at 1.5V

**Power Management Logic<sup>[3]</sup> - Active when MODE pin is held 'LOW'**

$\overline{\text{CPU\_STOP}}$	$\overline{\text{PCI\_STOP}}$	$\overline{\text{PWR\_DWN}}$	CPUCLK	PCICLK	PCICLK_F	Other Clocks	Osc.	PLLs
X	X	0	Low	Low	Stopped	Stopped	Off	Off
0	0	1	Low	Low	Running	Running	Running	Running
0	1	1	Low	33/30 MHz	Running	Running	Running	Running
1	0	1	60/66/75/83 MHz	Low	Running	Running	Running	Running
1	1	1	60/66/75/83 MHz	30/33/30/33 MHz	Running	Running	Running	Running

**Serial Configuration Map**

- The Serial bits will be read by the clock driver in the following order:
  - Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0
  - Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0
  - ...
  - Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0
- Reserved and unused bits should be programmed to "0".
- I<sup>2</sup>C Address for the CY2273 is:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	----

**Byte 0: Functional and Frequency Select Clock Register (1 = Enable, 0 = Disable)**

Bit	Pin #	Description	
Bit 7	--	(Reserved) drive to '0'	
Bit 6	--	(Reserved) drive to '0'	
Bit 5	--	(Reserved) drive to '0'	
Bit 4	--	(Reserved) drive to '0'	
Bit 3	--	(Reserved) drive to '0'	
Bit 2	--	(Reserved) drive to '0'	
Bit 1 Bit 0	--	Bit 1 1 1 0 0	Bit 0 1 - Three-State 0 - N/A 1 - Testmode 0 - Normal Operation

**Select Functions**

Functional Description	Outputs					-2 only	
	CPU	PCI, PCI_F	SDRAM	Ref	IOAPIC	USBCLK	AGP
Three-State	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Test Mode <sup>[5]</sup>	TCLK/2 <sup>[4]</sup>	TCLK/4	TCLK/2	TCLK	TCLK	TCLK/2	TCLK/2

**Notes:**

- AGP clocks are driven on PCICLK5 and PCICLK4 on -2 option. These clocks behave similar to the PCICLK\_F output, in that they are free-running and stop only when the PWR\_DWN pin is asserted. The frequency of the AGP clocks is as shown in the Function Table.
- TCLK supplied on the XTALIN pin in Test Mode.
- Valid only for SEL1=0.

**Byte 1: CPU Active/Inactive Register  
(1 = Active, 0 = Inactive), Default = Active**

Bit	Pin #	Description
Bit 7	47 (-1,-2, and -4) 1 (-3 only)	USBCLK
Bit 6	N/A	(Reserved) drive to '0'
Bit 5	N/A	(Reserved) drive to '0'
Bit 4	N/A	Not used - drive to '0'
Bit 3	40	CPUCLK3 (Active/Inactive)
Bit 2	41	CPUCLK2 (Active/Inactive)
Bit 1	43	CPUCLK1 (Active/Inactive)
Bit 0	44	CPUCLK0 (Active/Inactive)

**Byte 3: SDRAM Active/Inactive Register  
(1 = Active, 0 = Inactive), Default = Active**

Bit	Pin #	Description
Bit 7	28	SDRAM7 (Active/Inactive)
Bit 6	29	SDRAM6 (Active/Inactive)
Bit 5	31	SDRAM5 (Active/Inactive)
Bit 4	32	SDRAM4 (Active/Inactive)
Bit 3	34	SDRAM3 (Active/Inactive)
Bit 2	35	SDRAM2 (Active/Inactive)
Bit 1	37	SDRAM1 (Active/Inactive)
Bit 0	38	SDRAM0 (Active/Inactive)

**Byte 5: Peripheral Active/Inactive Register  
(1 = Active, 0 = Inactive), Default = Active**

Bit	Pin #	Description
Bit 7	N/A	(Reserved) drive to '0'
Bit 6	N/A	(Reserved) drive to '0'
Bit 5	N/A	(Reserved) drive to '0'
Bit 4	47	IOAPIC (Active/Inactive) (-3 only)
Bit 3	N/A	(Reserved) drive to '0'
Bit 2	N/A	(Reserved) drive to '0'
Bit 1	N/A	(Reserved) drive to '0'
Bit 0	2	REF0 (Active/Inactive)

**Byte 2: PCI Active/Inactive Register  
(1 = Active, 0 = Inactive), Default = Active**

Bit	Pin #	Description
Bit 7	--	(Reserved) drive to '0'
Bit 6	7	PCICLK_F (Active/Inactive)
Bit 5	15	PCICLK5 (Active/Inactive) (-1,-3 and -4) AGP1 (Active/Inactive) (-2 only)
Bit 4	13	PCICLK4 (Active/Inactive) (-1,-3 and -4) AGP0 (Active/Inactive) (-2 only)
Bit 3	12	PCICLK3 (Active/Inactive)
Bit 2	11	PCICLK2 (Active/Inactive)
Bit 1	10	PCICLK1 (Active/Inactive)
Bit 0	8	PCICLK0 (Active/Inactive)

**Byte 4: SDRAM Active/Inactive Register  
(1 = Active, 0 = Inactive), Default = Active**

Bit	Pin #	Description
Bit 7	N/A	Not used - drive to '0'
Bit 6	N/A	Not used - drive to '0'
Bit 5	N/A	Not used - drive to '0'
Bit 4	N/A	Not used - drive to '0'
Bit 3	17	SDRAM11
Bit 2	18	SDRAM10
Bit 1	20	SDRAM9
Bit 0	21	SDRAM8

**Byte 6: Reserved, for future use**

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... -0.5 to +7.0V  
 Input Voltage ..... -0.5V to  $V_{DD}+0.5$

Storage Temperature (Non-Condensing) ... -65°C to +150°C  
 Max. Soldering Temperature (10 sec) ..... +260°C  
 Junction Temperature ..... +150°C  
 Package Power Dissipation ..... 1W  
 Static Discharge Voltage ..... >2000V  
 (per MIL-STD-883, Method 3015, like  $V_{DD}$  pins tied together)

**Operating Conditions<sup>[6]</sup>**

Parameter	Description	Min.	Max.	Unit
$AV_{DD}, V_{DDQ3}$	Analog and Digital Supply Voltage	3.135	3.465	V
$V_{DDCPU}$	CPU Supply Voltage	2.375 3.135	2.9 3.465	V
$V_{DDQ2}$	IOAPIC Supply Voltage	2.375	2.9	V
$T_A$	Operating Temperature, Ambient	0	70	°C
$C_L$	Max. Capacitive Load on CPUCLK, USBCLK, IOAPIC PCICLK, AGP(-2 only), SDRAM REF0	10 30, 20 20	20 30 45	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
$V_{IH}$	High-level Input Voltage	Except Crystal Inputs	2.0		V
$V_{IL}$	Low-level Input Voltage	Except Crystal Inputs		0.8	V
$V_{ILic}$	Low-level Input Voltage	I <sup>2</sup> C inputs only		0.7	V
$V_{OH}$	High-level Output Voltage	$V_{DDCPU} = V_{DDQ2} = 2.375V$	2.0		V
		$I_{OH} = 16\text{ mA}$ CPUCLK $I_{OH} = 18\text{ mA}$ IOAPIC			
$V_{OL}$	Low-level Output Voltage	$V_{DDCPU} = V_{DDQ2} = 2.375V$		0.4	V
		$I_{OL} = 27\text{ mA}$ CPUCLK $I_{OL} = 29\text{ mA}$ IOAPIC			
$V_{OH}$	High-level Output Voltage	$V_{DDQ3}, AV_{DD}, V_{DDCPU} = 3.135V$	2.4		V
		$I_{OH} = 16\text{ mA}$ CPUCLK			
		$I_{OH} = 36\text{ mA}$ SDRAM			
		$I_{OH} = 32\text{ mA}$ PCICLK			
		$I_{OH} = 26\text{ mA}$ USBCLK			
		$I_{OH} = 36\text{ mA}$ REF0			
$V_{OL}$	Low-level Output Voltage	$V_{DDQ3}, AV_{DD}, V_{DDCPU} = 3.135V$		0.4V	V
		$I_{OL} = 27\text{ mA}$ CPUCLK			
		$I_{OL} = 29\text{ mA}$ SDRAM			
		$I_{OL} = 26\text{ mA}$ PCICLK			
		$I_{OL} = 21\text{ mA}$ USBCLK			
		$I_{OL} = 29\text{ mA}$ REF0			
$I_{IH}$	Input High Current	$V_{IH} = V_{DD}$	-10	+10	μA
$I_{IL}$	Input Low Current	$V_{IL} = 0V$		10	μA
$I_{OZ}$	Output Leakage Current	Three-state	-10	+10	μA
$I_{DD}$	Power Supply Current <sup>[7]</sup>	$V_{DD} = 3.465V, V_{IN} = 0$ or $V_{DD}$ , Loaded Outputs, CPU = 66.67 MHz		300	mA
$I_{DD}$	Power Supply Current <sup>[7]</sup>	$V_{DD} = 3.465V, V_{IN} = 0$ or $V_{DD}$ , Unloaded Outputs		120	mA
$I_{DDS}$	Power-down Current	Current draw in power-down state		500	μA

**Notes:**

6. Electrical parameters are guaranteed with these operating conditions.
7. Power supply current will vary with number of outputs which are running.

**Switching Characteristics for CY2273A-1, CY2273A-2<sup>[8]</sup> Over the Operating Range**

Parameter	Output	Description	Test Conditions	Min.	Typ.	Max.	Unit
t <sub>1</sub>	All	Output Duty Cycle <sup>[9, 10]</sup>	t <sub>1</sub> = t <sub>1A</sub> ÷ t <sub>1B</sub>	45	50	55	%
t <sub>2</sub>	CPUCLK	CPU Clock Rising and Falling Edge Rate <sup>[10]</sup>	Between 0.4V and 2.0V, V <sub>DDCPU</sub> = 2.5V Between 0.4V and 2.4V, V <sub>DDCPU</sub> = 3.3V	0.75		4.0	V/ns
t <sub>2</sub>	SDRAM, PCI, REF0, USB	SDRAM, PCI, REF0 Clock Rising and Falling Edge Rate <sup>[10]</sup>	Between 0.4V and 2.4V	0.85		4.0	V/ns
t <sub>2</sub>	AGP (-2 only)	AGP Rising and Falling Edge Rate	Between 0.4V and 2.4V	0.85		4.0	V/ns
t <sub>3</sub>	CPUCLK	CPU Clock Rise Time	Between 0.4V and 2.0V, V <sub>DDCPU</sub> = 2.5V Between 0.4V and 2.4V, V <sub>DDCPU</sub> = 3.3V	0.4 0.5		2.13 2.67	ns
t <sub>4</sub>	CPUCLK	CPU Clock Fall Time	Between 2.0V and 0.4V, V <sub>DDCPU</sub> = 2.5V Between 2.4V and 0.4V, V <sub>DDCPU</sub> = 3.3V	0.4 0.5		2.13 2.67	ns
t <sub>5</sub>	CPUCLK	CPU-CPU Clock Skew	Measured at 1.25V, V <sub>DDCPU</sub> = 2.5V Measured at 1.5V, V <sub>DDCPU</sub> = 3.3V		100	250	ps
t <sub>6</sub>	CPUCLK, PCICLK	CPU-PCI Clock Skew	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks	1.0	3.0	5.5	ns
t <sub>7</sub>	CPUCLK, SDRAM	CPU-SDRAM Clock Skew <sup>[10]</sup>	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks			650	ps
t <sub>8</sub>	PCICLK, PCICLK	PCI-PCI Clock Skew	Measured at 1.5V			500	ps
t <sub>9</sub>	PCICLK, AGP (-2 only)	PCICLK-AGP Clock Skew (-2 only)	Measured at 1.5V			500	ps
t <sub>10</sub>	CPUCLK, SDRAM	Cycle-Cycle Clock Jitter <sup>[10]</sup>	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks			250	ps
t <sub>10</sub>	PCICLK, AGP (-2 only)	Cycle-Cycle Clock Jitter <sup>[10]</sup>	Measured at 1.5V			500	ps
t <sub>11</sub>	CPUCLK, PCICLK, AGP (-2 only), SDRAM	Power-up Time	CPU, PCI, AGP, and SDRAM clock stabilization from power-up			3	ms

**Notes:**

8. All parameters specified with loaded outputs.
9. Duty cycle is measured at 1.5V when V<sub>DD</sub> = 3.3V. When V<sub>DDCPU</sub> = 2.5V, CPUCLK duty cycle is measured at 1.25V.
10. Measured at CPU=66.6 MHz, SDRAM=66.6 MHz, PCI=33.3 MHz, AGP=66.6 MHz.

**Switching Characteristics for CY2273A-3<sup>[8]</sup> Over the Operating Range**

Parameter	Output	Description	Test Conditions	Min.	Typ.	Max.	Unit
t <sub>1</sub>	All	Output Duty Cycle <sup>[9]</sup>	$t_1 = t_{1A} \div t_{1B}$	45	50	55	%
t <sub>2</sub>	CPUCLK, IOAPIC	CPU and IOAPIC Clock Rising and Falling Edge Rate	Between 0.4V and 2.0V, V <sub>DDCPU</sub> = 2.5V Between 0.4V and 2.4V, V <sub>DDCPU</sub> = 3.3V	0.75	1.0	4.0	V/ns
t <sub>2</sub>	REF0 USBCLK	REF0 and USBCLK Rising and Falling Edge Rate	Between 0.4V and 2.4V	1.0		4.0	V/ns
t <sub>2</sub>	SDRAM PCI	SDRAM and PCI Clock Rising and Falling Edge Rate	Between 0.4V and 2.4V	0.85	1.0	4.0	V/ns
t <sub>3</sub>	CPUCLK	CPU Clock Rise Time	Between 0.4V and 2.0V, V <sub>DDCPU</sub> = 2.5V Between 0.4V and 2.4V, V <sub>DDCPU</sub> = 3.3V	0.4 0.5		2.13 2.67	ns
t <sub>4</sub>	CPUCLK	CPU Clock Fall Time	Between 2.0V and 0.4V, V <sub>DDCPU</sub> = 2.5V Between 2.4V and 0.4V, V <sub>DDCPU</sub> = 3.3V	0.4 0.5		2.13 2.67	ns
t <sub>5</sub>	CPUCLK	CPU-CPU Clock Skew	Measured at 1.25V, V <sub>DDCPU</sub> = 2.5V Measured at 1.5V, V <sub>DDCPU</sub> = 3.3V		100	300	ps
t <sub>6</sub>	CPUCLK, PCICLK	CPU-PCI Clock Skew	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks			900	ps
t <sub>7</sub>	CPUCLK, SDRAM	CPU-SDRAM Clock Skew	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks			600	ps
t <sub>8</sub>	PCICLK, PCICLK	PCI-PCI Clock Skew	Measured at 1.5V			500	ps
t <sub>10</sub>	CPUCLK, SDRAM	Cycle-Cycle Clock Jitter	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks			750	ps
t <sub>10</sub>	PCICLK	Cycle-Cycle Clock Jitter	Measured at 1.5V			500	ps
t <sub>11</sub>	CPUCLK, PCICLK, SDRAM	Power-up Time	CPU, PCI, AGP, and SDRAM clock stabilization from power-up			3	ms

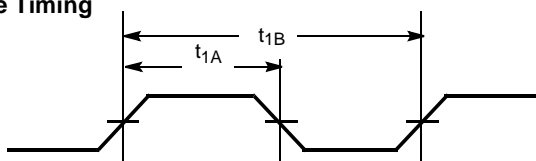


**Switching Characteristics for CY2273A-4<sup>[8]</sup> Over the Operating Range**

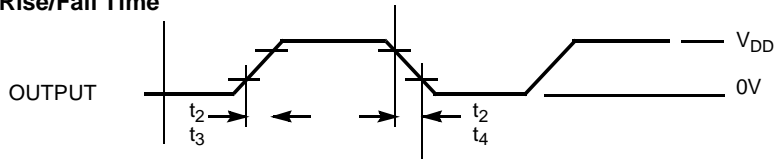
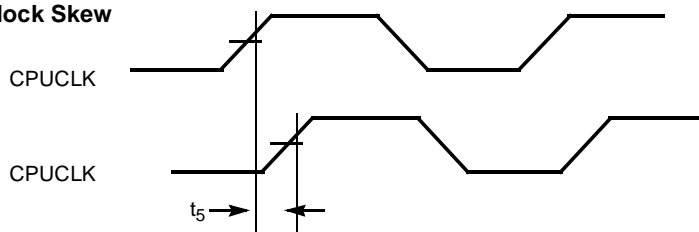
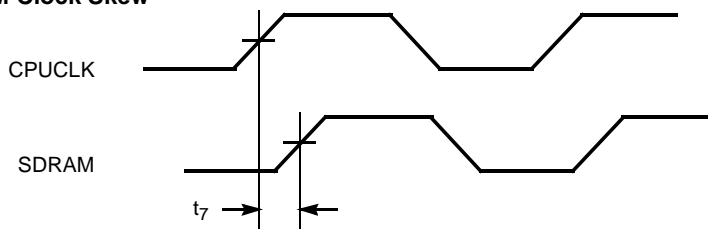
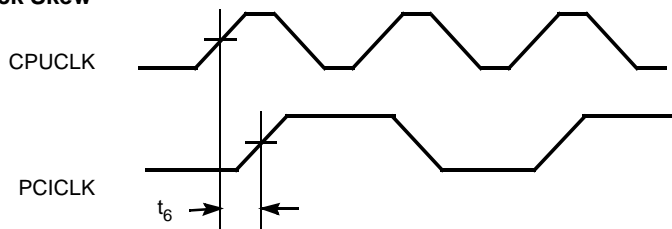
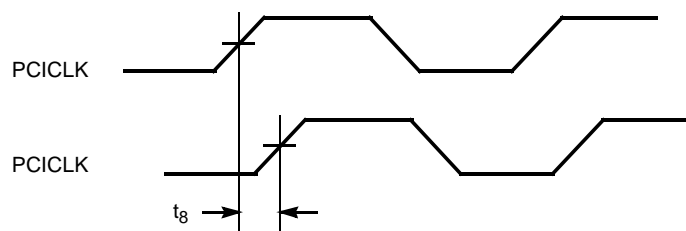
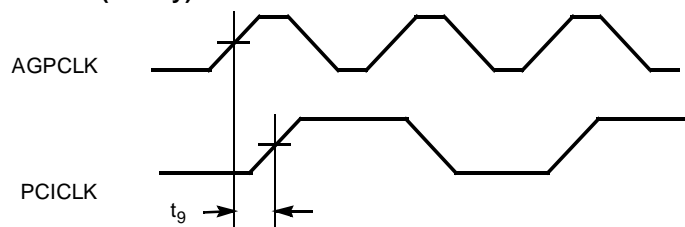
Parameter	Output	Description	Test Conditions	Min.	Typ.	Max.	Unit
t <sub>1</sub>	All	Output Duty Cycle <sup>[9]</sup>	t <sub>1</sub> = t <sub>1A</sub> ÷ t <sub>1B</sub>	45	50	55	%
t <sub>2</sub>	CPUCLK	CPU Clock Rising and Falling Edge Rate	Between 0.4V and 2.0V, V <sub>DDCPU</sub> = 2.5V	0.75	1.0	4.0	V/ns
t <sub>2</sub>	SDRAM, PCI, REF0, USB	SDRAM, PCI, REF0, USB Clock Rising and Falling Edge Rate	Between 0.4V and 2.4V	0.85	1.0	4.0	V/ns
t <sub>3</sub>	CPUCLK	CPU Clock Rise Time	Between 0.4V and 2.0V, V <sub>DDCPU</sub> = 2.5V	0.4		2.13	ns
t <sub>4</sub>	CPUCLK	CPU Clock Fall Time	Between 2.0V and 0.4V, V <sub>DDCPU</sub> = 2.5V	0.4		2.13	ns
t <sub>5</sub>	CPUCLK	CPU-CPU Clock Skew	Measured at 1.25V		100	250	ps
t <sub>6</sub>	CPUCLK, PCICLK	CPU-PCI Clock Skew	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks			1200	ps
t <sub>7</sub>	CPUCLK, SDRAM	CPU-SDRAM Clock Skew	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks			650	ps
t <sub>8</sub>	PCICLK, PCICLK	PCI-PCI Clock Skew	Measured at 1.5V			500	ps
t <sub>10</sub>	CPUCLK,	Cycle-Cycle Clock Jitter	Measured at 1.25V, V <sub>DDCPU</sub> = 2.5V			650	ps
t <sub>10</sub>	SDRAM	Cycle-Cycle Clock Jitter	Measured at 1.5V			650	ps
t <sub>10</sub>	PCICLK	Cycle-Cycle Clock Jitter	Measured at 1.5V			1200	ps
t <sub>11</sub>	CPUCLK, PCICLK, SDRAM	Power-up Time	CPU, PCI, AGP, and SDRAM clock stabilization from power-up			3	ms

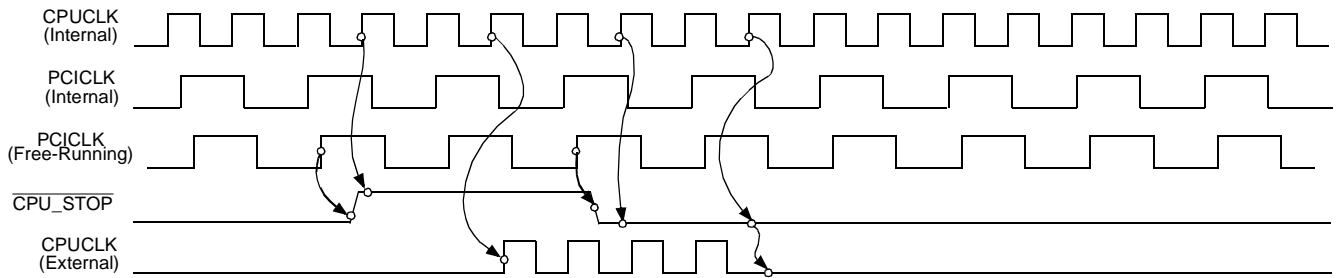
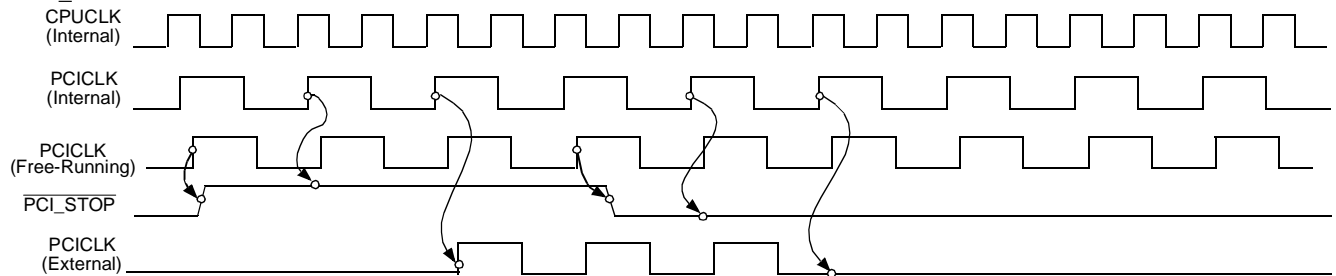
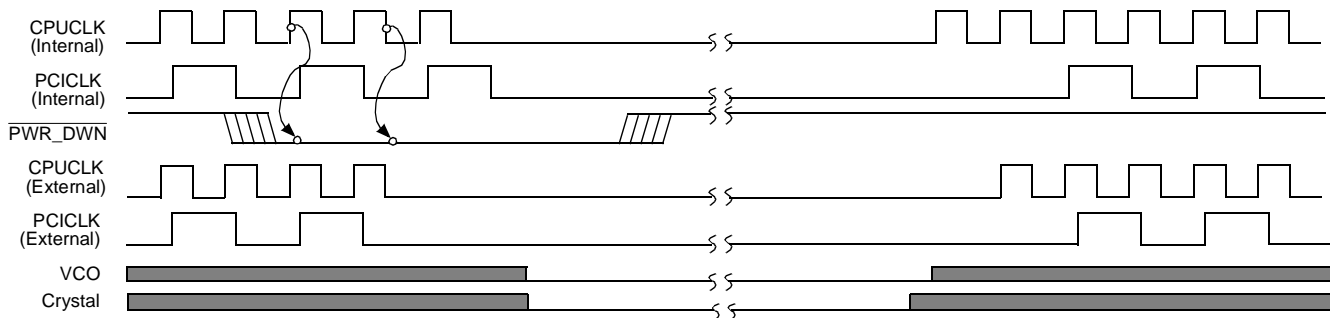
**Timing Requirement for the I<sup>2</sup>C Bus**

Parameter	Description	Min.	Max.	Unit
t <sub>12</sub>	SCLK Clock Frequency	0	100	kHz
t <sub>13</sub>	Time the bus must be free before a new transmission can start	4.7		μs
t <sub>14</sub>	Hold time start condition. After this period the first clock pulse is generated.	4		μs
t <sub>15</sub>	The Low period of the clock.	4.7		μs
t <sub>16</sub>	The High period of the clock.	4		μs
t <sub>17</sub>	Set-up time for start condition. (Only relevant for a repeated start condition.)	4.7		μs
t <sub>18</sub>	Hold time DATA for CBUS compatible masters. for I <sup>2</sup> C devices	5 0		μs
t <sub>19</sub>	DATA input set-up time	250		ns
t <sub>20</sub>	Rise time of both SDATA and SCLK inputs		1	μs
t <sub>21</sub>	Fall time of both SDATA and SCLK inputs		300	ns
t <sub>22</sub>	Se-up time for stop condition	4.0		μs

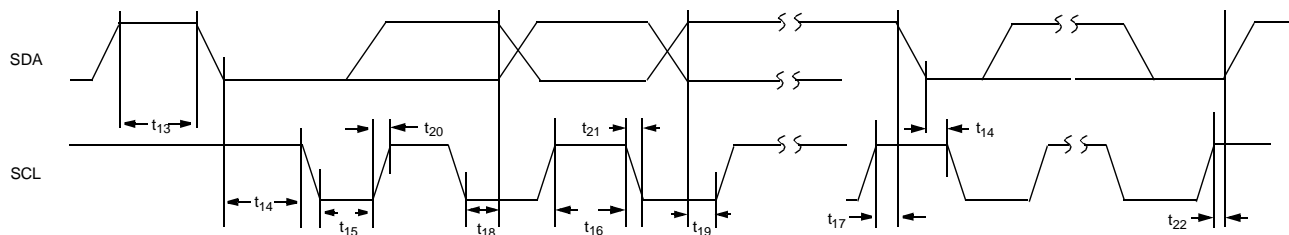
**Switching Waveforms**
**Duty Cycle Timing**


**Switching Waveforms** (continued)

**All Outputs Rise/Fall Time**

**CPU-CPU Clock Skew**

**CPU-SDRAM Clock Skew**

**CPU-PCI Clock Skew**

**PCI-PCI Clock Skew**

**AGP-PCI Clock Skew (-2 only)**


**Switching Waveforms (continued)**
**CPU\_STOP<sup>[11, 12]</sup>**

**PCI\_STOP<sup>[13, 14]</sup>**

**PWR\_DOWN**


Shaded section on the VCO and Crystal waveforms indicates that the VCO and crystal oscillator are active, and there is a valid clock.

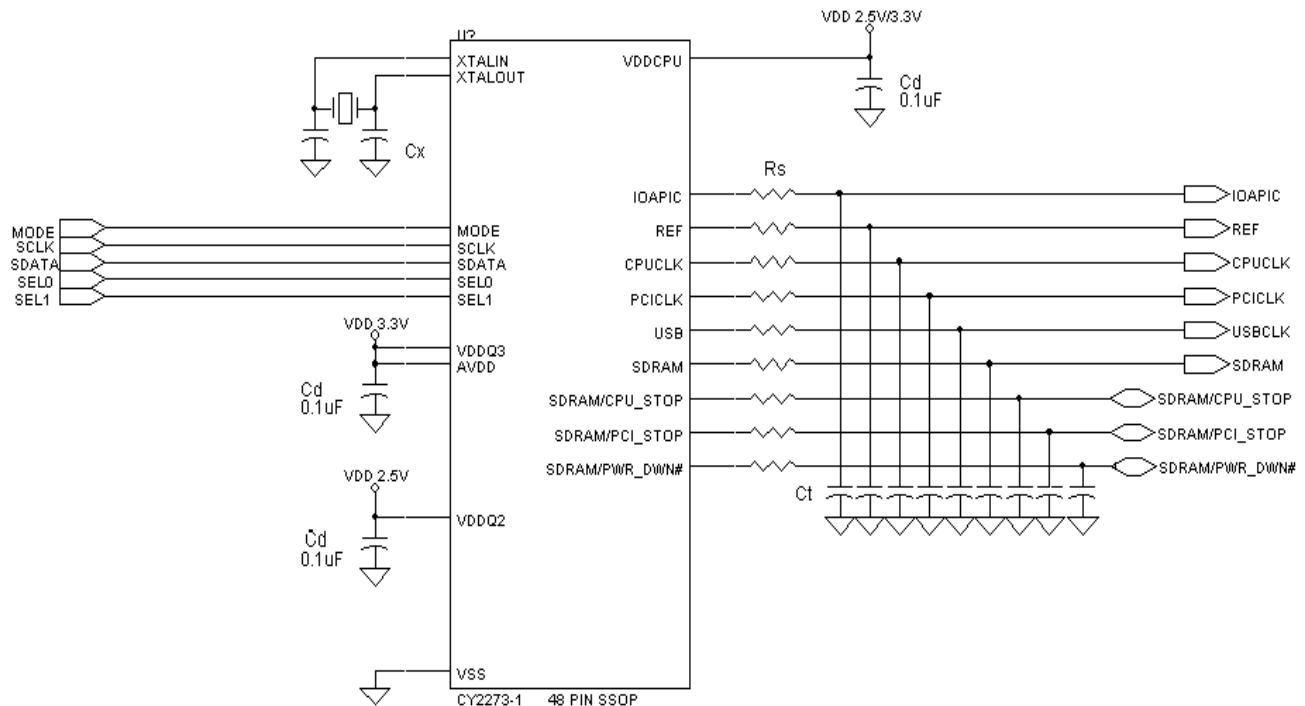
**Timing Requirements for the I<sup>2</sup>C Bus**

**Notes:**

11. CPUCLK on and CPUCLK off latency is 2 or 3 CPUCLK cycles.
12. CPU\_STOP may be applied asynchronously. It is synchronized internally.
13. PCICLK on and PCICLK off latency is 1 rising edge of the external PCICLK.
14. PCI\_STOP may be applied asynchronously. It is synchronized internally.

## Application Information

Clock traces must be terminated with either series or parallel termination, as they are normally done.

## Application Circuit



Cd = DECOUPLING CAPACITORS

Ct = OPTIONAL EMI-REDUCING CAPACITORS

Cx = OPTIONAL LOAD MATCHING CAPACITOR

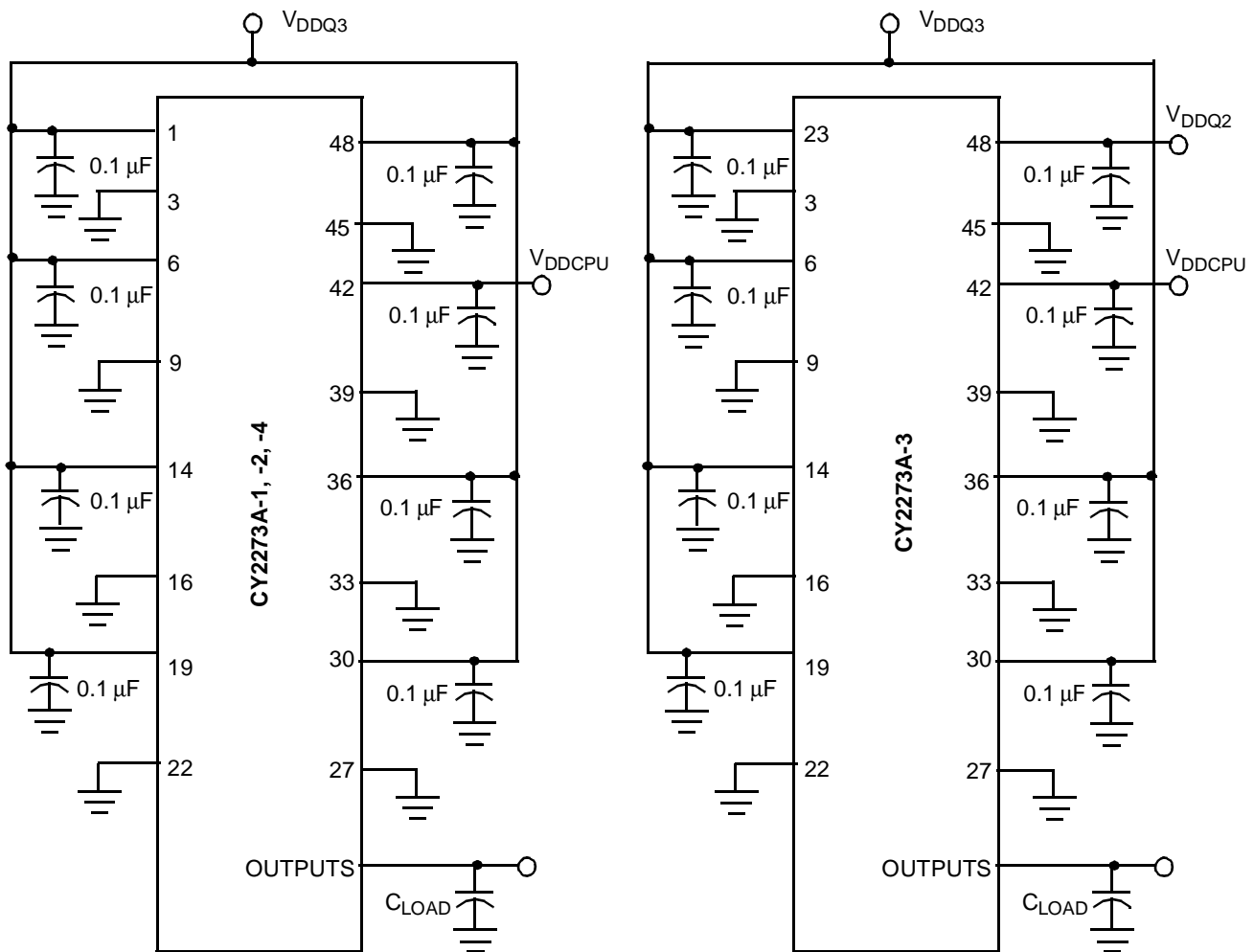
Rs = SERIES TERMINATING RESISTORS

## Summary

- A parallel-resonant crystal should be used as the reference to the clock generator. The operating frequency and  $C_{LOAD}$  of this crystal should be as specified in the data sheet. Optional trimming capacitors may be needed if a crystal with a different  $C_{LOAD}$  is used. Footprints must be laid out for flexibility.
- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1  $\mu$ F. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where  $R_{trace}$  is the loaded characteristic impedance of the trace,  $R_{out}$  is the output impedance of the clock generator (specified in the data sheet), and  $R_{series}$  is the series terminating resistor.

$$R_{series} \geq R_{trace} - R_{out}$$

- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF.
- A Ferrite Bead **may** be used to isolate the Board  $V_{DD}$  from the clock generator  $V_{DD}$  island. Ensure that the Ferrite Bead offers greater than 50 $\Omega$  impedance at the clock frequency, under loaded DC conditions. Please refer to the application note "Layout and Termination Techniques for Cypress Clock Generators" for more details.
- If a Ferrite Bead is used, a 10  $\mu$ F– 22  $\mu$ F tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

**Test Circuit**


Note: All Capacitors must be placed as close to the pins as is possible

**Ordering Information**

Ordering Code	Package Name	Package Type	Operating Range
CY2273APVC-1	O48	48-Pin SSOP	Commercial
CY2273APVC-2	O48	48-Pin SSOP	Commercial
CY2273APVC-3	O48	48-Pin SSOP	Commercial
CY2273APVC-4	O48	48-Pin SSOP	Commercial

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Package Diagram

48-Lead Shrunken Small Outline Package O48

