Chrontel

CH7017 TV Encoder / LVDS Transmitter

Features

TV-Out:

• VGA to TV conversion supporting up to 1024x768 pixels.
• Macrovision™ 7.1.L1 copy protection support.
• Two variable-voltage digital input ports.
• Simultaneous LVDS and TV output.
• True scale rendering engine supporting under-scan in all TV output resolutions. †¥
• Enhanced text sharpness and adaptive flicker removal with up to 7 lines of filtering. ¥
• Support for NTSC and PAL TV formats.
• Outputs CVBS, S-Video, RGB and YPrPb.
• Support for SCART output.
• TV / Monitor connection detect.
• Output video switch for easy wiring to connectors.

LVDS-Out:

• Single / Dual LVDS transmitter.
• Dual LVDS supporting pixel rates up to 330Mpixels/sec when both 12-bit input ports are ganged together.
• Panel fitting scaler – up scale to 1600x1200 pixels.
• LVDS low jitter PLL accepting EMI reduction input.
• LVDS 18-bit and 24-bit outputs.
• 2D dither engine.
• Panel protection and Power-Down sequencing.
• Programmable power management.

• Support for second CRT DAC bypass mode.
• Four 10-bit video DAC outputs.
• Fully programmable through serial port.
• Complete Windows and DOS driver support.
• Variable voltage interface to graphics device.
• 128-pin LQFP package.

1.0 General Description

The CH7017 is a Display Controller device that accepts two digital graphics input data streams. One data stream outputs through an LVDS transmitter to a LCD panel, while the other data stream is encoded for NTSC or PAL TV and outputs through four 10-bit high-speed DACs. The TV encoder device encodes a graphics signal up to 1024x768 resolution and outputs the video signals according to NTSC or PAL standards. The LVDS transmitter operates at pixel speeds up to 165MHz per link, supporting 1600x1200 panels at 60Hz refresh rate.

The device can also accept one graphics data stream over two 12-bit wide variable voltage ports which support nine different data formats including RGB and YCrCb (RGB must be used for LVDS output). A maximum of 330M pixels per second can be output through dual LVDS links.

The TV-Out processor will perform non-interlaced to interlaced conversion with scaling, flicker filtering, and encoding into any of the NTSC or PAL video standards. The scaler and flicker filter are adaptive and programmable for superior text display. Eight graphics resolutions are supported up to 1024 by 768 pixels with full vertical and horizontal under-scan capability in all modes. A high accuracy low jitter phase locked loop is integrated to create outstanding video quality. Anti-copy protection support is provided by Macrovision™ technology. In addition to TV encoder modes, bypass modes are included which allow the TV DACs to be used as a second CRT DAC.

The LVDS transmitter includes a panel fitting up-scaler and a programmable dither function for the support of 18-bit panels. Data is encoded into commonly used formats, including those detailed in the OpenLDI and the SPWG specifications. Serialized data outputs on three to eight differential channels.

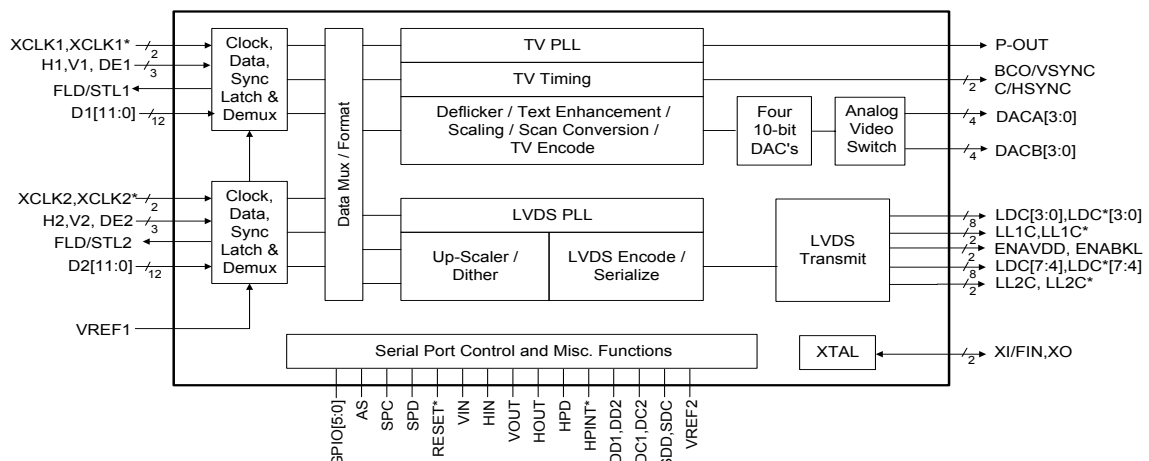† Patent number 5,781,241
¥ Patent number 5,914,753

Figure 1: CH7017 Functional Block Diagram

2.0 Pin Assignment

2.1 Package Diagram

Pin layout (Top View):

Left side (pins 1–38):
- 1 LPLL_VDD
- 2 LPLLCAP
- 3 LPLL_GND
- 4 LGND
- 5 LL2C
- 6 LL2C*
- 7 LVDD
- 8 LDC7
- 9 LDC7*
- 10 LGND
- 11 LDC6
- 12 LDC6*
- 13 LVDD
- 14 LDC5
- 15 LDC5*
- 16 LGND
- 17 LDC4
- 18 LDC4*
- 19 LVDD
- 20 LVDD
- 21 LDC3
- 22 LDC3*
- 23 LGND
- 24 LL1C
- 25 LL1C*
- 26 LVDD
- 27 LDC2
- 28 LDC2*
- 29 LGND
- 30 LDC1
- 31 LDC1*
- 32 LVDD
- 33 LDC0
- 34 LDC0*
- 35 LGND
- 36 VSWING
- 37 DAC_VDD
- 38 ISET

Top side (pins 128–103):
- 128 ENABKL
- 127 ENAVDD
- 126 GPIO[3]
- 125 GPIO[2]
- 124 GPIO[1]
- 123 GPIO[0]
- 122 HPINT*
- 121 HPD
- 120 VOUT
- 119 HOUT
- 118 V5V
- 117 DC2
- 116 DD2
- 115 DC1
- 114 DD1
- 113 SDC
- 112 SDD
- 111 VREF2
- 110 VIN
- 109 HIN
- 108 SPC
- 107 SPD
- 106 AS
- 105 FLD/STL2
- 104 DE2
- 103 DVDD

Right side (pins 102–65):
- 102 V2
- 101 H2
- 100 DGND
- 99 D2[11]
- 98 D2[10]
- 97 D2[9]
- 96 D2[8]
- 95 D2[7]
- 94 D2[6]
- 93 XCLK2
- 92 DGND
- 91 XCLK2*
- 90 D2[5]
- 89 D2[4]
- 88 D2[3]
- 87 D2[2]
- 86 D2[1]
- 85 D2[0]
- 84 DVDD
- 83 DVDD
- 82 D1[11]
- 81 D1[10]
- 80 D1[9]
- 79 D1[8]
- 78 D1[7]
- 77 D1[6]
- 76 XCLK1
- 75 DGND
- 74 XCLK1*
- 73 D1[5]
- 72 D1[4]
- 71 D1[3]
- 70 D1[2]
- 69 D1[1]
- 68 D1[0]
- 67 DGND
- 66 H1
- 65 V1

Bottom side (pins 39–64):
- 39 DAC_GND
- 40 N/C
- 41 CVBS (DACA3)
- 42 Y/G (DACB1)
- 43 Y/G (DACA1)
- 44 Pr/R (DACB2)
- 45 C/R (DACA2)
- 46 Pb/B (DACB0)
- 47 CVBS/B (DACA0)
- 48 DAC_GND
- 49 C/HSYNC
- 50 BCO/VSYNC
- 51 TVPLL_GND
- 52 XI / FIN
- 53 XO
- 54 TVPLL_VCC
- 55 TVPLL_VDD
- 56 GPIO[4]
- 57 GPIO[5]
- 58 RESET*
- 59 P-OUT
- 60 VDDV
- 61 VREF1
- 62 FLD/STL1
- 63 DE1
- 64 DVDD

Center: Chrontel CH7017

Figure 2: CH7017 128 Pin LQFP Package (Top View)

2.2 Pin Description

Table 1: Pin Description

Pin #	# of Pins	Type	Symbol	Description
66, 101	2	In/Out	H1, H2	**Horizontal Sync Input / Output** When the SYO control bit is low, these pins accept a horizontal sync inputs for use with the input data. The amplitude will range from 0 to VDDV. VREF1 is the threshold level for these inputs. These pins must be used as inputs in RGB Bypass mode. When the SYO control bit is high, the TV encoder will output a 64-pixels wide horizontal sync pulse from one of these pins. The output is driven from the DVDD supply, and it is valid ONLY when TV-Out is in operation.
65, 102	2	In/Out	V1, V2	**Vertical Sync Input / Output** When the SYO control bit is low, these pins accept a vertical sync inputs for use with the input data. The amplitude will range from 0 to VDDV. VREF1 is the threshold level for these inputs. These pins must be used as inputs in RGB Bypass mode. When the SYO control bit is high, the TV encoder will output a 1-line wide vertical sync pulse from one of these pins. The output is driven from the DVDD supply, and it is valid ONLY when TV-Out is in operation.
63, 104	2	In	DE1, DE2	**Data Enable** These pins accept a data enable signal that is high when active video data is input to the device, and remains low during all other times. The amplitude will range from 0 to VDDV. VREF1 is the threshold level for these inputs. The TV-Out function uses H and V sync signals and values in the SAV Register as reference to active video.
62, 105	2	Out	FLD/STL1, FLD/STL2	**TV Field / Flat Panel Stall Signal** These outputs can be programmed to be either a TV Field output from the TV encoder, or a Stall output from the flat panel Up-scaler. These outputs are tri-stated upon power up.
107	1	In/Out	SPD	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port. It can operate with input levels from VDDV to DVDD. Outputs are driven from 0 to VREF2.
108	1	In	SPC	**Serial Port Clock Input** This pin functions as the clock input of the serial port. It can operate with input levels from VDDV to DVDD.
106	1	In	AS	**Address Select** (Internal Pull-up) This pin determines the device address of the serial port.
112	1	In/Out	SDD	**Low-Voltage DDC Serial Data** Low-voltage serial data for DDC. It uses VREF2 / 2 as the threshold voltage. VREF2 divide by 2 function is generated on-chip.
113	1	In/Out	SDC	**Low-Voltage DDC Serial Clock** Low-voltage serial clock for DDC. It uses VREF2 / 2 as the threshold voltage. VREF2 divide by 2 function is generated on-chip.
114, 116	2	In/Out	DD1, DD2	**DDC Serial Data** Serial data for DDC. (0V to 5V)
111	1	In	VREF2	**Reference Voltage 2** Used to generate the output supply level for the SPD port. This pin should be tied externally to the maximum voltage seen by the ports. (1.5V to 3.3V).
115, 117	2	In/Out	DC1, DC2	**DDC Serial Clock** Clock for DDC. (0V to 5V)
123-126, 56, 57	6	In/Out	GPIO[5:0]	**General Purpose Input / Output [5:0]** These pins provide general purpose I/O and are controlled via the serial port. (3.3V). See description of GPIO Controls for I/O configuration.
127	1	Out	ENAVDD	**Panel Power Enable** Enable panel VDD. (3.3V)
128	1	Out	ENABLK	**Back Light Enable** Enable Back-Light of LCD Panel. (3.3V)

Table 1: Pin Description (Continued)

Pin #	# of Pins	Type	Symbol	Description
121	1	In	HPD	**Hot Plug Detect** (Internal Pull-down) This input pin determines whether a display device is connected to the VGA connector. When terminated, the display device is required to apply a voltage greater than 2.4 volts. Changes on the status of this pin will be relayed to the graphics controller via the HPINT* pin pulling low.
122	1	Out	HPINT*	**Hot Plug Interrupt Output** This pin provides an open drain output, which pulls low when a termination change has been detected on the HPD input.
36	1	In	VSWING	**LVDS Voltage Swing Control** This pin sets the swing level of the LVDS outputs. A 2.4K Ohm resistor should be connected between this pin and LGND (pin 35) using short and wide traces.
58	1	In	RESET*	**Reset * Input** (Internal Pull-up) When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port.
2	1	Analog	LPLLCAP	**LVDS PLL Capacitor** This pin allows coupling of any signal to the on-chip loop filter capacitor.
5, 24	2	Out	LL2C, LL1C	**Positive LVDS differential Clock2 & Clock1**
6, 25	2	Out	LL2C*, LL1C*	**Negative LVDS differential Clock2 & Clock1**
8, 11, 14, 17	4	Out	LDC[7:4]	**Positive LVDS differential data[7:4]**
9, 12, 15, 18	4	Out	LDC[7:4]*	**Negative LVDS differential data[7:4]**
21, 27, 30, 33	4	Out	LDC[3:0]	**Positive LVDS differential data[3:0]**
22, 28, 31, 34	4	Out	LDC[3:0]*	**Negative LVDS differential data [3:0]**
38	1	Analog	ISET	**Current Set Resistor Input** This pin sets the DAC current. A 140-ohm resistor should be connected between this pin and DAC_GND (pin 39) using short and wide traces.
41	1	Out	CVBS (DACA3)	**Composite Video** This pin outputs a composite video signal capable of driving a 75 ohm doubly terminated load. During bypass modes this output is valid only if the data format is compatible with one of the TV-Out display modes.
42	1	Out	Y/G (DACB1)	**Luma / Green Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to be the luminance component of YPrPb or green (for VGA bypass)
43	1	Out	Y/G (DACA1)	**Luma / Green Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to be s-video luminance or green (for SCART type 1 connections) or the luminance component of YPrPb or green (for VGA bypass)
44	1	Out	Pr/R (DACB2)	**Pr / Red Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to be the Pr component of YPrPb or red (for VGA bypass)
45	1	Out	C/R/Pr (DACA2)	**Chroma / Red Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to be s-video chrominance or red (for SCART type 1 connections) or the Pr component of YPrPb or red (for VGA bypass)
46	1	Out	Pb/B (DACB0)	**Pb / Blue Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to the Pb component of YPrPb or blue (for VGA bypass).
47	1	Out	CVBS/B/Pb (DACA0)	**Composite Video / Blue Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to be composite video or blue (for SCART type 1 connections) or the Pb component of YPrPb or blue (for VGA bypass).
120	1	Out	VOUT	**V-Sync Output** This pin is the output of a voltage translating digital buffer and is driven from V5V.

Table 1: Pin Description (Continued)

Pin #	# of Pins	Type	Symbol	Description
110	1	In	VIN	**V-Sync Input** This pin is the input of a voltage translating digital buffer. Input threshold can be programmed by serial port to equal to VREF2/2 or to DVDD/2.
119	1	Out	HOUT	**H-Sync Output** This pin is the output of a voltage translating digital buffer and is driven from V5V.
109	1	In	HIN	**H-Sync Input** This pin is the input of a voltage translating digital buffer. Input threshold can be programmed by serial port to equal to VREF2/2 or to DVDD/2
49	1	Out	C/HSYNC	**Composite / Horizontal Sync** This pin provides composite sync in TV modes and horizontal sync in bypass RGB mode. This pin is driven by the DVDD supply.
50	1	Out	BCO/VSYNC	**Buffered Clock Outputs / Vertical Sync** This output pin provides buffered crystal oscillator clock output or VSYNC output in bypass RGB mode. This pin is driven by the DVDD supply.
52	1	In	XI / FIN	**Crystal Input / External Reference Input** A parallel resonant 14.31818MHz crystal ($\pm$ 20 ppm) should be attached between this pin and XO. However, an external CMOS compatible clock can drive the XI/FIN input.
53	1	Out	XO	**Crystal Output** A parallel resonance 14.31818MHz crystal ($\pm$ 20 ppm) should be attached between this pin and XI / FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open.
59	1	Out	P-Out	**Pixel Clock Output** This pin provides a pixel clock signal to the VGA controller, which can be used as a reference frequency. The output is selectable between 1X and 2X of the pixel clock frequency. The output driver is driven from the VDDV supply (pin 60). This output has a programmable tri-state. The capacitive loading on this pin should be kept to a minimum.
61	1	In	VREF1	**Reference Voltage Input 1** The VREF1 pin inputs a reference voltage of VDDV / 2. The signal is derived externally through a resistor divider and decoupling capacitor, and will be used as a reference level for data, sync and clock inputs.
68-73, 77-82	12	In	D1[11:0]	**Data1[11] through Data1[0] Inputs** These pins accept the 12 data inputs from a digital video port of a graphics controller. The levels are 0 to VDDV. VREF1 is the threshold level.
76, 74	2	In	XCLK1, XCLK1*	**External Clock Inputs** These inputs form a differential clock signal input to the device for use with the H1, V1 and D1[11:0] data. If differential clocks are not available, the XCLK1* input should be connected to VREF1. The clock polarity can be selected by the MCP1 control bit.
85-90, 94-99	12	In	D2[11:0]	**Data2[11] through Data2[0] Inputs** These pins accept the 12 data inputs from a digital video port of a graphics controller. The levels are 0 to VDDV. VREF1 is the threshold level.
93, 91	2	In	XCLK2, XCLK2*	**External Clock Inputs** These inputs form a differential clock signal input to the device for use with the H2, V2 and D2[11:0] data. If differential clocks are not available, the XCLK2* input should be connected to VREF1. The clock polarity can be selected by the MCP2 control bit.
118	1	Power	V5V	**5V supply for H/VOUT** (5V)
64, 83, 84, 103	4	Power	DVDD	**Digital Supply Voltage** (3.3V)
67, 75, 92, 100	4	Power	DGND	**Digital Ground**
60	1	Power	VDDV	**I/O Supply Voltage** (1.1V to 3.3V)
55	2	Power	TVPLL_VDD	**TV PLL Supply Voltage** (3.3V)
54	1	Power	TVPLL_VCC	**TV PLL Supply Voltage** (3.3V)
51	1	Power	TVPLL_GND	**TV PLL Ground**
37	1	Power	DAC_VDD	**DAC Supply Voltage** (3.3V)

Table 1: Pin Description (Continued)

Pin #	# of Pins	Type	Symbol	Description
39, 48	1	Power	DAC_GND	**DAC Ground**
7, 13, 19, 20, 26, 32	6	Power	LVDD	**LVDS Supply Voltage** (3.3V)
4, 10, 16, 23, 29, 35	6	Power	LGND	**LVDS Ground**
1	1	Power	LPLL_VDD	**LVDS PLL Supply Voltage** (3.3V)
3	1	Power	LPLL_GND	**LVDS PLL Ground**

3.0 Package Dimensions
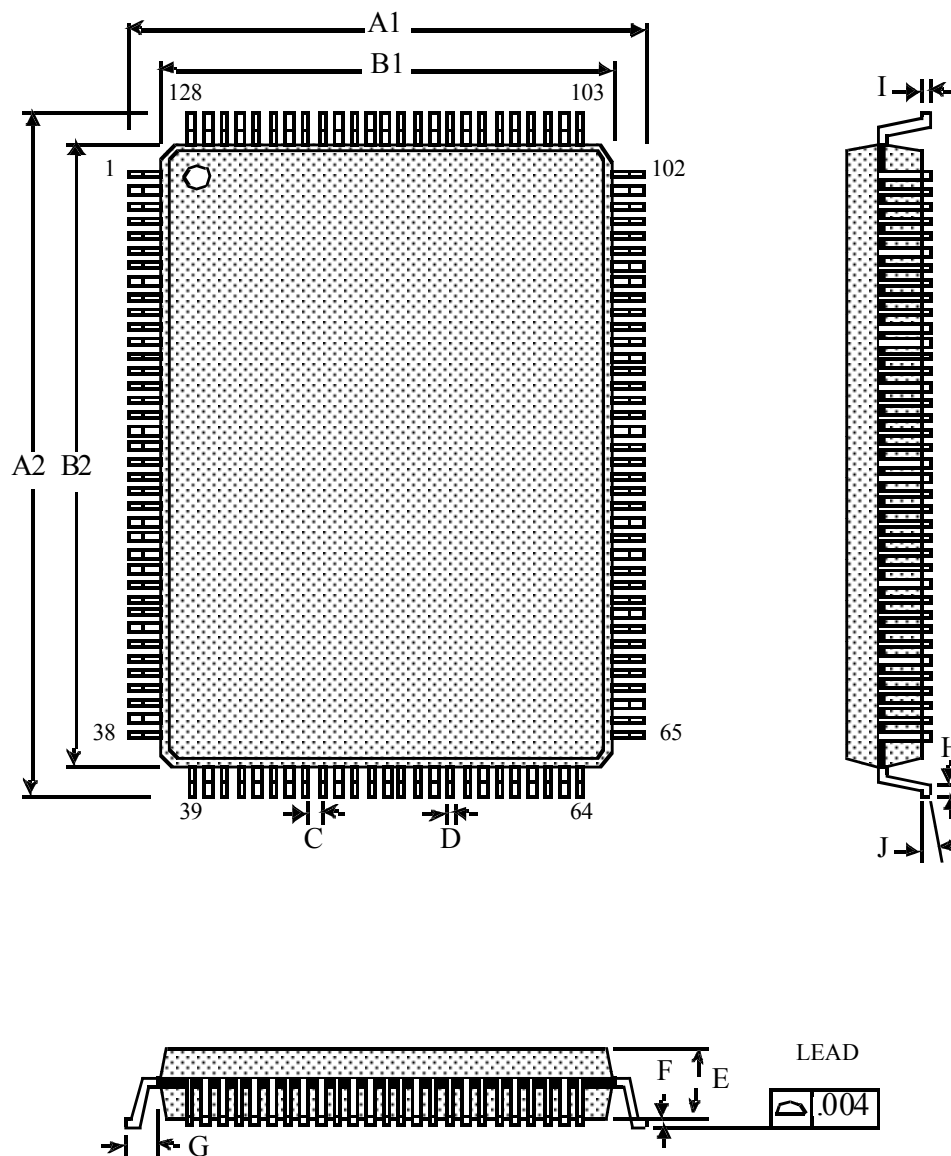
Table of Dimensions

No. of Leads		SYMBOL											
		A1	A2	B1	B2	C	D	E	F	G	H	I	J
128 (14X20)													
Milli-meters	MIN	16	22	14	20	0.50	0.17	1.35	0.05	1.00	0.45	0.09	0°
	MAX						0.27	1.45	0.15		0.75	0.20	7°

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ORDERING INFORMATION			
Part Number	Package Type	Number of Pins	Voltage Supply
CH7017A-T	LQFP	128	3.3V

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