TriTech Microelectronics

TR88801/802

Pen-input Processor

Features

- Fully integrated pen input processor
- No programming required
- 10-bit A/D for high resolution
- Low current consumption
- Pen detection circuitry
- 8-bit Parallel Interface option (TR88802)
- Serial Interface option (TR88801)
- On-chip oscillator circuit
- Data Averaging Mode (TR88802)
- 5V operation

Applications

- Personal digital assistants
- Touch screens
- Touch Pads for mouse replacement in computers
- Electronic organizers/terminals
- Feature phones
- Digitizer tablets

General Description

The TR88801/802 contain all the circuitry required to easily interface low-cost resistive digitizer tablets and add pen-input capability. The TR88801/802 use a 10-bit ADC to resolve 1024 levels. This translates to a resolution of 204 dpi when used with a typical PDA sized digitizer pad of 5 inches length. The TR88802 is designed to simplify pen interfacing by integrating all pen-input tasks required to present X,Y-position data to the main application at 200 coordinate pairs per second, when used with a 1.8432 MHz clock.

The application interface is via either an interrupt-driven parallel bus or a serial connection. The TR88801/802 are fully self-contained and require no user programming. Pen detection status is signalled to the application for use in handwriting recognition and verification. Its low power consumption makes the device suitable for use with hand-held or battery-operated devices.

An on-chip oscillator circuit allows the chip to function with an external quartz crystal or, alternatively, a CMOS-level input clock.

BLOCK DIAGRAM

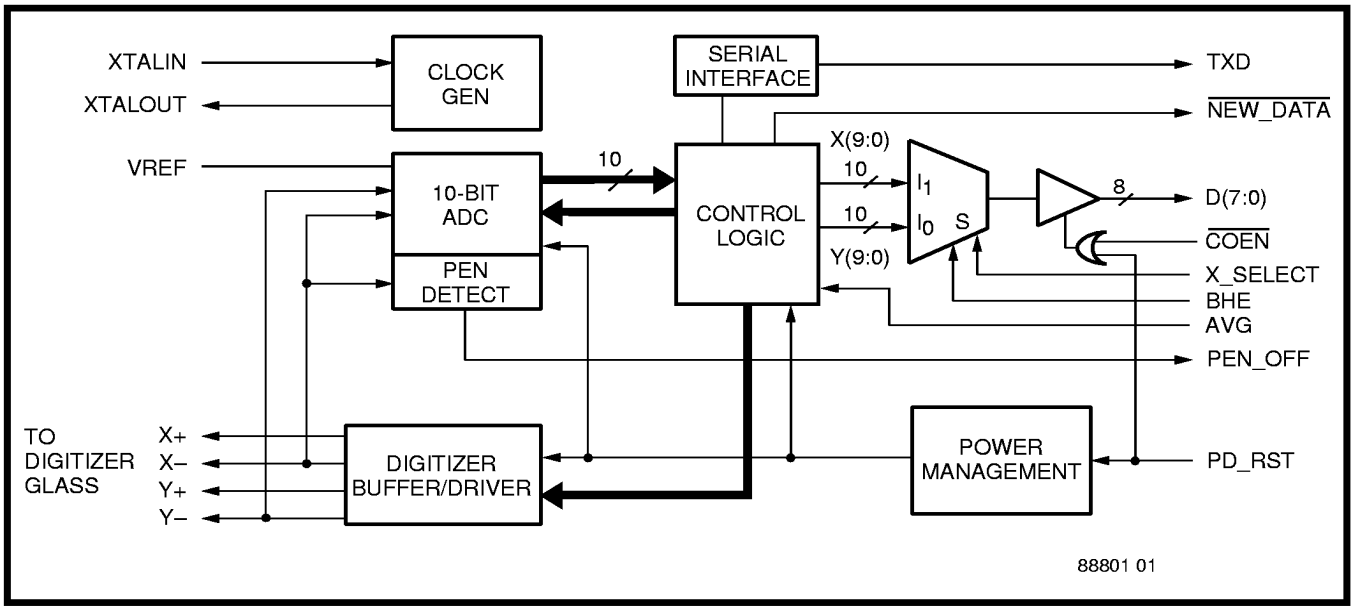


Figure 1 • *TR88802 Block Diagram*

BLOCK DIAGRAM

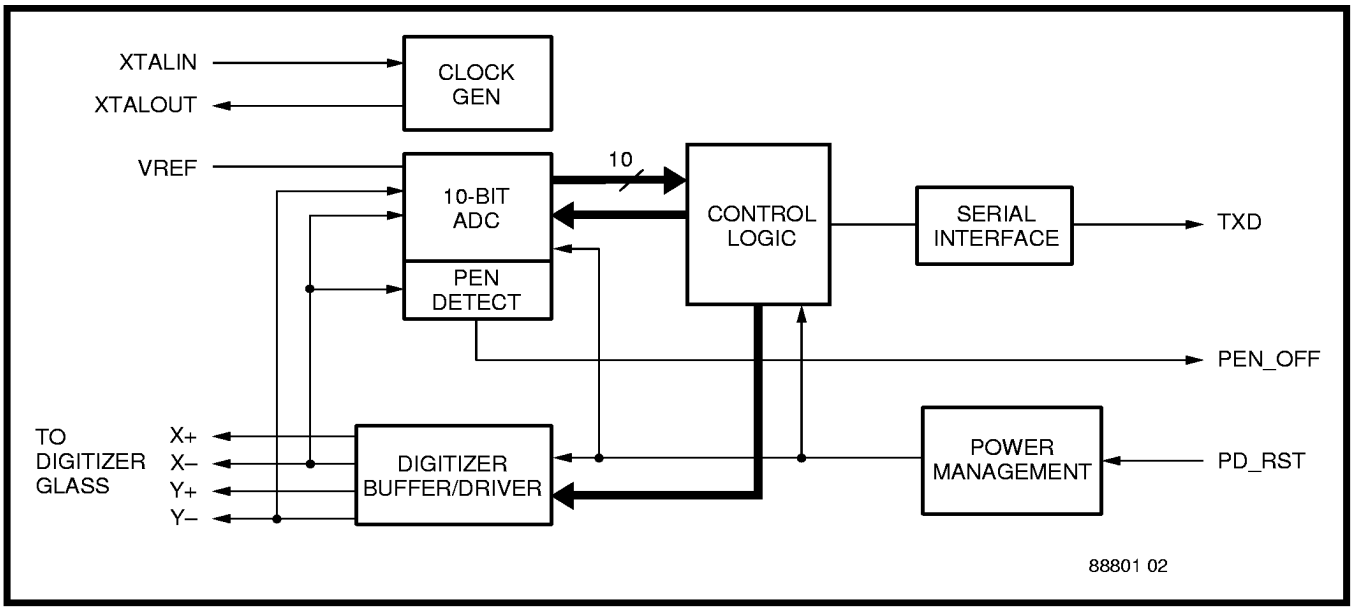
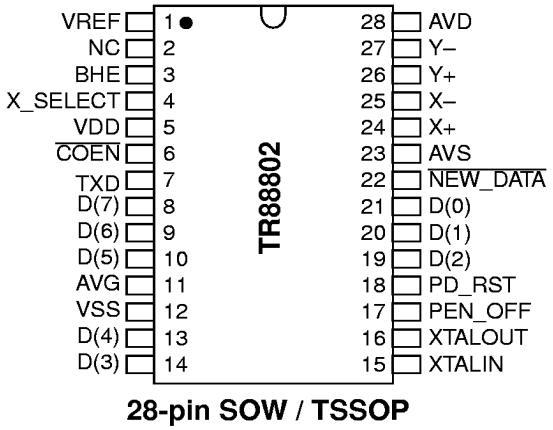
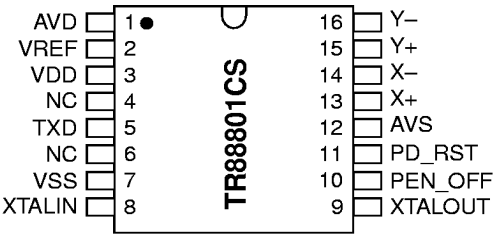


***Figure 2** • TR88801 Block Diagram*

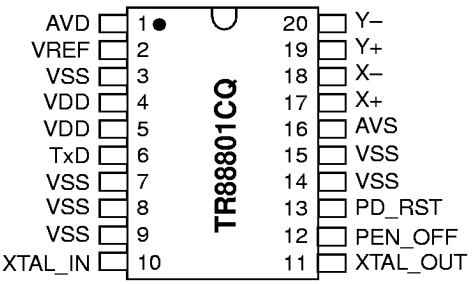
Pin Configuration



28-pin SOW / TSSOP



16-pin SOW



20-pin TSSOP

Package Top Views

Pin Definitions – TR88801CS/CQ

(SOW-16) Pin	(TSSOP-20) Pin	Pin Name	I/O	Description
1	1	AVD	Power	Analog Positive Supply. May be connected to digital positive supply (VDD) via a ferrite bead.
2	2	VREF	Analog Input	Internal 2.5V reference. Connect a 1 μF capacitor between this pin and analog ground pin (AVS).
n/a	3	VSS	Ground	Digital Ground
3	4, 5	VDD	Power	Digital Power Supply
4	n/a	NC	–	No Connect
5	6	TXD	TTL Output	Serial Data Out. With a 1.8432MHz input clock, data is 19.2 kbps NRA format (1 start bit; 1 stop bit).
6	n/a	NC	–	No Connect
7	7, 8, 9	VSS	Ground	Digital Ground
8	10	XTAL_IN	CMOS Input	Crystal Oscillator input pin. Normally connected to 1.8432MHz CMOS input clock.
9	11	XTAL_OUT	CMOS Output	Used when connected to crystal as shown in Figure 7. Should be left floating if clock input is applied at XTAL_IN.
10	12	PEN_OFF	TTL Output	Indicates pen not detected. Logic 1 if pen is not detected.
11	13	PD_RST	TTL Schmitt Input	Active-High Power down/Reset input. Assert Logic 1 for >= 10 ns to reset. Hold at Logic 1 if pen is not detected.
n/a	14, 15	VSS	Ground	Digital Ground
12	16	AVS	Ground	Analog Ground
13	17	X+	Analog I/O	Resistive tablet X- plane driver. Connect to X- terminal of resistive tablet.
14	18	X–	Analog I/O	
15	19	Y+	Analog I/O	Resistive tablet Y- plane driver. Connect to Y- terminal of resistive tablet.
16	20	Y–	Analog I/O	

Pin Definitions – TR88802CS/CQ

(SOW/ TSSOP-28) Pin	Pin Name	I/O	Description
1	VREF	Analog Input	Internal 2.5V reference. Connect a 1μF ceramic capacitor between this pin and analog ground pin (AVS).
2	NC		No Connection
3	BHE	TTL Schmitt input	Bus High Enable. (TR88802 only) Logic 1 to select D(9:2) Logic 0 to select D(1:0) as MSBs. The lower 6 bits will all be zeros
4	X_SELECT	TTL Schmitt input	X-Y data select. (TR88802 only) Logic 1 to select X-data output. Logic 0 to select Y-data output.
5	VDD	Power	Digital Positive Supply.
6	$\overline{\text{COEN}}$	TTL Input	Chip Output Enable (TR88802 only) Logic 1 to Hi-Z D(7:0) Logic 0 to enable X/Y date to be read on D(7:0)
7	TXD	TTL Output	Serial data out. With a 1.8432 MHz input clock, data is 19.2 kbps NRZ format (1 start bit; 8 data bits; 1 stop bit).
8-10	D(7:5)	Tristate TTL Output	X or Y coordinate output (TR88802 only)
11	AVG	TTL Input	Data Average select pin (TR88802 only) Logic 1 selects Data average mode Logic 0 selects raw data mode.
12	VSS	Power	Digital Ground.
13, 14	D(4:3)	Tristate TTL Output	X or Y coordinate output (TR88802 only)
15	XTALIN	CMOS Input	Crystal oscillator input pin. Normally connected to 1.8432MHz CMOS input clock.
16	XTALOUT	CMOS Out-put	Used when connected to crystal as shown in Figure 7. Should be left floating if clock input is applied at XTALIN.
17	PEN_OFF	TTL Output	Indicates pen not detected. Logic 1 if pen is not detected.
18	PD_RST	TTL Schmitt Input	Active-Hi Power down/Reset input. Assert Logic 1 for ≥ 10ns to reset. Hold at Logic 1 for power-down mode.
19-21	D(2:0)	Tristate TTL Output	X or Y coordinate output (TR88802 only)
22	$\overline{\text{NEW\_DATA}}$	TTL Output	Indicates new data. (TR88802 only). A Logic 0 pulse indicates that new data packet is available at D(7:0).
23	AVS	Power	Analog Ground.
24	X+,	Analog I/O	Resistive tablet X- plane driver. Connect to X- terminal of resistive tablet.
25	X–	Analog I/O	
26	Y+	Analog I/O	Resistive tablet Y- plane driver. Connect to Y- terminal of resistive tablet.
27	Y–	Analog I/O	
28	AVD	Power	Analog Positive Supply. May be connected to digital positive supply (VDD) via a ferrite bead.

Background Information

Digitizer Technologies

Pen-input appliances usually employ some form of digitizer tablet as a designated writing surface for capturing the position of the pen. The digitizer tablet often comes coupled with a display technology layer (for example LCD) so that the pen position on the digitizer tablet may be echoed on the display as "ink".

Resistive Digitizers

A resistive digitizer is made up of a multi-layer sandwich of resistive films and protective coatings all sitting on top of a flat-panel LCD.

Figure 3 shows a simplified blown-up picture of a typical resistive digitizer and its connections in a pen-input appliance.

The resistive digitizer works by direct contact of the pen flexing a pair of resistive films, hence any blunt pointing instrument may be used as the "pen". A protective hard coating is often added at the top of the resistive tablet to ensure durability of the resistive films and to prevent subsequent digitizing errors arising from the non-uniform wear and tear of an unprotected resistive film surface.

The simplicity of a resistive digitizer design and the use of a passive pen makes it an energy–efficient, lightweight and cost-effective solution to meet the needs of most pen-input appliances.

Digitizer Resolution

The resolution of a digitizer is typically measured in dots per inch (dpi) and is a function of the physical size of the digitizer tablet and the resolution of the ADC used in the conversion circuitry.

For example a 10-bit ADC is capable of resolving 2^{10} (or 1024) levels. When used in a 5 inch by 8 inch digitizer system, this results in a digitizer resolution of 128 dpi. When used in a smaller 3 inch by 5 inch system, the resolution becomes 204 dpi.

The effective digitizer resolution will be affected by things like the choice of digitizer technology, the choice of pen architecture (particularly the shape of the tip) and also by system noise.

In the case of resistive digitizers, the direct-contact nature of its operation and the pen thickness often imposes an upper limit on the effective system resolution that may be achieved, regardless of the resolution of the ADC itself.

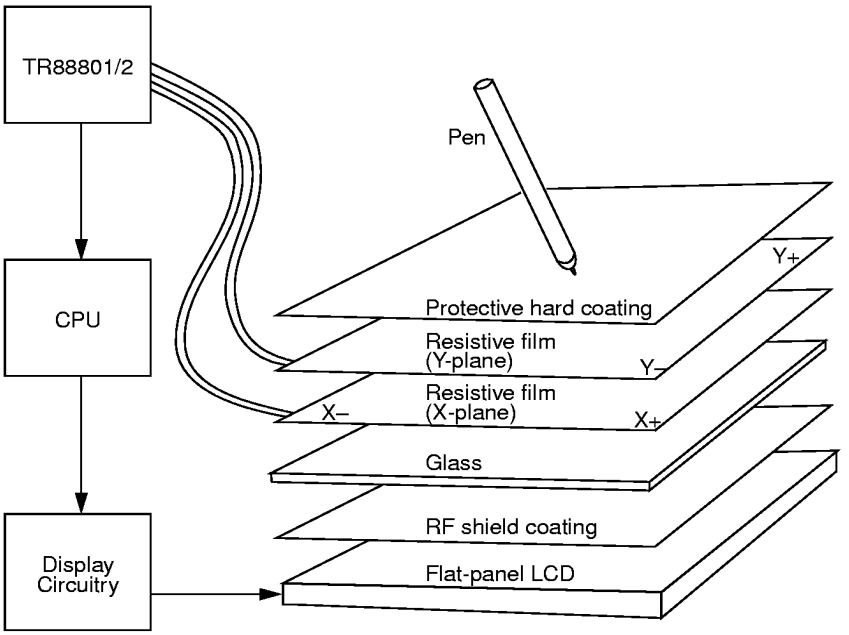


Figure 3 • *Typical Resistive Digitizer*

Coordinate Data Report Rate

The coordinate data report rate is quantified in coordinate pairs per second (cpps) and refers to how many (x,y) coordinate positions of the pen were obtained from the tablet, digitized, and reported to the CPU every second. A higher coordinate rate enables closer tracking of the pen movement over the digitizer tablet surface and prevents distortion of quick doodles or missed pen strokes in the entry of complex characters (e.g. Chinese or Japanese script).

Functional Description

The TR88801/802 when used in a pen-input appliance interfaces to a resistive digitizer and a microcontroller.

Resistive Digitizer Interface

The devices interface to a typical resistive digitizer consists of four bi-directional (input/output) pins. These four pins (X+, X–, Y+, Y–) are connected across the X-plane resistive film and Y-plane resistive film of the digitizer respectively. On-chip buffers provide the necessary current drive to the resistive digitizer via these same four pins.

When a pen is in contact with the digitizer tablet, the pressure forces the X-plane and Y-plane resistive films to come into contact at the exact position where the pen is located (see Figure 4).

To get the X-coordinate position, the TR88801/802 will apply current drive to the X-plane resistive film (via X+, X–) and sense the voltages picked up by the Y-plane resistive film (via Y–). The current drive to the X-plane sets up a voltage gradient (V+, V–) across the resistive film. At the point of pen contact, the voltage at that point along the X-plane voltage gradient may be some value Vx, where $V- \leq Vx \leq V+$. Through direct contact, the Y-plane resistive film picks up the voltage Vx at the point of contact with the X-plane resistive film. This voltage is sensed by the TR88801/802 and used to calculate the X-coordinate of the pen position.

Next, to get the Y-coordinate position, the TR88801/802 will apply the current drive at the Y-plane resistive film and sense the voltage picked up by the X-plane resistive film.

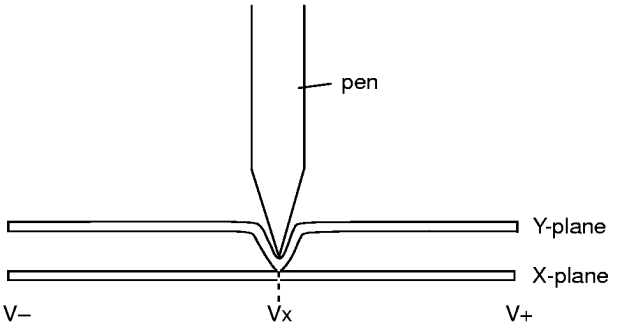


***Figure 4** • Locating the Pen Position*

Pen Detection

On-chip circuitry detects if the pen is in contact with the digitizer tablet. The pen-detection status is flagged on a pin (PEN_OFF) and may be used by the system for signalling end-of-stroke for handwriting recognition software purposes. If no pen is detected, PEN_OFF will be pulled to Logic 1 and no coordinate data will be made available. PEN_OFF at Logic 0 indicates that a pen is detected on the digitizer tablet and its coordinate position will be made available at the parallel and serial interfaces.

Power Management

The TR88801/802 is designed in advanced submicron CMOS process and consumes minimal power under normal operation. To further conserve power, the system programmer may wish to power down the TR88801/802 device whenever the pen-input interface is not in use. TR88801/802 will enter power down when the PD_RST pin is held at LOGIC 1. Normal operation (power up) will resume when PD_RST is returned to Logic 0.

Coordinate Calculation

The voltages picked up by the digitizer interface are first passed to a 10-bit Analog-to-Digital Converter (ADC) where they are digitized before further processing. The conversion speed of the ADC permits a data rate of 200 coordinate pairs per second when the crystal frequency (Fclk) is 1.8432 MHz. The Control Logic block calculates the (x,y) coordinate location of the pen and formats the data for output via the parallel (D(7:0)) and serial (TXD) interfaces. The X-coordinate and Y-coordinate information are each 10-bit wide.

Parallel Interface: TR88802

A parallel interface is available on the TR88802 in a 28-lead SOP package. The coordinate data is available at the data interface as D(7:0). Three control pins ($\overline{\text{COEN}}$, X_SELECT, BHE) multiplex the X-coordinate and Y-coordinate data onto D(7:0). A logic 0 on COEN will enable data onto the bus so that the TR88802 may be used in parallel with other devices. When a Logic 1 is asserted on X_SELECT, the X-coordinate data is made available on D(7:0). When a Logic 0 is asserted on X_SELECT, the Y-coordinate data is selected. As the device offers 10-bit resolution, the pin BHE enables the data as D(9:2) (logic 1) and D(1:0) (+ five LSBs = logic 0) onto D(7:0). A status pin ($\overline{\text{NEW\_DATA}}$) pulses low if a pen is detected, to indicate that a new coordinate data pair is available. Parallel data format is shown in Figure 5 and parallel interface timing is shown in Figure 7.

Data-Averaging Mode

When the AVG pin is set to Logic 0, the coordinate data at pins TXD and D(7:0) will indicate the most recent X-Y position sampled by the ADC.

When the AVG pin is set to Logic 1, the data-averaging mode is invoked for the parallel interface. In this mode, the coordinate data output at D(7:0) will indicate the rolling average of the four most recent X-Y positions sampled by the ADC. The serial data at pin TXD will still indicate the most recent X-Y position sampled by the ADC.

Serial Interface: TR88801

With the TR88801 device, serial data is available at the TXD pin. With an input clock of 1.8432 MHz, the serial baud rate is 19200 bits per second. A different clock than 1.8432 MHz may be used if an exact baud rate of 19200 bps is not required or if the serial interface is not used. The serial baud rate scales with the input clock frequency, a faster clock than 1.8432MHz will result in a baud rate of more than 19200 bps (and vice versa). Table 1 shows the serial interface data format.

		MSB							LSB
High byte	BHE=Logic 1	D9	D8	D7	D6	D5	D4	D3	D2
Low byte	BHE=Logic 0	D1	D0	0	0	0	0	0	0

Figure 5 • *Parallel data format*

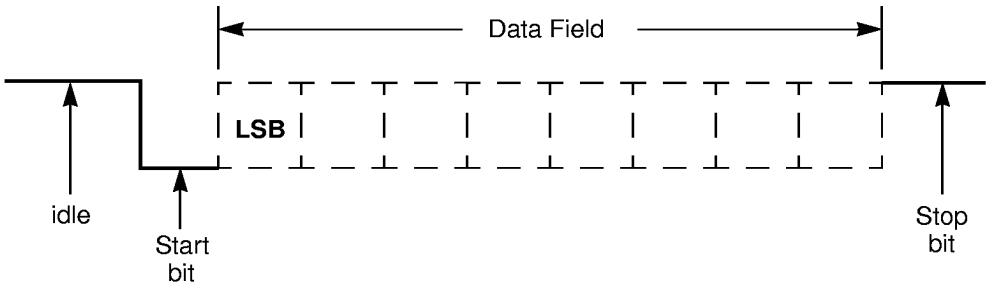


Figure 6 • *Serial data format*

Table 1 • Serial Interface Data Format

Parameter	Description
Data Output Voltage Levels	CMOS (VSS to VDD)
Serial output	1 start bit, 8 data bits, 1 stop bit, Non-return-to-zero (NRZ); No parity
Normal Frame [1] (5 bytes)	byte 1 = 0xFF byte 2 = Low byte of X byte 3 = High byte of X byte 4 = Low byte of Y byte 5 = High byte of Y
Pen off frame [2] (3 bytes)	byte 1 = 0xFF byte 2 = 0xFE byte 3 = 0xFE
Stream Format	Normal Frame Normal Frame . . . Normal Frame Pen-Off Frame
Transmission Rate	200 frames/sec at 19200 bps

***Notes**:*

1. *Normal frames sent when pen is detected on Digitizer. Refer to Fig 5. for bit pattern of these bytes.*
2. *TxD line goes idle after a Pen Off frame.*

Absolute Maximum Ratings

Beyond these limits damage may occur to the device.

Symbol	Parameter	Min	Max	Units
V	Supply Voltage	-0.25	6.5	V
Ts	Storage Temperature	-40	125	°C

Recommended Operating Conditions

Valid for 25°C ambient temperature and 5V supply unless otherwise stated.

Symbol	Parameter	Min	Typ	Max	Units
Vdd	Supply Voltage	4.5	5.0	5.5	V
Avd	Analog Supply Voltage	4.75	5.0	5.25	V
Fclk	Crystal Frequency		1.8432		MHz

General Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{il}	TTL input LO	Vdd = 5V			0.8	V
V_{ih}	TTL input HI	Vdd = 5V	2.0			V
I_{il}	Input leakage	V_i = Vdd or Vss	-10		10	µA
V+	Schmitt input high	Vdd = 5V		1.6		V
V-	Schmitt input low	Vdd = 5V	2.0			V
V_{hyst}	Schmitt hysterisis	Vdd = 5V		0.4		V
V_{ol}	Low Level Output	I_{ol} = 8mA, Vdd = 5V			0.4	V
V_{oh}	High Level Output	I_{oh} = -1mA, Vdd = 5V	2.4			V
I_{oz}	High Z leakage	V_o = Vdd or Vss	-10		10	µA

Electrical Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{VDD}	Digital Supply Current (using CMOS-level clock)	Power up PD_RST = Logic **0**		0.3		mA
I_{AVD}	Analog Supply Current	Power up PD_RST = Logic **0**		1.6		mA
I_{VDDPD}	Digital Supply Current	Power down PD_RST = Logic **1**		1		µA
I_{AVDPD}	Analog Supply Current	Power down PD_RST = Logic **1**		1		µA

Electrical Specifications (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$C_{interplate}$	Parasitic capacitance between X and Y-plates of Digitizer			5	10	nF
R_D	Resistance of Digitizer Film		250	600	1000	Ω
BR	Serial Baud Rate	Fclk = 1.8432MHz		19200		bps
CPPS	Coordinate Pairs Per Second	Fclk = 1.8432MHz		200		cpps
T_{UP}	Power Up Time from PD_RST being de-asserted to reliable operation	(using 1μF capacitor at VREF)			100	ms
Rdriver	Parasitic resistance of on chip driver	Note 1		35	50	Ω

Notes:

1. Effect of parasitic resistance is to reduce total count from 1024 by 6% to 8% on each of the four sides of digitizer.

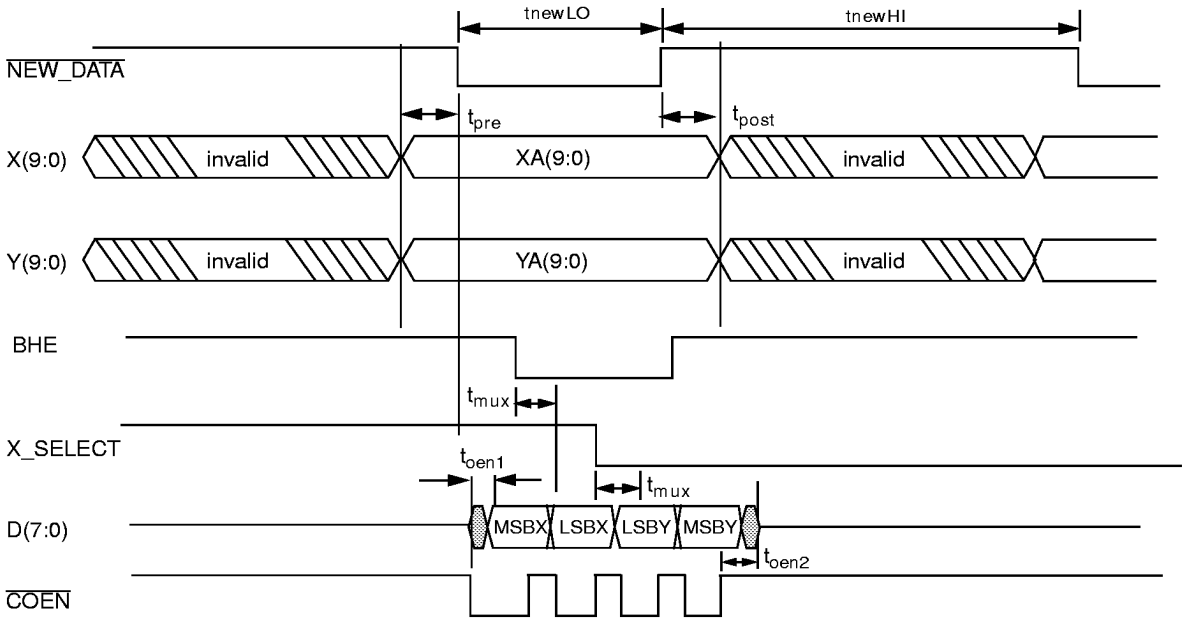


Figure 7 • *Parallel Interface Timing Diagram*

Parallel Interface Timing Fclk = 1.8432MHz

Symbol	Parameter	Min	Typ	Max	Units
tnewHI	NEW_DATA Logic 1 pulse width. Scales to Fclk		4.2		ms
tnewLO	NEW_DATA Logic 0 pulse width. Scales to Fclk		0.8		ms
tpre	Data setup before NEW_DATA falling edge	100			ns
tpost	Data setup before NEW_DATA rising edge	100			ns
tmux	Multiplexer selector path propagation delay		10	40	ns
toen1	COEN falling edge to data bus driven		10	40	ns
toen2	COEN rising edge to data bus Hi-Z		10	40	ns

Applications Information

Figure 8 shows a typical connection for TR88802 where an input clock of 1.8432 MHz is connected at XTALIN. On the board, the analog traces at X–, X+, Y–, Y+ should be kept short and routed away from other signal lines, especially clock-lines and high-activity lines. The traces from the TR88802 to the capacitors should also be kept short.

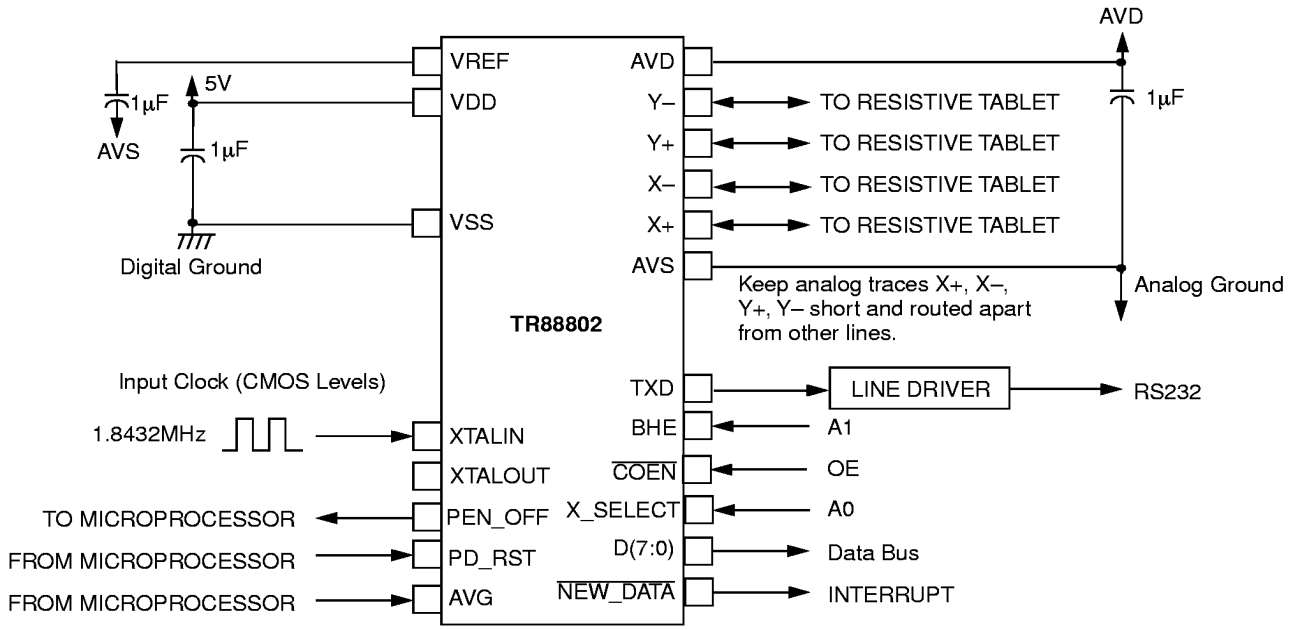


Figure 8 • *Typical Connection Diagram for TR88802*

Alternatively, a quartz crystal of 1.8432 MHz may be connected across XTALIN and XTALOUT as shown in Figure 9.

The TR88801/802 4-wire digitizer interface connects easily to most resistive digitizer tablets available from various manufacturers including MicroTouch, Dynapro, Panasonic and Samsung.

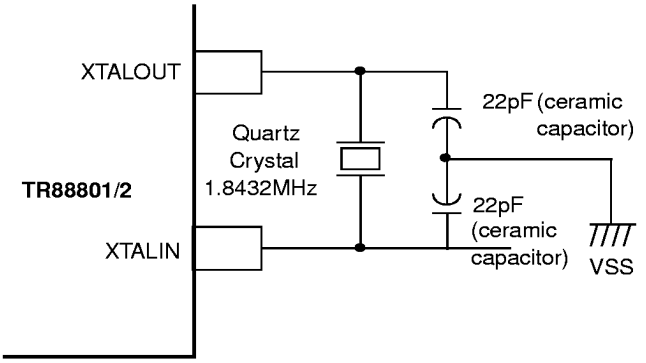


Figure 9 • *Connection using a Quartz Oscillator*

Serial Interface Connections

Figure 10 shows a typical connection for TR88801 where an input clock of 1.8432 MHz is connected at XTALIN. On the board, the analog traces at X–, X+, Y–, Y+ should be kept short and routed away from other signal lines, especially clock-lines and high-activity lines. The traces from the TR88801 to the capacitors should also be kept short.

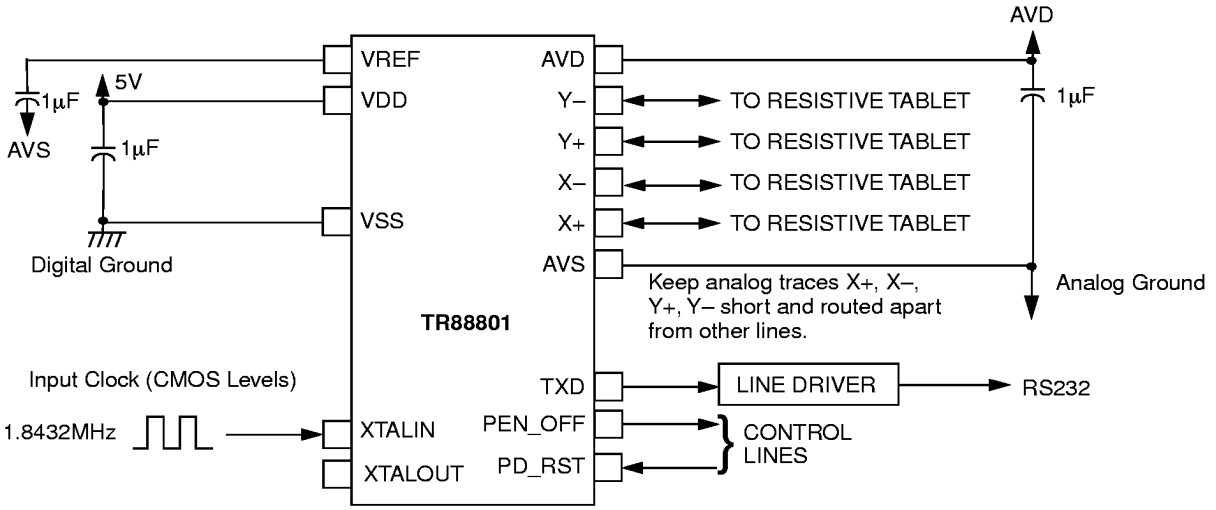
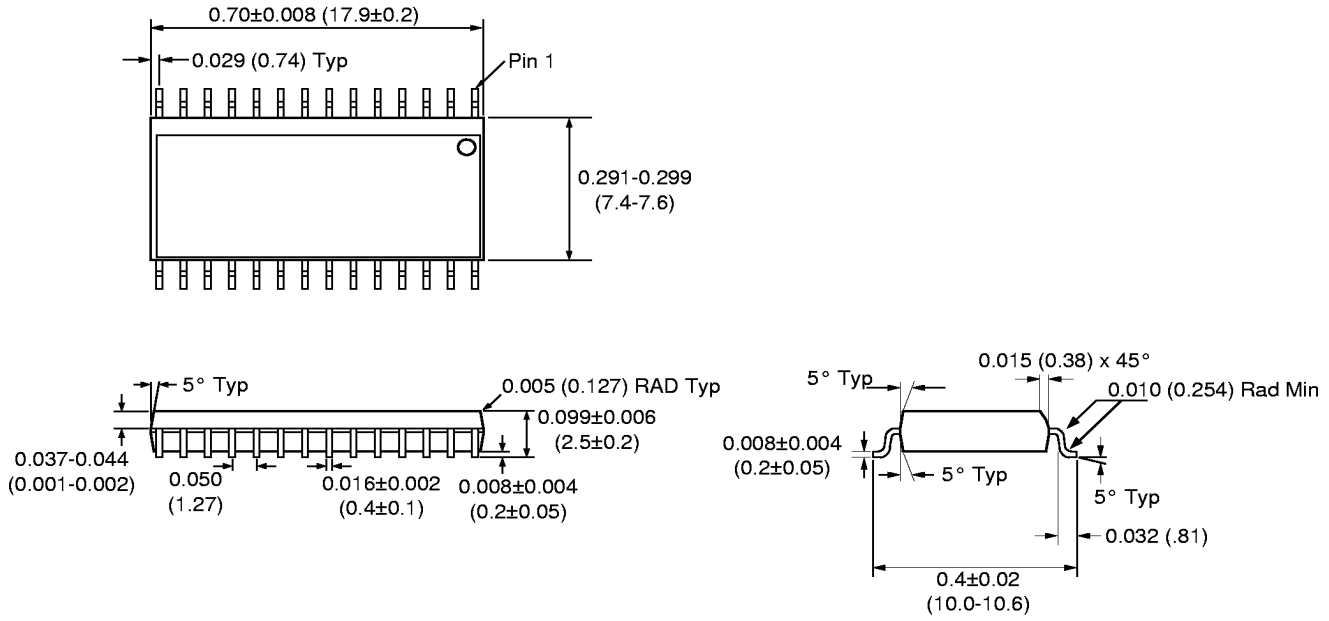


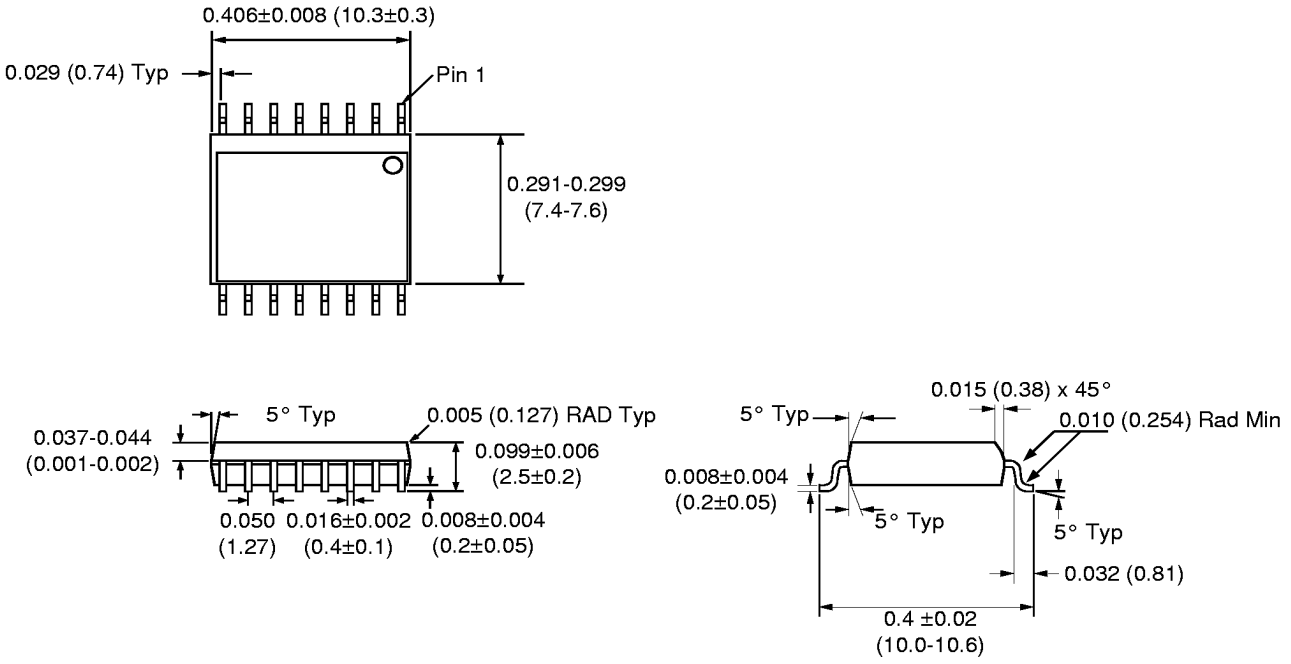
Figure 10 • *Typical Connection Diagram for TR88801*

Mechanical Dimensions

28-pin SOW Dimensions in inches (mm)

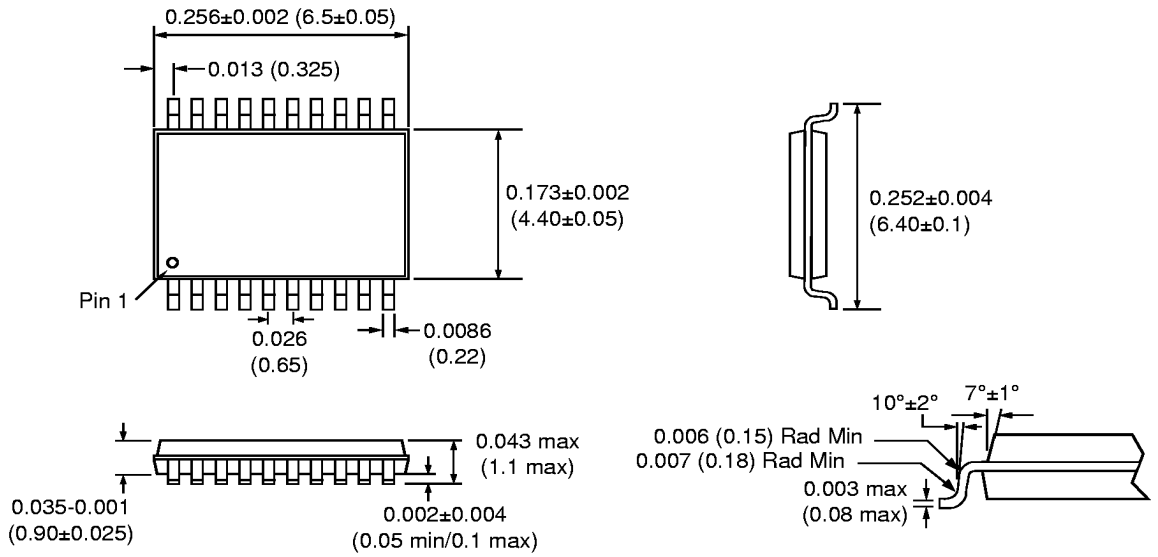


16-pin SOW Dimensions in inches (mm)

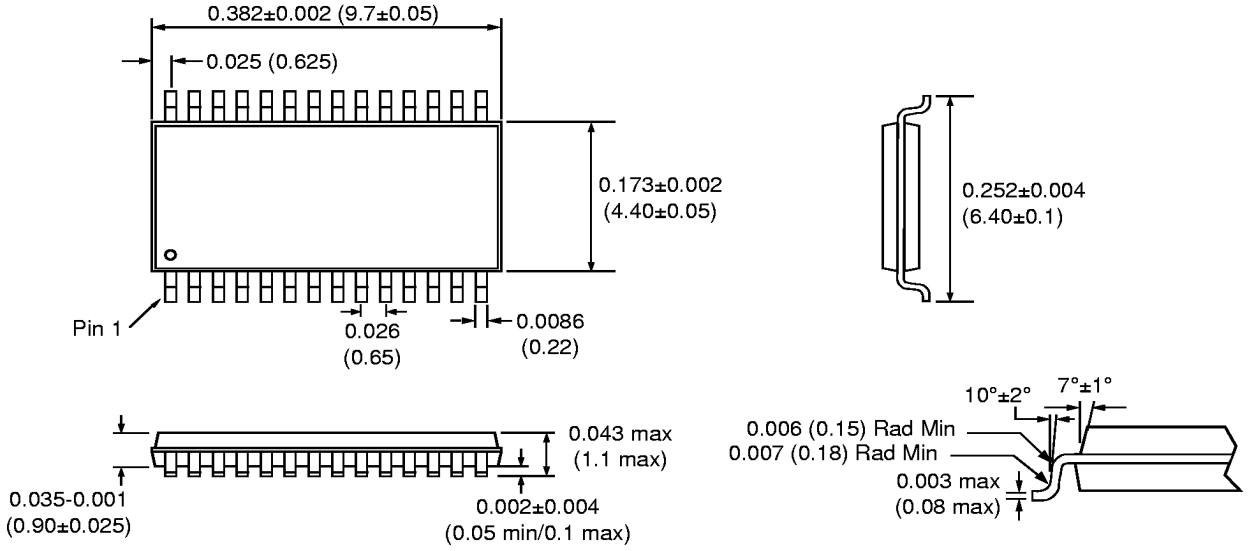


Mechanical Dimensions (continued)

20-pin TSSOP Dimensions in inches (mm)



28-pin TSSOP Dimensions in inches (mm)



Ordering Information

Part Number	Package Type
TR88801CS	16-pin SOW
TR88801CQ	20-pin TSSOP
TR88802CS	28-pin SOW
TR88802CQ	28-pin TSSOP