TOPRO
凌越科技
Topro Technology Inc.

TP6800

Digital Video Camera Controller

(USB interface / JPEG compression / Video processing)

DataSheet

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General Specifications

General Description

The **TP 6800**, a Digital Video Camera controller, is a single-chip solution which supports the full functions including sensor control interface、 regulator、video/color processing、JPEG compression、USB interface. There is no need to use external microprocessor or external memory DRAM /SRAM. In addition, **TP 6800** provides a software driver for PC Camera application solution.

Features

- VGA/CIF USB Camera Solution.
- Support frame rate up to 30fps at VGA mode and CIF mode.
- Built-in MJPEG compression encoder
- Build-in memory.
- Build-in regulator.
- Build-in Phase Lock Loop (PLL).
- Support power from USB port.
- Compact package.

Video Sensor

- Support VGA/CIF Color Sensor
- Support both Master Mode and Slave Mode CMOS Sensor
- Support CCD Sensor plus vertical driver and A/D.
- Support 10 bits Input Raw Data From Sensor.

Interface

- Support USB interface, which is compliant to USB 1.1 high speed and supports four endpoints: control, Isochroous-IN, Bulk-IN, Bulk-OUT
- Support USB suspended high power device.
- All the USB descriptors (VID & PID) can be fetched from internal mask ROM or external EEPROM.

Image compression/Format

- Built-in MJPEG compression encoder.
- Support dynamic compression ratio controller.

Image Processor

- Support 10-bit input raw data from sensor.
- Support Programmable LUT for Gamma correction by driver.
- Support color-processing functions including: interpolation (DeMosaic), GAMMA correction, Auto-White-Balance, Auto Exposure, Edge-Enhancement, False color suppression, Top color tuning, Anti-flicker, Color correction/Color matching, Contract/Brightness control.

Image /Video Data

- Supports Snap Shot Function, and which could be saved as a JPEG file.
- Supports XGA/SVGA Still Image Function.
- Supports VGA/CIF/QCIF/QVGA Still Image Function.
- Supports continuous still image function.
- Supports VGA/CIF/QCIF/QVGA Video Function.

Applications

- PC Camera
- Web Camera

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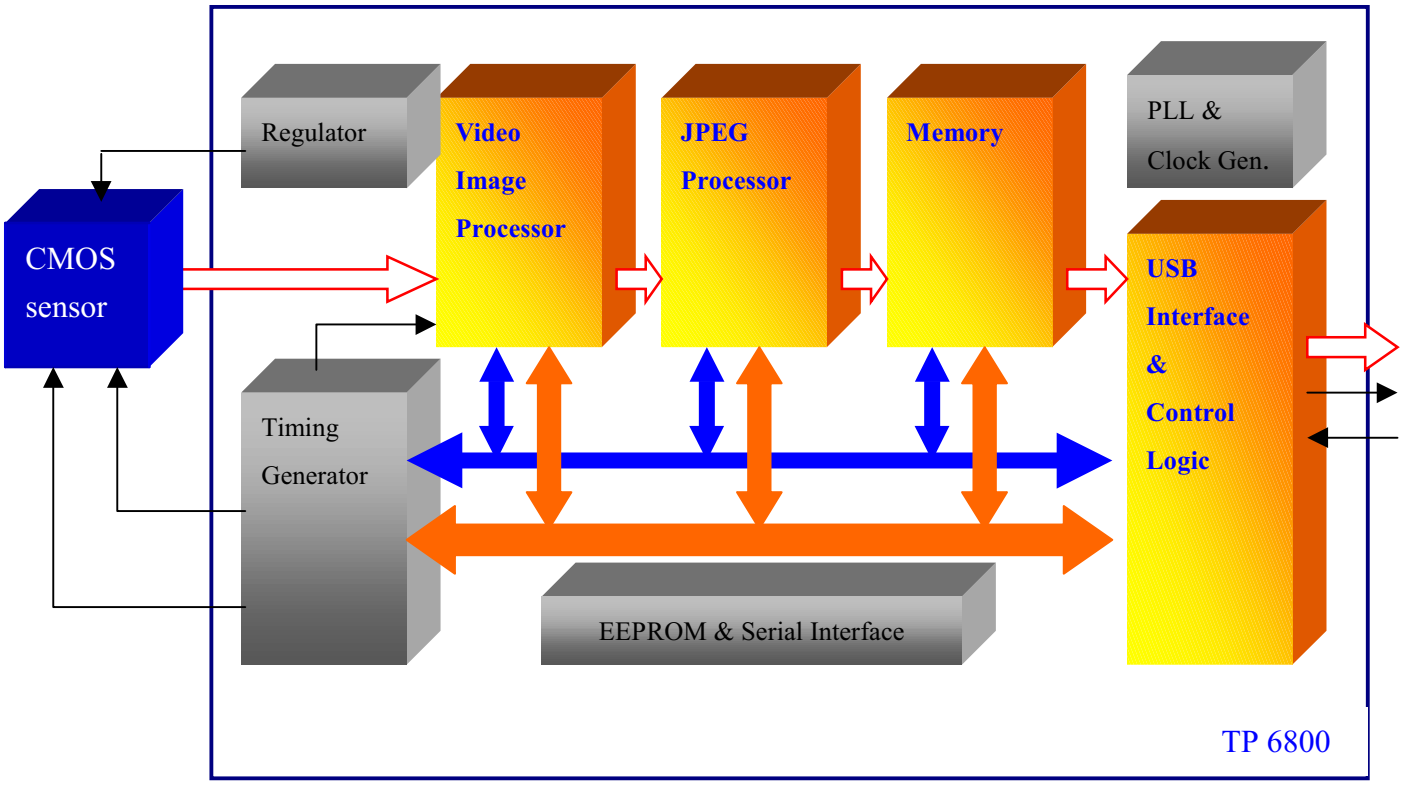
- Security monitor Camera
- Internet video phone
- Microscope

…

Function Block Diagram



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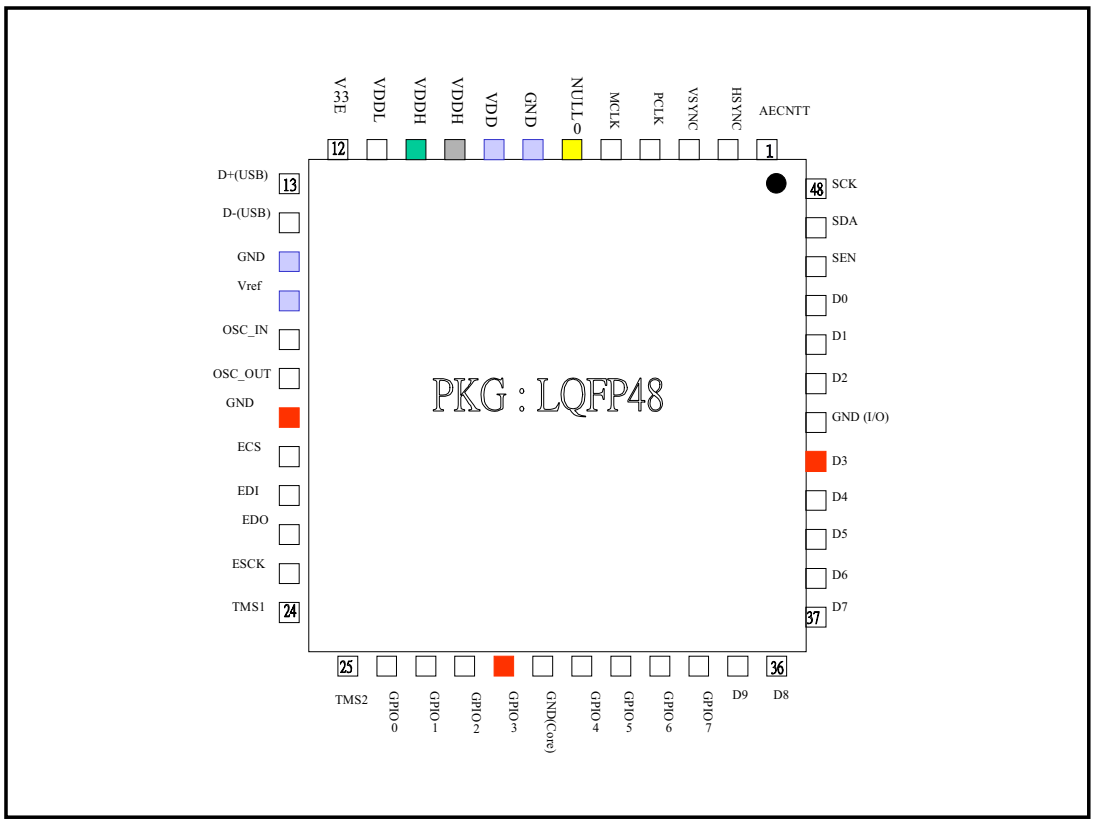
Contents：

Pin Configurations

Package Type: LQFP 48



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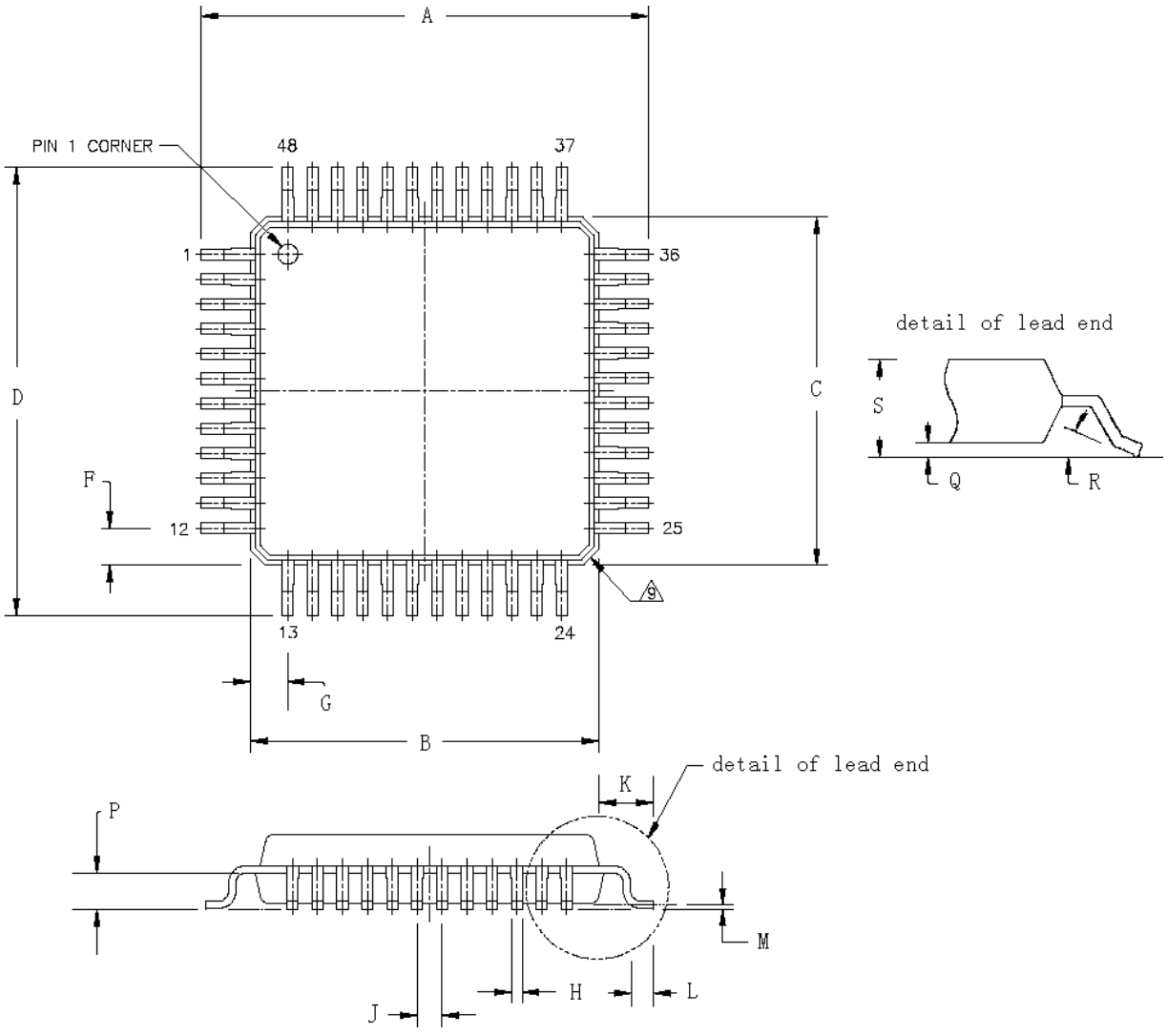
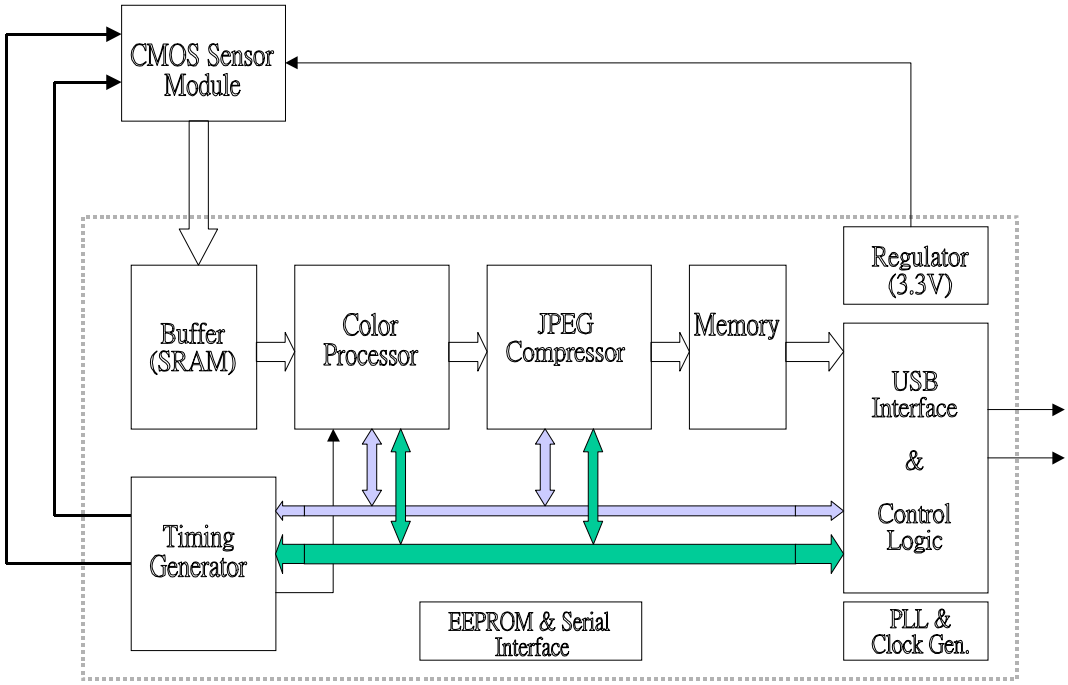


Item	Millimeters	Inches	Item	Millimeters	Inches	Item	Millimeters	Inches
A	9.00	0.354	H	0.22± 0.05	0.008± 0.002			
B	7.00	0.275	J	0.5	0.020			
C	7.00	0.275	K	1.00	0.039	Q	0.1± 0.05	0.004± 0.002
D	9.00	0.354	L	0.6± 0.15	0.024± 0.006	R	5° ± 5°	5° ± 5°
			M	0.1± 0.05	0.004± 0.002	S	1.6 Max	0.063

Pin Description (LQFP48)

Pin	Name	I/O	Function
1	AECNT	O	Auto-exposure control signal of CMOS image sensor.
2	HSYNC	I/O	Horizontal synchronous signal of sensor.
3	VSYNC	I/O	Vertical synchronous signal of sensor.
4	PCLK	I/O	Pixel clock of CMOS image sensor.
5	MCLK	O	Master clock signal of CMOS image sensor.
6	NC	NC	Not connect.
7	GND	PWR	Analog ground for PLL/Regulator
8	VDD	PWR	Power supply of 2.5 volt which is generated by internal regulator.
9,10	VDDH	PWR	Analog power supply for Regulator/PLL
11	VDDL	PWR	Power supply of 3.3 volt which is generated by internal regulator.
12	V33E	PWR	Power supply for external CMOS sensor. This pin will be shutdown in USB suspend mode.
13	D+	I/O	Differential signal of USB interface.
14	D-	I/O	Differential signal of USB interface.
15	GND	PWR	Ground of Analog power supply.
16	Vref	I/O	Reference voltage for analog circuit.
17	OSCIN	I	Input of crystal
18	OSCOUT	I/O	Crystal output or input of external clock signal while working test mode.
19	GND	PWR	Ground of power supply for I/O cells.
20	ECS	O	External EEPROM chip-select pin.
21	EDI	O	External EEPROM data input pin.
22	EDO	I	External EEPROM data output pin.
23	ESCK	O	External EEPROM synchronous clock signal.
24	TMS1	I	Test mode select pin.(With 30K pull-down resistor)
25	TMS2	I	Test mode select pin.(With 30K pull-down resistor)
26-29	GPIO0-3	I/O	Programmable I/O
30	GND	PWR	Ground of internal circuit
31-34	GPIO4-7	I/O	Programmable I/O pins.
35-41,43-45	D9-D0	I	Digital data from CMOS image sensor.
42	GND	PWR	Ground for I/O cells.
46	SEN	O	Enable signal for Serial interface which connect to CMOS image sensor.
47	SDA	I/O	Data signal of serial interface (SPI, I2C…etc.) which connect to sensor.
48	SCK	I/O	CLK signal of serial interface connected to CMOS image sensor.

Functional Block Diagram



Function Descriptions

Special function registers:

1.1 Serial interface related registers

Address	Name	Attribute	Descriptions
10	SIF_TYPE	R/W	Serial interface type b1b0=00 ……I2C interface(Default) b1b0=01 ……SPI interface(TASC) b1b0=10 …….UART(Not implemented) b2=1…16-bit data(photobit)，b2=0…8-bit data (b7,b6,b5,b4,b3 are reserved for future use)
11	SIF_CONTROL	R/W	Serial interface control When read from this register: b0: TX_ACK(1: transferring TX_DATA register is finished, cleared by F/W) b1: RX_ACK(1: received data is available on RX_DATA register. Cleared by F/W) When write to this register: b0: tx_trig(1: trigger to transfer TX_DATA and cleared by H/W when transferring is completed) b1: rx_trig(1: trigger to send slave address and get data from RX_DATA) Be sure to write 1 into tx_trigger/rx_trigger after writing SIF_ADDR_S and SIF_TX/RX_DATA. b7,b6,b5,b4,b3,b2 are reserved for future use.
12	SIF_ADDR_S	R/W	Serial interface slave address (I2C master mode) b7 : X, unused b6 ~ b0 : slave address
19	SIF_ADDR_S2	W	When b1b0 of SIF_TYPE is "00", this register use as the register address of device.
13	SIF_TX_DATA	W	Data register for transferring data to slave
1A	SIF_TX_DATA2	W	Data register for transferring data(2nd byte) to slave
14	SIF_RX_DATA	R	Data register for receiving data from slave.
1B	SIF_RX_DATA2	R	Data register for receiving data(2nd byte)from slave
15	GPIO_PU	W	GPIO pull-up enable(Default = 11111111)
16	GPIO_PD	W	GPIO pull-down enable(Default = 00000000)
17	GPIO_IO	W	GPIO direction control(Default = input)
18	GPIO_DATA	R/W	GPIO data(Default = 00000000) Suggested definition of GPIO as below:

			B7 : SNAP shot button B6 : Power LED(indicator) B5 : reserved B4 : Descriptor selector of internal mask rom. (0: Bank 1， 1: Bank 2) B3 : Before USB SET the device configured, this pin is used as the selector of internal ROM(0) or external EEPROM(1) by connecting a 50KΩ(5V) resistor to pull-up/pull-down . Once the device has been configured by USB command, this port could work as a general-purpose programmable I/O. B2, B1, B0 : Selector of the CMOS sensor bank.

1.2 System related registers:

Address	Name	attribute	Descriptions
21	ENDP_1_CTL (endpoint 1 control register)	W	Bit[0]: Enable bit for endpoint 1 to begin send data.(1: enable，0:disable) Bit[1]: Enable bit for chip internal Timing generator.(1: enable to generate timing signals, 0: disable all the timing sequence signals) Bit[2-7]: reserved.
22	ENDP1_MAX_PackSize **Note :** The value of this register also could be set by usb command "Set Interface", And read by usb command "get Interface".	W	Bit 2/Bit 1/Bit 0 : 000 : Max_PackSize of endpoint 1 is 0.(Default) 001 : Max_PackSize of endpoint 1 is 128 010 : Max_PackSize of endpoint 1 is 256 011 : Max_PackSize of endpoint 1 is 512 100 : Max_PackSize of endpoint 1 is 640 101 : Max_PackSize of endpoint 1 is 768 110 : Max_PackSize of endpoint 1 is 1023 Bit3 - bit7 : reserved.

1.3 Timing Generator related registers

Address	Name	attribute	Descriptions
2F	Timing_CFG Default value : 0Ch	W	Bit[0] : PCLK direction (1: input from sensor， 0: generated by TP6800) Bit[1] : HSYNC/VSYNC direction control (0: output，1: input from sensor) Bit[2] : HSYNC/VSYNC Polarity(1: Active high, 0: Active low) Bit[3] : PCLK2MCLK.(1: Generated PCLK has same phase with MCLK, otherwise they have different phase)

			Bit[4]：PCLK phase indicator.(See the description of timing generator below) Bit[5] : When this bit set to "1" means the Sensor output data change value at Positive edge of PCLK, and when this bit reset to "0", it means sensor output data change value at negative edge of PCLK。 Bit[6]：All the signals(dark_pix, first_pix, last_pix, line_en, ID, sensor data) will delay half cycle when set to "1"。 Bit[7]：when this bit set to "1", chip will enter customer testing mode, otherwise chip will under normal working mode。
30	SENSOR_CFG Default value : 00h	R/W	Sensor configuration Bit[7]：reserved. Bit[6]：reserved. Bit[5]：reserved. Bit[4:3]: color filter type 00: RG0 … G1B … 01: G0R … BG1 … 10: BG1 … G0R … 11: G1B … RG0 … **ID[1]/ID[0] of interface between TG & Color processing unit：** 0/0 : **R** 0/1 : **G0** 1/0 : **G1** 1/1 : **B** Bit[2]: reserved Bit[1]: reserved Bit[0]: reserved
31	PIXEL_START Default value : 3CH(60d)	W	Window horizontal start
32 33	PIXEL_END_L (32H) PIXEL_END_H (33H) Default value : x2BBH	W	Window horizontal end (lower byte & higher byte)

34	LINE_START Default value : 09H	W	Window vertical start
35 36	LINE_END_L(35H) LINE_END_H(36H) Default value : x1E8H	W	Window vertical end (lower byte & higher byte)
37	FRONT_DARK_ST Default value : 3AH(58d)	W	Front dark start
38	FRONT_DARK_END Default value : 3AH(58d)	W	Front dark end
39 3A	REAR_DARK_ST_L REAR_DARK_ST_H Default value : x2C6(700)	W	Rear dark start (lower byte & higher byte)
3B 3C	REAR_DARK_END_L REAR_DARK_END_H Default value : x31A(794)	W	Rear dark end (lower byte & higher byte)
3D 3E	Horizontal Dark Line control register 3D: low-byte, 3E: high-byte Default value(3DH) : 07H Default value(3EH) : 88H	W	Start Line # : Bit[9-0] Dark Line number : Bit[14-10] Bit[15] : Enable bit(1: This register is enable, otherwise there will be no dark-pixel lines)
3F	FRAME_RATE (MCTL=0, 2x clock mode) (MCTL=1, 1x clock mode)	R/W	Bit[2:0] : used to select Master clock rate.(MCLK) 000 : 2.5fps(Master clock = 1MHz，MCTL=1) 001 : 5fps(Master clock=2MHz，MCTL=1) 010 : 7.5fps(Master clock=3MHz，MCTL=1) 011 : 10fps(Master clock=4MHz，MCTL=1) 100 : 15fps(Master clock=6MHz，MCTL=1)

40 41	EXPOSURE_L[7:0] EXPOSURE_H[1:0]	W	EXPOSURE(10 bits) : EXPOSURE[1:0] + EXPOSURE[7:0] is used to program the Auto-exposure timing control of AECNT which is valid when this chip(6800) is connected to TASC VGA Sensor。
42 43	VSYNC_EN_PERIOD_L VSYNC_EN_PERIOD_H Default value : 550	W	
44	VSYNC_DIS_PERIOD Default value : 28H(40)	W	
45 46	HSYNC_EN_PERIOD_L HSYNC_EN_PERIOD_H Default value : x320H(800)	W	
47	HSYNC_DIS_PERIOD Default value : 24H(36)	W	
48 49	HSYNC_TO_VSYNC_L HSYNC_TO_VSYNC_H Default value : x190H(400)	W	

1.4 Image Processor related registers

address	Name	attribute	Descriptions
54	DARK_CFG	R/W	Dark level compensation configuration Bit[2]: bad concealment for under low threshold Bit[1]: bad concealment for over high threshold Bit[0]: dark subtraction enable
55	GAMMA_R	R/W	Gamma table entry point for R
56	GAMMA_G	R/W	Gamma table entry point for G
57	GAMMA_B	R/W	Gamma table entry point for B
58	reserved	R/O	

59	reserved	R/O	
5a	reserved	R/O	
5b	reserved	R/O	
5c	EDGE_THRLD	R/W	Edge enhancement low threshold
5d	DEMOSAIC_CFG	R/W	Image Processor configuration Bit[4]: gray mode Bit[3]: grid compensation enable Bit[2]: scaling down enable Bit[1:0]: 0: edge enhance ooff 1: slight edge enhancement 2: medium edge enhancement 3: strong edge enhancement
5e	Reserved	R/O	
5f	Reserved	R/O	
60	Y_GAIN_RL	R/W	Parameter Y_GAIN_R (lower byte)
61	Y_GAIN_RH	R/W	Parameter Y_GAIN_R (higher byte)
62	Y_GAIN_GL	R/W	Parameter Y_GAIN_G (lower byte)
63	Y_GAIN_GH	R/W	Parameter Y_GAIN_G (higher byte)
64	Y_GAIN_BL	R/W	Parameter Y_GAIN_B (lower byte)
65	Y_GAIN_BH	R/W	Parameter Y_GAIN_B (higher byte)
66	U_GAIN_RL	R/W	Parameter U_GAIN_R (lower byte)
67	U_GAIN_RH	R/W	Parameter U_GAIN_R (higher byte)
68	U_GAIN_GL	R/W	Parameter U_GAIN_G (lower byte)
69	U_GAIN_GH	R/W	Parameter U_GAIN_G (higher byte)
6a	U_GAIN_BL	R/W	Parameter U_GAIN_B (lower byte)
6b	U_GAIN_BH	R/W	Parameter U_GAIN_B (higher byte)
6c	V_GAIN_RL	R/W	Parameter V_GAIN_R (lower byte)
6d	V_GAIN_RH	R/W	Parameter V_GAIN_R (higher byte)
6e	V_GAIN_GL	R/W	Parameter V_GAIN_G (lower byte)
6f	V_GAIN_GH	R/W	Parameter V_GAIN_G (higher byte)
70	V_GAIN_BL	R/W	Parameter V_GAIN_B (lower byte)
71	V_GAIN_BH	R/W	Parameter V_GAIN_B (higher byte)
80	ACC_R0	RO	R accumulator byte 0
81	ACC_R1	RO	R accumulator byte 1
82	ACC_R2	RO	R accumulator byte 2
83	ACC_R3	RO	R accumulator byte 3
84	ACC_G0	RO	G accumulator byte 0
85	ACC_G1	RO	G accumulator byte 1

86	ACC_G2	RO	G accumulator byte 2
87	ACC_G3	RO	G accumulator byte 3
88	ACC_B0	RO	B accumulator byte 0
89	ACC_B1	RO	B accumulator byte 1
8a	ACC_B2	RO	B accumulator byte 2
8b	ACC_B3	RO	B accumulator byte 3
8c	MAX_R	RO	Maximum value for R
8d	MAX_G	RO	Maximum value for G
8e	MAX_B	RO	Maximum value for B
8f	MAX_Y	RO	Maximum value for Y
90	ACC_Y0	RO	Y accumulator byte 0
91	ACC_Y1	RO	Y accumulator byte 1
92	ACC_Y2	RO	Y accumulator byte 2
93	ACC_Y3	RO	Y accumulator byte 3

1.5 JPEG Compression related registers

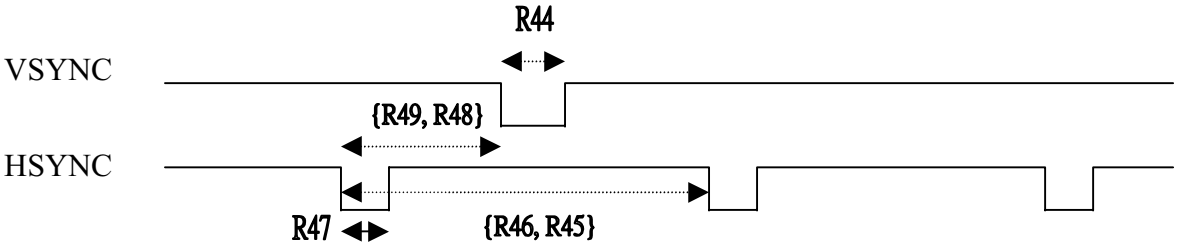
address	Name	attribute	Descriptions
78	FORMAT	R/W	Bit[2:0]JPEG Compression Format 0: VGA (640x480) 1: QVGA (320x240) 2: CIF (352x288) 3: QCIF (176x144) 4: SIF (352x240) 5: QSIF (176x120) 6: reserved (640x240 from NTSC ?) 7: reserved (640x288 from PAL/SECAM?) Bit[3]: Raw data mode enable
79	QUALITY	R/W	JPEG compression quality factor 0~31 0: good quality 15: smallest size 16~31: ultra fine quality
7a	BLK_THRLD	R/W	JPEG block size threshold, parameter for internal compression control Average byte count of each block is recommended for this register Ex. Bandwidth = 850000 byte/sec BLK_THRLD = 850000 / (hsize * vsize * fram_rate / 32)
7b	BUFFER_STATUS	R/O	USB Buffer status[4:0]

			Bit[4]: buffer full Bit[3]: buffer almost full at maximum threshold Bit[2]: buffer almost full Bit[1]: buffer almost full Bit[0]: buffer almost full at minimum threshold
7c	Reserved	R/O	
7d	Reserved	R/O	
7e	Reserved	R/O	
7f	Reserved	R/O	

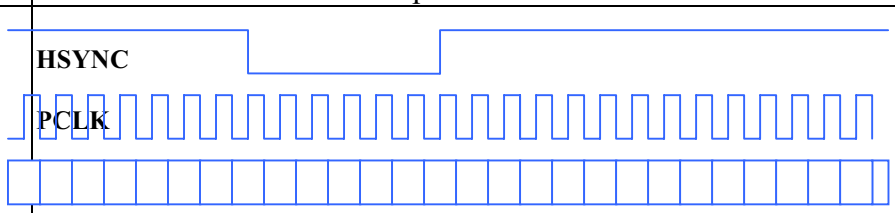
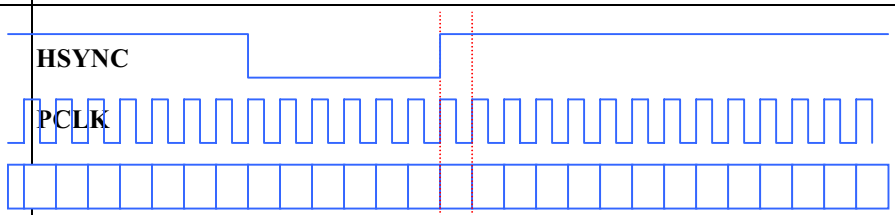
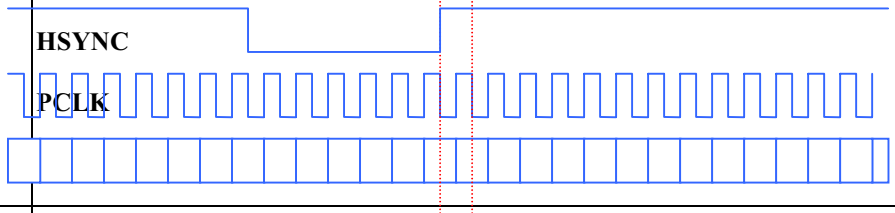
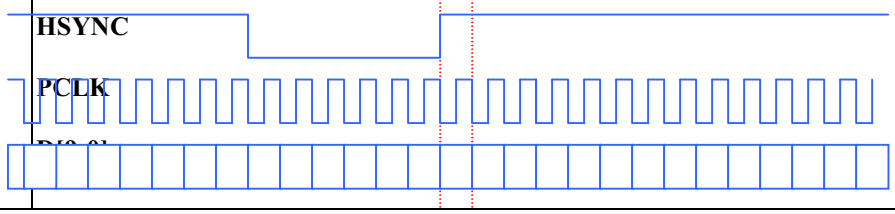
Timing generator ：

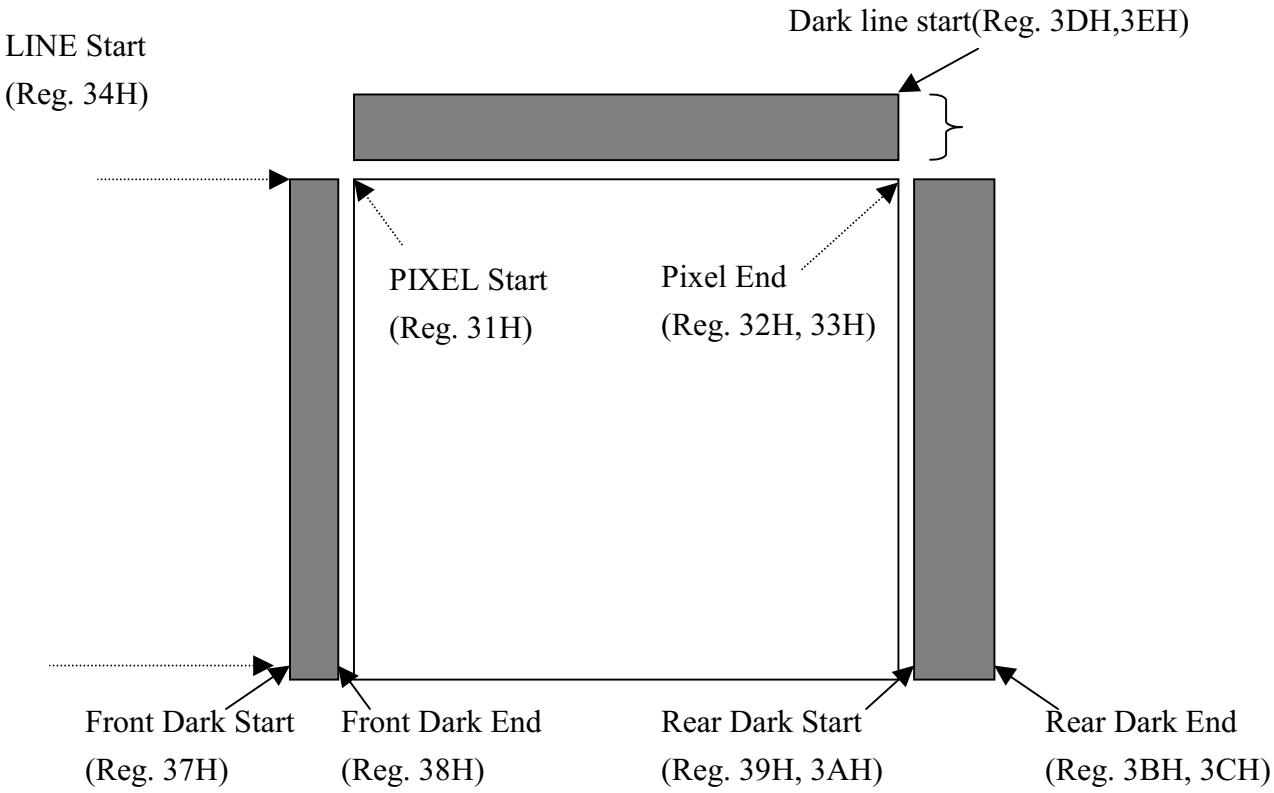
Note 1：All the values of R44, R45, R46, R47, R48, R49 are number of PCLK

Note 2：The value of R42, R43 is the number of HSYNC which counted starts after VSYNC



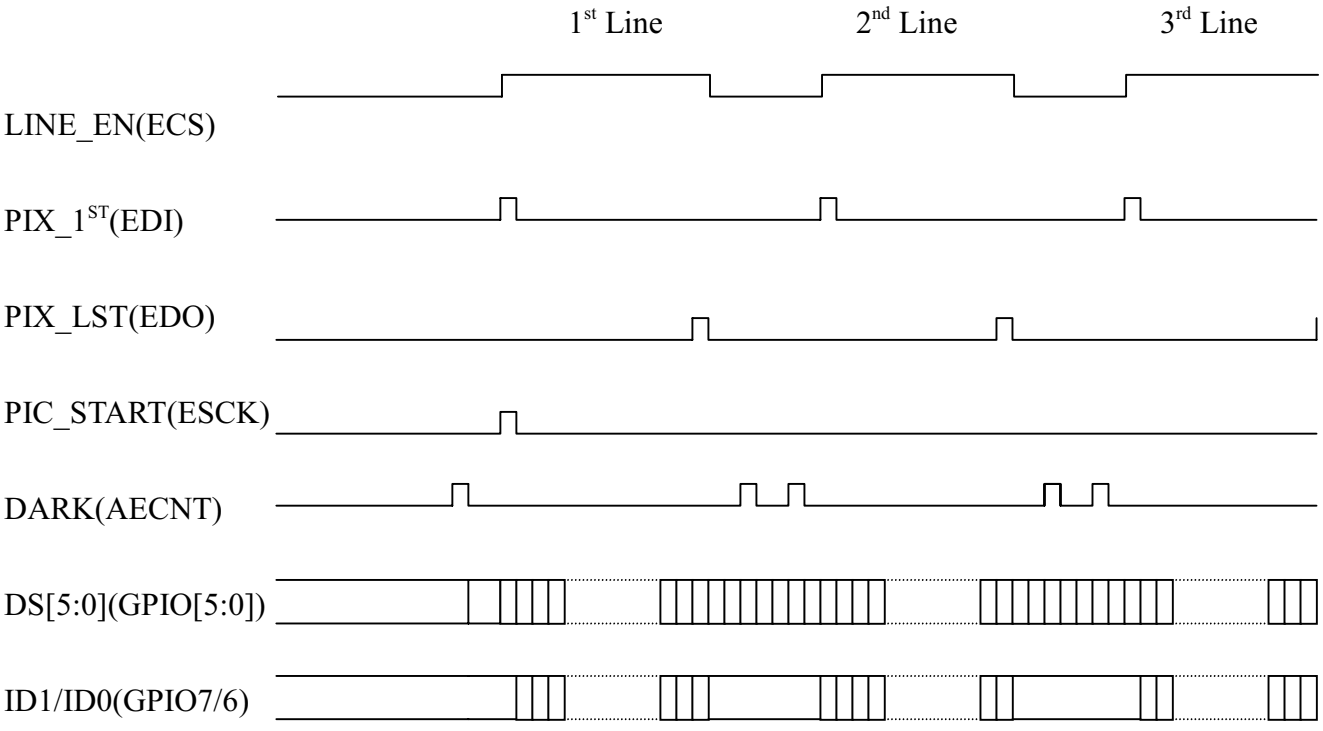
Reg.**2F**H：

bit5 / bit4	Description of PCLK & Sensor data
00	
10	
11	
01	


LINE Start
(Reg. 34H)
Dark line start(Reg. 3DH,3EH)
PIXEL Start
(Reg. 31H)
Pixel End
(Reg. 32H, 33H)
Front Dark Start
(Reg. 37H)
Front Dark End
(Reg. 38H)
Rear Dark Start
(Reg. 39H, 3AH)
Rear Dark End
(Reg. 3BH, 3CH)

Customer Testing mode：

When bit7 of register(2Fh) set to "1", TP6800 will enter customer testing mode. In this mode, Customer can find the proper value of all the registers related to Sensor's timing which will generate exact waveform of internal signals which could be observed at I/O pins.



USB Commands :

Command :	**Content :** (bmRequestType),(bRequest),(wValue),(wIndex),(wLength) (wValue) = (low-byte, high-byte) (wIndex) = (low-byte, high-byte) (wLength) = (low-byte, high-byte)	
Clear feature	(00) (01) (01,00) (00,00) (00,00) (02) (01) (00,00) (endp#, 00) (00,00)	Disable remote wakeup Clear endp# HALT
Set feature	(00) (03) (01,00) (00,00) (00,00) (02) (03) (00,00) (endp#,00) (00,00) endp# : b7 -> direction bit(0:OUT，1:IN) b6b5b4 : 000 b3b2b1b0 : endpoint number	Enable remote-wakeup Set endp# Stall(Halt)
Get configuration	(80) (08) (00,00) (00,00) (01,00)	Get Config. value
Set configuration	(00) (09) (Config. Value) (00,00) (00,00)	Set Config. value
Get descriptor	(80) (06) (index, type) (zero) (descriptor length)	Get all descriptors
Set descriptor	Not supported. (Device will response "STALL" while Host issue this command)	
Get interface	(81) (0A) (00,00) (interface #) (01,00)	Device will response this request by sending the alternative setting value of interface
Set interface	(01) (0B) (Alternative setting) (Interface #) (00,00) Alternative value : 00, 01, 02, 03, 04, 05, 06 Interface # : 00(high byte)，00(low byte)	Host will set the alternative setting value of this interface
Get status	(80) (00) (00,00) (00,00) (02,00) (81) (00) (00,00) (interface #,00) (02,00) (82) (00) (00,00) (endp #,00) (02,00)	Status of Device Status of interface Status of endpoint
Set address	(00) (05) (Device address value) (00,00) (00,00)	Host will set the device address
Read register	(C1) (0D) (00,00) (Address, 00) (01,00)	
Write register	(41) (0E) (value,00) (Address, 00) (00,00)	

USB Endpoint functional descriptions:

(1) Endpoint 0：(Control pipe)

(2) Endpoint 1：(Isochronous IN)

This endpoint is used to transfer image data. The first byte of each USB transaction is a control byte used to note the image stream, and the rest of the transaction stream is the image data. There are three kinds of control byte which is described below:

2'h55 : The start of image frame.

2'hAA : Abandoned image stream. The new image frame will be send in the following new transaction.

2'hCC : The valid image stream.

(3) Endpoint 2：(Bulk-IN)

This endpoint is used to transfer the register values of 80H to 93H. These registers also can be accessed by SETUP command of endpoint 0, but it will cost less timing to fetch these register values by single Bulk-IN transaction instead of many SETUP transfers which may need few "ms" to complete.

(4) Endpoint 3：(Bulk-OUT)

This type of transaction is used to transfer the color parameters and Gamma table from PC to chip. The first byte of this transaction is a control byte which is used to indicate whether the data is parameter, R Gamma table, G Gamma, or B Gamma table. The description of control byte is as following:

2'h03 ： 18 bytes of Color parameters will write into register 60H - 71H

2'h00 ： 1024 bytes of R Gamma table(10-bit) will write into register 55H by 1024 times.

2'h01 ： 1024 bytes of G Gamma table(10-bit) will write into register 56H by 1024 times.

2'h02 ： 1024 bytes of B Gamma table(10-bit Gamma table) will write into register 57H by 1024 times.

- *Note. The Gamma table is designed for 10-bit data. If you just want to fill 256 byte(for 8 bit data), you still have to fill 1024 bytes into 55H/56H/57H。*

ROM address mapping for Descriptor & string :(512 Bytes)

000		Bank 1
001		
002		
003		
004		
⋮	⋮	
0FA	Address of Endpoint #3 descriptors	
0FB	Address of Endpoint #2 descriptors	
0FC	Address of Endpoint #1 descriptors	
0FD	Address of interface descriptors	
0FE	Address of Configuration descriptors	
0FF	Address of Device descriptor	
100		Bank 2
101		
102		
103		
104		
1F0		
1F1		
1F2		
1F3		
1F4		
1F5	Address of strings describing interface #1(index=5)	
1F6	Address of strings describing configuration(index=4)	
1F7	Address of strings describing serial number(index=3)	
1F8	Address of strings describing product(index=2)	
1F9	Address of strings describing manufacturer(index=1)	
1FA	Address of Endpoint #3 descriptors	
1FB	Address of Endpoint #2 descriptors	
1FC	Address of Endpoint #1 descriptors	
1FD	Address of interface descriptors	
1FE	Address of Configuration descriptors	
1FF	Address of Device descriptor	

USB Device Descriptors:

Offset	Field	Value
0	bLength	12
1	bDescriptorType	01
2	bcdUSB	0101
4	bDeviceClass	00
5	bDeviceSubClass	00
6	bDeviceProtocol	00
7	bMaxPacketSize	08
8	idVendor	06a2(TOPRO)
10	idProduct	0001
12	bcdDevice	0000
14	iManufacturer	00
15	iProduct	00
16	iSerialNumber	00
17	bNumConfigurations	01

When bit3 of GPIO is "1"
During USB reset signal,
The following data will be read
from external EEPROM

Data Read from External EEPROM	Customer VendorID
	idProduct
	bcdDevice
	00
	00

Configuration descriptors:

Offset	Field	Value
0	bLength	09
1	bDescriptorType	02
2	wTotalLength	db(219)
4	bNumInterfaces	01
5	bConfigurationValue	01
6	iConfiguration	00
7	bmAttributes	A0
9	Maxpower	32

NOTE： The bConfiguration has to be value of "01" in order to match TP6800

, because it is default in chip. Please refer to USB specification v1.1 (Chapter 9.4.7)

Interface 0 descriptors :(Alternate setting 0, 1, 2, 3, 4, 5, 6)

Offset	Field	Alternate Setting 0	Alternate setting 1	Alternate setting 2	Alternate setting 3	Alternate setting 4	Alternate setting 5	Alternate setting 6
0	bLength	09	09	09	09	09	09	09
1	bDescriptorType	04	04	04	04	04	04	04
2	bInterfaceNumber	00	00	00	00	00	00	00
3	bAlternateSetting	00	01	02	03	04	05	06
4	bNumEndpoint	03	03	03	03	03	03	03
5	bInterfaceClass	ff	ff	ff	ff	ff	ff	ff
6	bInterfaceSubClass	00	00	00	00	00	00	00
7	bInterfaceProtocol	ff	ff	ff	ff	ff	ff	ff
8	iInterface	00	00	00	00	00	00	00

Endpoint 1 descriptors : (ISO-IN)

Offset	Field	Alternate Setting 0	Alternate setting 1	Alternate setting 2	Alternate setting 3	Alternate setting 4	Alternate setting 5	Alternate setting 6
0	bLength	07	07	07	07	07	07	07
1	bDescriptorType	05	05	05	05	05	05	05
2	bEndpointAddress	81	81	81	81	81	81	81
3	bmAttributes	01	01	01	01	01	01	01
4	wMaxPacketSize	0000	0080	0100	0200	0210	0300	03FF
6	bInterval	01	01	01	01	01	01	01

Endpoint 2 descriptor : (Bulk-IN)

Offset	Field	Alternate Setting 0	Alternate setting 1	Alternate setting 2	Alternate setting 3	Alternate setting 4	Alternate setting 5	Alternate setting 6
0	bLength	07	07	07	07	07	07	07
1	bDescriptorType	05	05	05	05	05	05	05
2	bEndpointAddress	82	82	82	82	82	82	82
3	bmAttributes	02	02	02	02	02	02	02
4	wMaxPacketSize	0020	0020	0020	0020	0020	0020	0020
6	bInterval	00	00	00	00	00	00	00

Endpoint 3 descriptor：(Bulk-OUT)

Offset	Field	Alternate Setting 0	Alternate setting 1	Alternate setting 2	Alternate setting 3	Alternate setting 4	Alternate setting 5	Alternate setting 6
0	bLength	07	07	07	07	07	07	07
1	bDescriptorType	05	05	05	05	05	05	05
2	bEndpointAddress	03	03	03	03	03	03	03
3	bmAttributes	02	02	02	02	02	02	02
4	wMaxPacketSize	0020	0020	0020	0020	0020	0020	0020
6	bInterval	00	00	00	00	00	00	00

Implementation of USB Driver：

A). Initial USB Device ：

All the functions won't be enabled before device has been set configuration.

1. **Get device descriptor(8 bytes) :** To check the **MaxPacketSize** of device
2. **Set device address：**
3. **Get All Device descriptor(18 Bytes)**：To get the device information
4. **Get all configuration descriptors**
5. **Set device configuration**：To make all the USB commands enabled

B). Initial CMOS Sensor：

1. **Read register (18h) to check b2b1b0 in order to find the sensor manufacturer.**
2. **Write register (30H) to determine the sensor type and color filter type**
3. **Write register (3FH) to determine the Master clock rate for sensor**
4. **Write register (10H) to determine the Serial interface Type in order to set up sensor**
5. **Use register 11H，12H，19H，13H，1AH to set up sensor through Serial I/F**
6. **Use registers 31H ~ 3FH to determine the timing of sensor(HSYNC，VSYNC).**

C). Initial Color processing unit：

D). Initial JPEG Unit：

E). Check Snap-shot Button：

1. **Read register (18H) to check b7. if b7=0, the button is pressed.**

Absolute Maximum Ratings

Parameter	Min.	Ratings	Max.	Unit
Supply voltage	-0.3		5.5	V
Temperature under bias	0		70	ºC
Storage temperature range	-65		150	ºC
Power dissipation	-		500	mW

DC Electrical Characteristic (Ta=25 to 70 °C)

Parameter	Sym.	Min.	Typ.	Max.	Unit
Operating voltage	V_{DD}	4.25	5.0	5.5	V
Operating current (without sensor)@12MHz	Iop	68.1		85.7	mA
Suspend current	Isu			2.8	mA
I/O level	Voh	3.5			V
I/O level	Vol			80	mV
Regulator voltage	Vr	3.4		3.66	V

* All voltages in above table are compared with V_{SS}.

**** All parameters in above table are tested under V_{DD}=5V.***

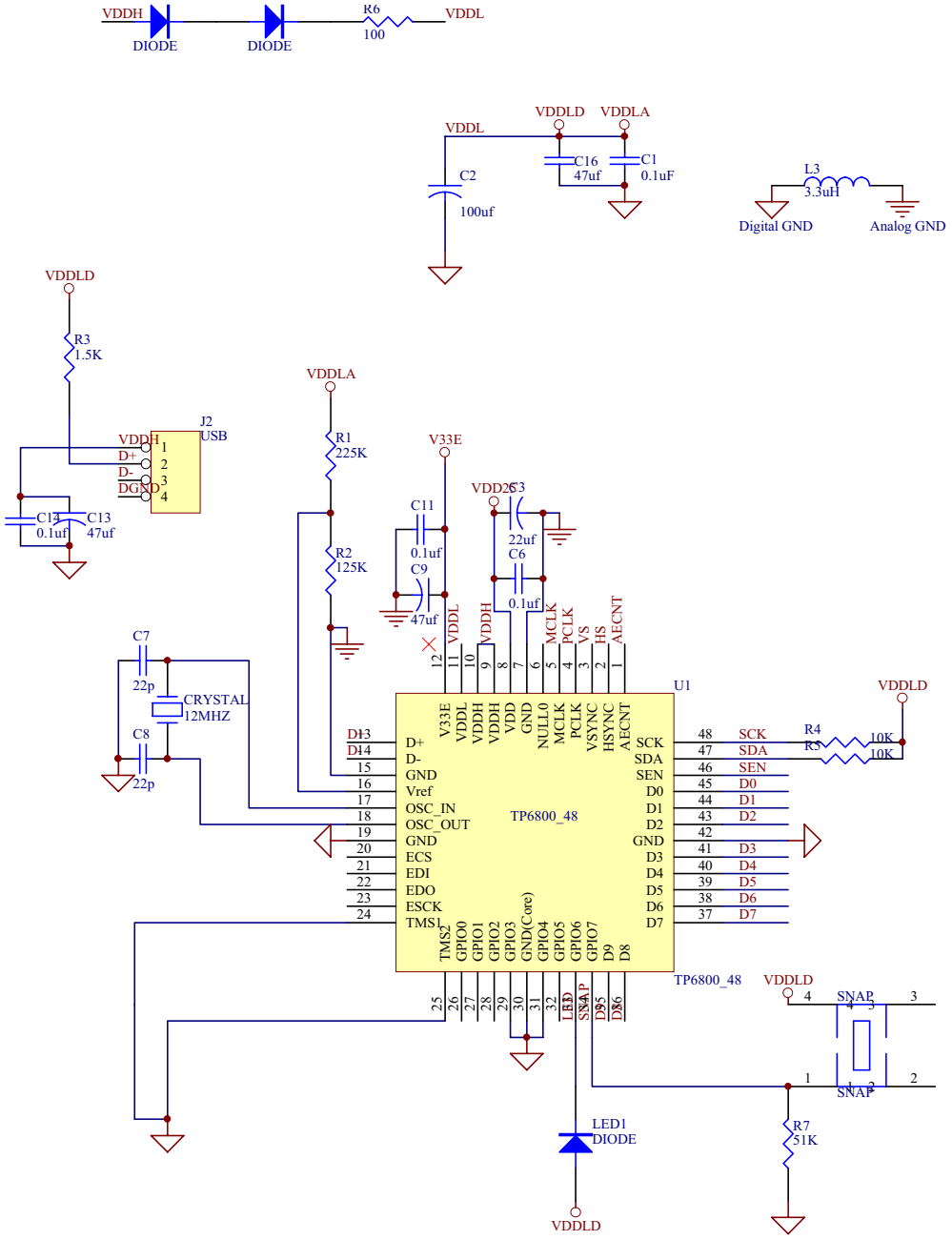
AC Electrical Characterisitics (Ta=25 to 70 °C)

Parameter	Sym.	Min.	Typ.	Max.	Unit

PS. The AC timings are measured with 12MHz system clock signal.

Application Notes

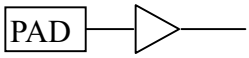
Reference Circuit for PC camera



I/O cell Types:

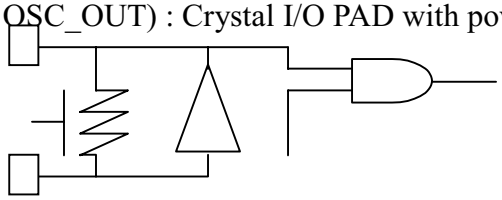
(1) Pin1, 2, 3, 4, 10, 11, 14, 26, 39, 52: power PAD(VDD & GND)

(2) Pin17，Pin32~38，Pin40~42(D0~D9) : Input only buffer

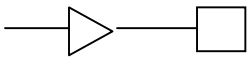


(3) Pin8, 9 : Bi-directional USB PAD

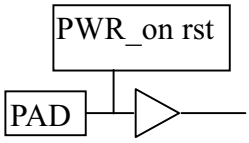
(4) Pin12, 13(OSC_IN，OSC_OUT) : Crystal I/O PAD with power-down pin(12MHz)



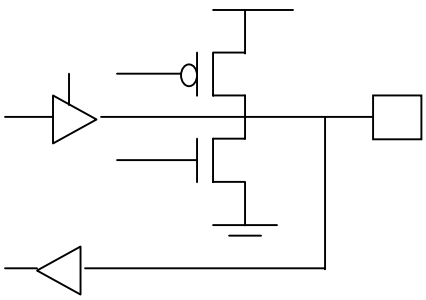
(5) Pin15, 16, 18(ECS，EDI，ESCK)，Pin43(SEN)，Pin46(AECNT)，Pin50(MCLK) : Output buffer PAD



(6) Pin21(Reset) : Input buffer PAD with internal power-on reset ckt



(7) Pin22~25，Pin27~30(GPIO0~7) : Bi-directional I/O buffer with programmable pull-up/down resistor



(8) Pin44, 45(SDA, SCK)，Pin47, 48, 49(HSYNC, VSYNC, PCLK) : Bi-directional I/O buffer