8-bit Low pin count Microcontrollers, 0-66 MHz

1. Description

TEMIC T8xC5101/02 family is a high performance CMOS ROM, OTP, EPROM derivative of the 80C51 CMOS single chip 8-bit microcontroller.

The T8xC5101/02 family is a low pin count device where only Port 1, port 3 and 2/6 bits of a new port 4 are outputted. This prevents to do any external access, like external program memory access (fetch, MOVC) or external data memory (MOVX)

The T8xC5101/02 family retains all features of the TEMIC 80C51 with extended capacity 8Kb ROM (5102), 16Kb ROM (5101) / 16Kb EPROM/OTP (5101) , 256 bytes of internal RAM, a 6-source, 4-level interrupt system, an on-chip oscillator and three timer/counters.

In addition, the T8xC5101/02 family has an XRAM of 256 bytes, the X2 feature, a more versatile serial channel that facilitates multiprocessor communication (EUART), a dual data pointer and an improved timer 2.

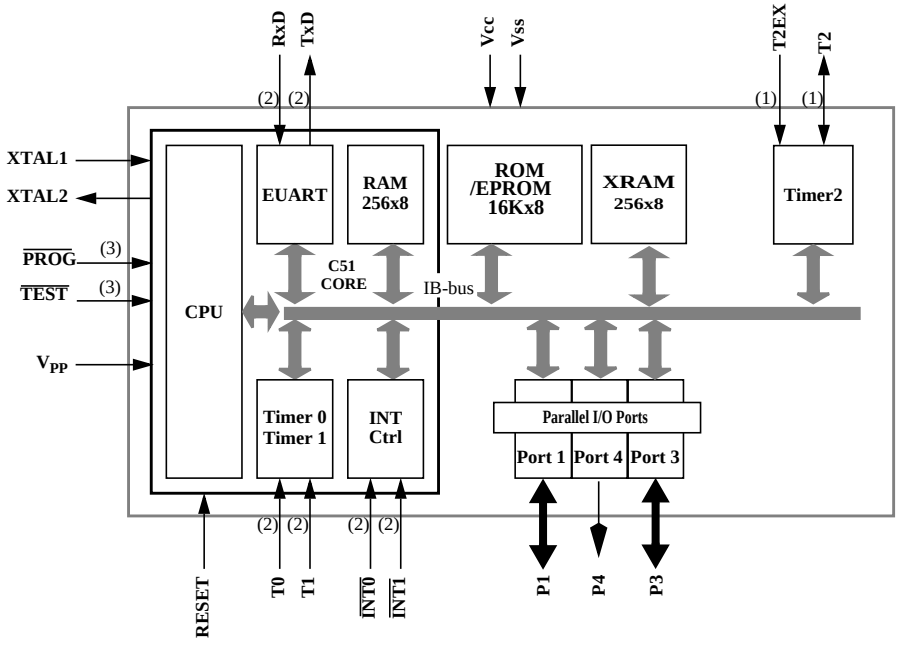
The fully static design of the T8xC5101/02 family allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.

The T8xC5101/02 family has 2 software-selectable modes of reduced activity for further reduction in power consumption. In the idle mode the CPU is frozen while the timers, the serial port and the interrupt system are still operating. In the power-down mode the RAM is saved and all other functions are inoperative.

2. Features

- 80C51 code Compatible
  - 8051 instruction compatible
  - 16 I/O + 2 Outputs in 24 pin packages
    16 I/O + 6 Outputs in 28 pin packages
  - Three 16-bit timer/counters
  - 256 bytes scratchpad RAM
- Program Memory
  - 8Kb ROM T83C5102
  - 16Kb ROM T83C5101
  - 16Kb EPROM/OTP T87C5101
- High-Speed Architecture
  - 40 MHz from 2.7 to 5.5V, commercial or industrial temperature range :
    - 40 MHz with a 40 MHz crystal in std mode
    - 40 MHz with a 20 MHz crystal in X2 mode
  - 66 MHz from 4.5 to 5.5V, commercial temperature range
    - 40MHz with a 40 MHz crystal in std mode
    - 66MHz with a 33MHz crystal in X2 mode
- Dual Data Pointer
- On-chip eXpanded RAM (XRAM) (256 bytes)
- Programmable Clock Out and Up/Down Timer/ Counter 2
- Asynchronous port reset
- Interrupt Structure with
  - 6 Interrupt sources,
  - 4 level priority interrupt system
- Full duplex Enhanced UART
  - Framing error detection
  - Automatic address recognition
- Low EMI (no ALE)
- Power Control modes
  - Idle mode
  - Power-down mode
- Packages: SO24, DIL24, TSSOP24*, SO28*
  * check for availability

3. Block Diagram



(1): Alternate function of Port 1
(2): Alternate function of Port 3
(3): Multiplexed function of Port 4.

4. SFR Mapping

The Special Function Registers (SFRs) of the T8xC5101/02 fall into the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP, AUXR1
- I/O port registers: P1, P3, P4
- Timer registers: T2CON, T2MOD, TCON, TH0, TH1, TH2, TMOD, TL0, TL1, TL2, RCAP2L, RCAP2H
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON
- Power and clock control registers: PCON
- Interrupt system registers: IE, IP, IPH
- Others: AUXR, CKCON

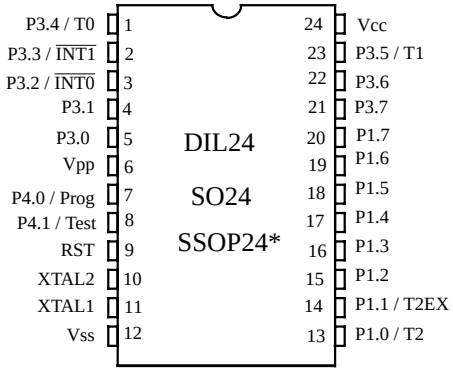
No write must be made to reserved areas. Reading a reserved area will give indeterminate result.

Table 1. All SFRs with their address and their reset value

	Bit address-able	**Non Bit addressable**						
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h									FFh
F0h	B 0000 0000								F7h
E8h									EFh
E0h	ACC 0000 0000								E7h
D8h									DFh
D0h	PSW 0000 0000								D7h
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			CFh
C0h	P4 XX11 1111								C7h
B8h	IP XX00 000	SADEN 0000 0000							BFh
B0h	P3 1111 1111							IPH XX00 0000	B7h
A8h	IE 0X00 0000	SADDR 0000 0000							AFh
A0h			AUXR1 XXXX0XX0						A7h
98h	SCON 0000 0000	SBUF XXXX XXXX							9Fh
90h	P1 1111 1111								97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XXXXXX00	CKCON XXXX XXX0	8Fh
80h		SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

reserved

5. T8xC5101/02Pin Configuration



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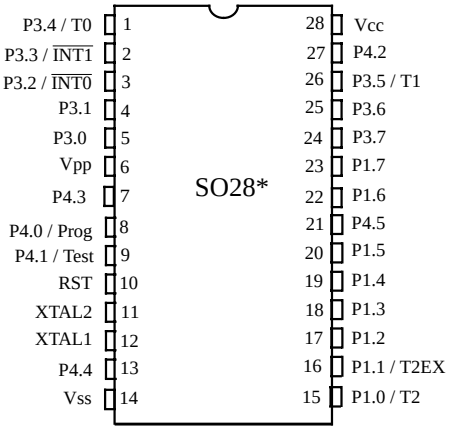

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Table 2. Pin Description for 24 and 28 pin packages

MNEMONIC	PIN NUMBER		TYPE	NAME AND FUNCTION
	24 pins	28 pins		
V_{SS}	12	14	I	**Ground:** 0V reference
V_{CC}	24	28	I	**Power Supply:** This is the power supply voltage for normal, idle and power-down operation
P1.0-P1.7	13-20	15-20 22-23	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. Port 1 also receives the low-order address byte during memory programming and verification. Alternate functions for Port 1 include:
			I/O	**T2 (P1.0):** Timer/Counter 2 external count input/Clockout
			I	**T2EX (P1.1):** Timer/Counter 2 Reload/Capture/Direction Control
P4.0 (Prog)- P4.1 (Test)	7 8	8 9	O (I) O (I)	**Port 4 bits 0 & 1**: Except during programming and verifying, these two bits are output port driving 30 micro Amps at high level and sinking 10 mA at low level (Vol < 1V). If they have 1s written to them, they output a high level and if they have 0 written to them, they output a low level. These 2 pins cannot be used as inputs. **Users should take care to never externally drive these pins low, especially during reset**. These two pins are primarily designed to drive LEDs. During programming and verifying, these two pins are used as input, as explained in the corresponding chapter. A Read or a Read/Modify/Write instruction to these bits will read the status of the output: 1 if the output is 1, 0 if the output is 0.
P4.2-P4.5	NA	27 7 13 21	I/O	**Port 4 bits 2 to 5:** bidirectional I/O port with internal pull-ups. Port 4.2 to 4.5 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 4.2 to 4.5 pins that are externally pulled low will source current because of the internal pull-ups.
P3.0-P3.7	5-1 23-21	5-1 26-24	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Port 3 also serves the special features of the 80C51 family, as listed below.
	5	5	I	**RxD (P3.0): Serial input port**
	4	4	O	**TxD (P3.1): Serial output port**
	3	3	I	**$\overline{\text{INT0}}$ (P3.2):** External interrupt 0
	2	2	I	**$\overline{\text{INT1}}$ (P3.3):** External interrupt 1
	1	1	I	**T0 (P3.4):** Timer 0 external input
	23	26	I	**T1 (P3.5):** Timer 1 external input
	22	25	I/O	**No alternate function on this pin**
	21	24	I/O	**No alternate function on this pin**
Reset	9	10	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to $V_{CC.}$
V_{PP}	6	6	I	**Programming Supply Voltage:** This pin receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming. **During normal operation, Vpp pin must be tied to Vcc.**
XTAL1	11	12	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	10	11	O	**Crystal 2:** Output from the inverting oscillator amplifier

6. Low Pin Count specificities

The T8xC5101/02 family is not able to perform any external memory access, such as a code fetch, a look-up table access (using MOVC) or a data access (using MOVX) because traditional Port 0 and Port 2 are not implemented anymore. It should be noted that 2 bits of a new port 4 are available, but they are pure user outputs. On the 28 pin package, there is also a set of 4 extra I/Os, which cannot be used for external access.

This inability to perform external memory accesses has the following consequences:

- Port 0 SFR doesn't exist any more
- Port 2 SFR doesn't exist any more
- Port 4 has six bits defined among which two are pure outputs for LED driving.
- Security level 4 is no longer applicable
- Code memory addresses is limited to 4000h. Accessing to any address above 3FFFh will return indeterminate value. Jumps, subroutine Calls, MOVC instructions should be limited to a maximum address range of 3FFFh to avoid any error.
- External data memory addresses is limited to 100h. Writing to any address above FFh will have no effect. Reading any address above FFh will return indeterminate value. To avoid any mistake, MOVX address should be limited to a maximum address range of FFh.
- In Rx devices, the user could disable the XRAM (for example, if he had shared resource at the corresponding address range). As no external access is possible with the T83/87C510x, it makes no sense to be able to disable accesses to XRAM. Nevertheless, access to AUXR bit 1 will cause no error and any write to this bit will have no effect.
- As there is no external access, EA, ALE, PSEN, RD and WR signals are not implemented. So, the corresponding pins or alternate functions are removed.
- As there is no ALE, there is no need for ALE disabling. Nevertheless, access to AUXR bit 0 will cause no error and any write to this bit will have no effect.
- Compared to the corresponding 16 Kbyte Rx2 device, the TS80C51RB2, the following features are removed:
  - Port 0 & 2
  - PCA
  - Watchdog
  - ONCE mode
  - Power Off Flag (POF)

7. T8xC5101/02 Enhanced Features

In comparison to the original 80C52, the T8xC5101/02 implements some new features, which are:

- The X2 option.
- The Dual Data Pointer.
- The extended RAM.
- The 4 level interrupt priority system.
- Some enhanced features are also located in the UART and the timer 2.

7.1 X2 Feature

The T8xC5101/02 core needs only 6 clock periods per machine cycle. This feature called "X2" provides the following advantages:

- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power.
- Save power consumption while keeping same CPU power (oscillator power saving).
- Save power consumption by dividing dynamically operating frequency by 2 in operating and idle modes.
- Increase CPU power by 2 while keeping same crystal frequency.

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

7.1.1 Description

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 1. shows the clock generation block diagram. X2 bit is validated on XTAL1÷2 rising edge to avoid glitches when switching from X2 to STD mode. Figure 2. shows the mode switching waveforms.

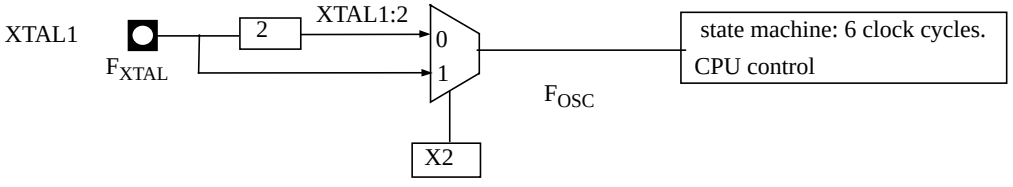


Figure 1. Clock Generation Diagram

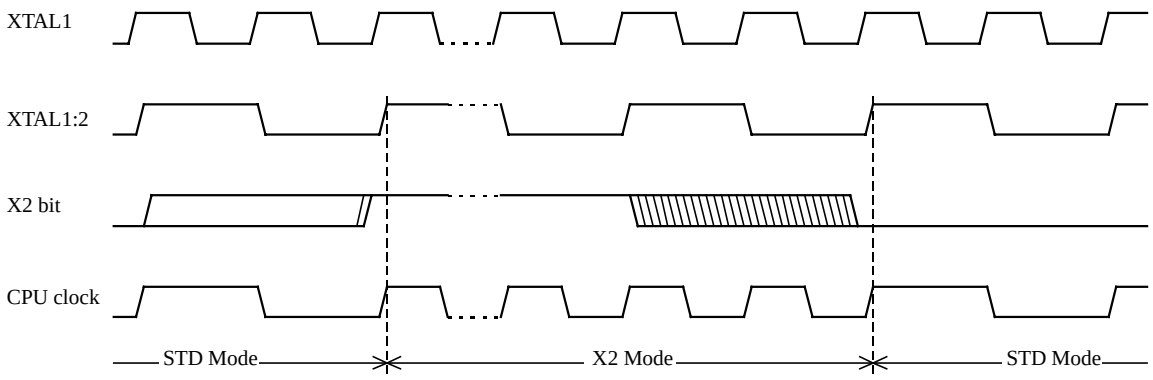


Figure 2. Mode Switching Waveforms

The X2 bit in the CKCON register (See Table 3.) allows to switch from 12 clock cycles per instruction to 6 clock cycles and vice versa. At reset, the standard speed is activated (STD mode). Setting this bit activates the X2 feature (X2 mode).

CAUTION

In order to prevent any incorrect operation while operating in X2 mode, user must be aware that all peripherals using clock frequency as time reference (UART, timers, PCA...) will have their time reference divided by two. For example a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms. UART with 4800 baud rate will have 9600 baud rate.

For further details on the X2 feature, please refer to ANM072 available on the web (http://www.temic-semi.com)

Table 3. CKCON Register

CKCON - Clock Control Register (8Fh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	X2

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	X2	**CPU and peripheral clock bit** Clear to select 12 clock periods per machine cycle (STD mode, $F_{OSC}=F_{XTAL}/2$). Set to select 6 clock periods per machine cycle (X2 mode, $F_{OSC}=F_{XTAL}$).

Reset Value = XXXX XXX0b
Not bit addressable

7.2 Dual Data Pointer Register Ddptr

The additional data pointer can be used to speed up code execution and reduce code size in a number of ways.

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1/bit0 (See Table 4.) that allows the program code to switch between them (Refer to Figure 3).

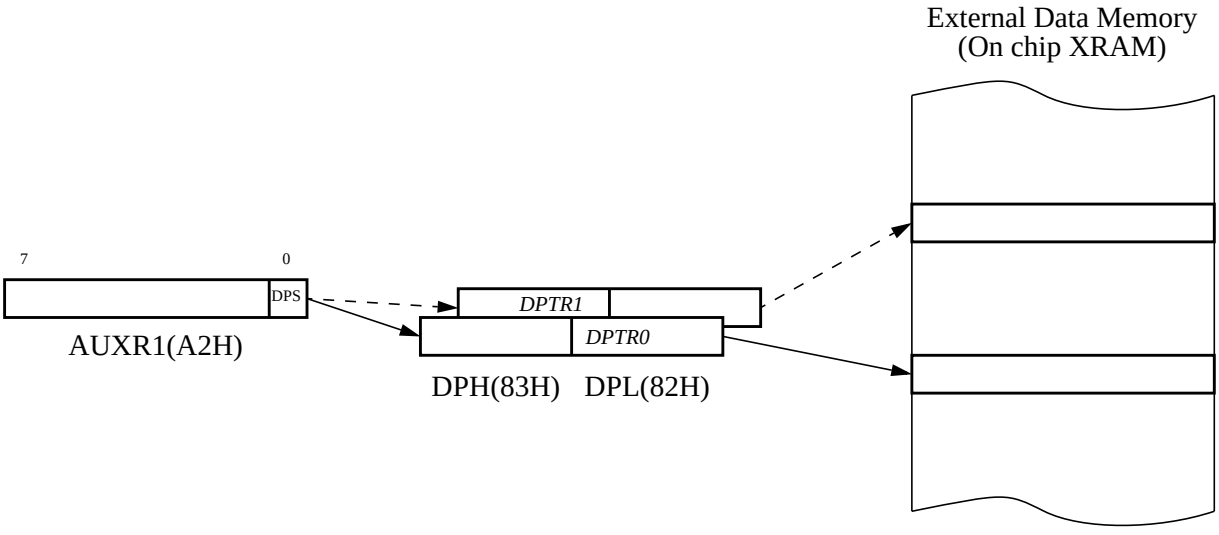


Figure 3. Use of Dual Pointer

Table 4. AUXR1: Auxiliary Register 1

AUXR1 Address 0A2H	-	-	-	-	GF3	0	-	DPS
Reset value	X	X	X	X	0	0	X	0

Symbol	Function	
-	Not implemented, reserved for future use.[a]	
DPS	Data Pointer Selection.	
	DPS	**Operating Mode**
	0	DPTR0 Selected
	1	DPTR1 Selected
GF3	This bit is a general purpose user flag[b].	

a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new feature. In that case, the reset value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.
b. GF3 will not be available on first version of the RC devices.

Application

Software can take advantage of the additional data pointers to both increase speed and reduce code size, for example, block operations (copy, compare, search ...) are well served by using one data pointer as a ’source’ pointer and the other one as a "destination" pointer.

ASSEMBLY LANGUAGE

```
; Block move using dual data pointers
; Destroys DPTR0, DPTR1, A and PSW
; note: DPS exits opposite of entry state
; unless an extra INC AUXR1 is added
;
00A2          AUXR1 EQU 0A2H
;
0000 909000MOV DPTR,#SOURCE       ; address of SOURCE
0003 05A2   INC   AUXR1           ; switch data pointers
0005 90A000 MOV DPTR,#DEST        ; address of DEST
0008          LOOP:
0008 05A2   INC   AUXR1           ; switch data pointers
000A E0       MOVX A,@DPTR        ; get a byte from SOURCE
000B A3       INC   DPTR          ; increment SOURCE address
000C 05A2   INC   AUXR1           ; switch data pointers
000E F0       MOVX @DPTR,A        ; write the byte to DEST
000F A3       INC   DPTR          ; increment DEST address
0010 70F6   JNZ   LOOP            ; check for 0 terminator
0012 05A2   INC   AUXR1           ; (optional) restore DPS
```

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.

7.3 Expanded RAM (XRAM)

The T8xC5101/02 provide 256 additional Bytes of random access memory (RAM) space for increased data parameter handling and high level language usage.

The T8xC5101/02 have internal data memory that is mapped into four separate segments.

The four segments are:

- 1. The Lower 128 bytes of RAM (addresses 00H to 7FH) are directly and indirectly addressable.
- 2. The Upper 128 bytes of RAM (addresses 80H to FFH) are indirectly addressable only.
- 3. The Special Function Registers, SFRs, (addresses 80H to FFH) are directly addressable only.
- 4. The expanded RAM bytes are indirectly accessed by MOVX instructions.

As external accesses are not possible on the T8xC5101/02 family, it makes no sense to have the possibility to disable accesses to XRAM. That's why, compared to TS80C51RB2, writing a 1 in AUXR register bit 1 will have no effect, and won't disable access to the XRAM.

The Lower 128 bytes can be accessed by either direct or indirect addressing. The Upper 128 bytes can be accessed by indirect addressing only. The Upper 128 bytes occupy the same address space as the SFR. That means they have the same address, but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the CPU knows whether the access is to the upper 128 bytes of data RAM or to SFR space by the addressing mode used in the instruction.

- Instructions that use direct addressing access SFR space. **For example: MOV 0A0H, # data**, accesses the SFR at location 0B0H (which is P3).
- Instructions that use indirect addressing access the Upper 128 bytes of data RAM. **For example: MOV @R0, # data** where R0 contains 0B0H, accesses the data byte at address 0B0H, rather than P3 (which address is 0B0H).
- The 256 XRAM bytes can be accessed by indirect addressing, with MOVX instructions. This part of memory which is physically located on-chip, logically occupies the first 256 bytes of external data memory.
- The XRAM is indirectly addressed, using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. **An access to XRAM will not affect any ports**. A write to external data memory locations higher than FFH (i.e. 0100H to FFFFH) will have no effect. A read will return an indeterminate value.

The stack pointer (SP) may be located anywhere in the 256 bytes RAM (lower and upper RAM) internal data memory. The stack may not be located in the XRAM.

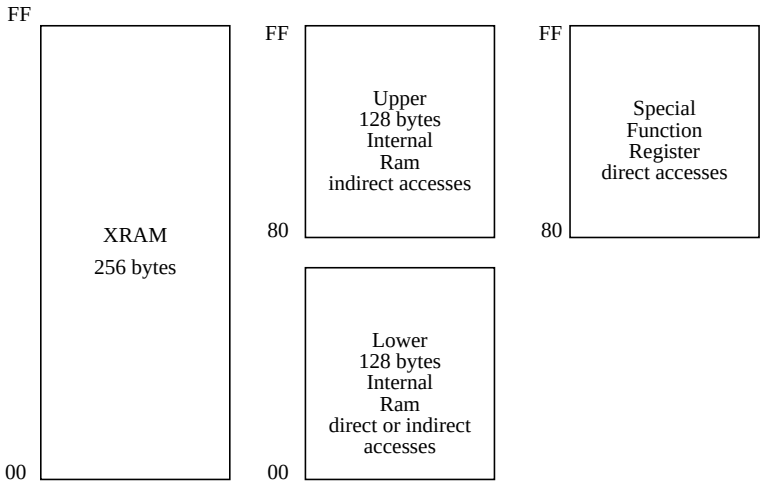


Figure 4. Internal and External Data Memory Address

Table 5. Auxiliary Register AUXR

AUXR Address 08EH	-	-	-	-	-	-	**EXTRAM**	**AO**
Reset value	X	X	X	X	X	X	0	0

Symbol	Function
-	Not implemented, reserved for future use.[a]
AO	Writing to this bit will have no effect (refer to chapter "Reduced EMI mode")
EXTRAM	Writing to this bit will have no effect

a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

7.4 Timer 2

The timer 2 in the T8xC5101/02 family is compatible with the timer 2 in the 80C52.
It is a 16-bit timer/counter: the count is maintained by two eight-bit timer registers, TH2 and TL2, connected in cascade. It is controlled by T2CON register (See Table 6) and T2MOD register (See Table 7). Timer 2 operation is similar to Timer 0 and Timer 1. C/$\overline{T2}$ selects $F_{OSC}/12$ (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows TL2 to be incremented by the selected input.

Timer 2 has 3 operating modes: capture, autoreload and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and CP/$\overline{RL2}$ (T2CON), as described in the TEMIC 8-bit Microcontroller Hardware description.

Refer to the TEMIC 8-bit Microcontroller Hardware description for the description of Capture and Baud Rate Generator Modes.

In T8xC5101/02 Timer 2 includes the following enhancements:

- Auto-reload mode with up or down counter
- Programmable clock-output

7.4.1 Auto-Reload Mode

The auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. If DCEN bit in T2MOD is cleared, timer 2 behaves as in 80C52 (refer to the TEMIC 8-bit Microcontroller Hardware description). If DCEN bit is set, timer 2 acts as an Up/down timer/counter as shown in Figure 5. In this mode the T2EX pin controls the direction of count.

When T2EX is high, timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when timer 2 overflows or underflows according to the the direction of the count. EXF2 does not generate any interrupt. This bit can be used to provide 17-bit resolution.

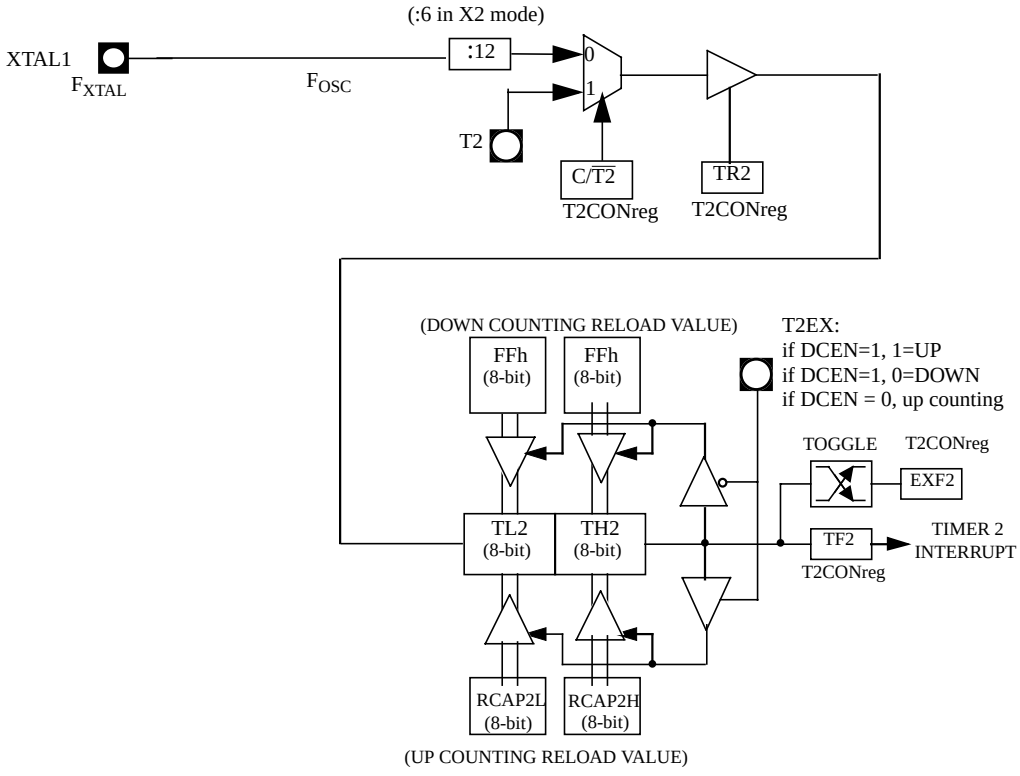


Figure 5. Auto-Reload Mode Up/Down Counter (DCEN = 1)

7.4.2 Programmable Clock-Output

In the clock-out mode, timer 2 operates as a 50%-duty-cycle, programmable clock generator (See Figure 6) . The input clock increments TL2 at frequency $F_{OSC}/2$. The timer repeatedly counts to overflow from a loaded value. At overflow, the contents of RCAP2H and RCAP2L registers are loaded into TH2 and TL2. In this mode, timer 2 overflows do not generate interrupts. The formula gives the clock-out frequency as a function of the system oscillator frequency and the value in the RCAP2H and RCAP2L registers :

$$Clock-OutFrequency = \frac{F_{osc} \times 2^{x2}}{4 \times (65536 - RCAP2H/RCAP2L)}$$

For a 16 MHz system clock, timer 2 has a programmable frequency range of 61 Hz ($F_{OSC}/2^{16)}$ to 4 MHz ($F_{OSC}/4$) in X1 mode. The generated clock signal is brought out to T2 pin (P1.0).

Timer 2 is programmed for the clock-out mode as follows:

- Set T2OE bit in T2MOD register.
- Clear C/$\overline{T2}$ bit in T2CON register.
- Determine the 16-bit reload value from the formula and enter it in RCAP2H/RCAP2L registers.
- Enter a 16-bit initial value in timer registers TH2/TL2. It can be the same as the reload value or a different one depending on the application.
- To start the timer, set TR2 run control bit in T2CON register.

It is possible to use timer 2 as a baud rate generator and a clock generator simultaneously. For this configuration, the baud rates and clock frequencies are not independent since both functions use the values in the RCAP2H and RCAP2L registers.

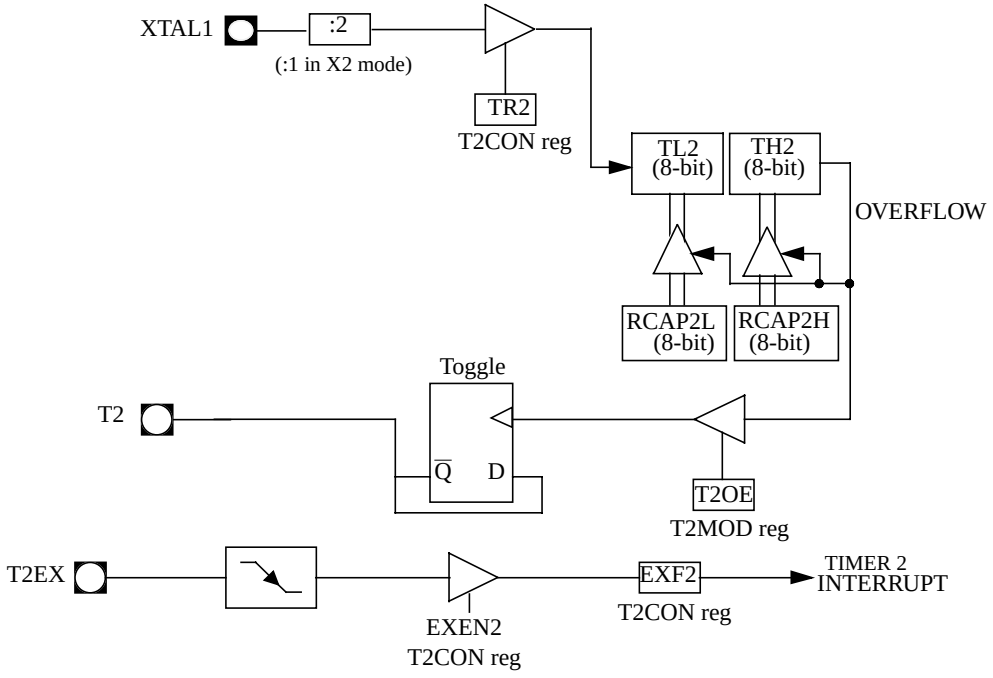


Figure 6. Clock-Out Mode C/$\overline{T2}$ = 0

Table 6. T2CON Register

T2CON - Timer 2 Control Register (C8h)

7	6	5	4	3	2	1	0
TF2	**EXF2**	**RCLK**	**TCLK**	**EXEN2**	**TR2**	**C/T2#**	**CP/RL2#**

Bit Number	Bit Mnemonic	Description
7	TF2	**Timer 2 overflow Flag** Must be cleared by software. Set by hardware on timer 2 overflow, if RCLK = 0 and TCLK = 0.
6	EXF2	**Timer 2 External Flag** Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. When set, causes the CPU to vector to timer 2 interrupt routine when timer 2 interrupt is enabled. Must be cleared by software. EXF2 doesn't cause an interrupt in Up/down counter mode (DCEN = 1)
5	RCLK	**Receive Clock bit** Clear to use timer 1 overflow as receive clock for serial port in mode 1 or 3. Set to use timer 2 overflow as receive clock for serial port in mode 1 or 3.
4	TCLK	**Transmit Clock bit** Clear to use timer 1 overflow as transmit clock for serial port in mode 1 or 3. Set to use timer 2 overflow as transmit clock for serial port in mode 1 or 3.
3	EXEN2	**Timer 2 External Enable bit** Clear to ignore events on T2EX pin for timer 2 operation. Set to cause a capture or reload when a negative transition on T2EX pin is detected, if timer 2 is not used to clock the serial port.
2	TR2	**Timer 2 Run control bit** Clear to turn off timer 2. Set to turn on timer 2.
1	C/T2#	**Timer/Counter 2 select bit** Clear for timer operation (input from internal clock system: F_{OSC}). Set for counter operation (input from T2 input pin, falling edge trigger). Must be 0 for clock out mode.
0	CP/RL2#	**Timer 2 Capture/Reload bit** If RCLK=1 or TCLK=1, CP/RL2# is ignored and timer is forced to auto-reload on timer 2 overflow. Clear to auto-reload on timer 2 overflows or negative transitions on T2EX pin if EXEN2=1. Set to capture on negative transitions on T2EX pin if EXEN2=1.

Reset Value = 0000 0000b
Bit addressable

Table 7. T2MOD Register

T2MOD - Timer 2 Mode Control Register (C9h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	T2OE	DCEN

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	T2OE	**Timer 2 Output Enable bit** Clear to program P1.0/T2 as clock input or I/O port. Set to program P1.0/T2 as clock output.
0	DCEN	**Down Counter Enable bit** Clear to disable timer 2 as up/down counter. Set to enable timer 2 as up/down counter.

Reset Value = XXXX XX00b
Not bit addressable

7.5 T8xC5101/02 Serial I/O Port

The serial I/O port in the T8xC5101/02 family is compatible with the serial I/O port in the 80C52. It provides both synchronous and asynchronous communication modes. It operates as an Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates.

Serial I/O port includes the following enhancements:

- Framing error detection
- Automatic address recognition

7.5.1 Framing Error Detection

Framing bit error detection is provided for the three asynchronous modes (modes 1, 2 and 3). To enable the framing bit error detection feature, set SMOD0 bit in PCON register (See Figure 7).

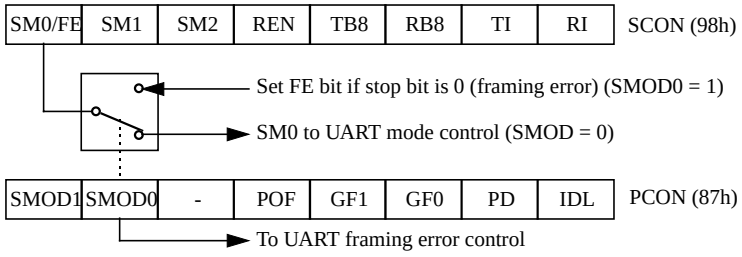


Figure 7. Framing Error Block Diagram

When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register (See Table 8.) bit is set.

Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 8. and Figure 9.).

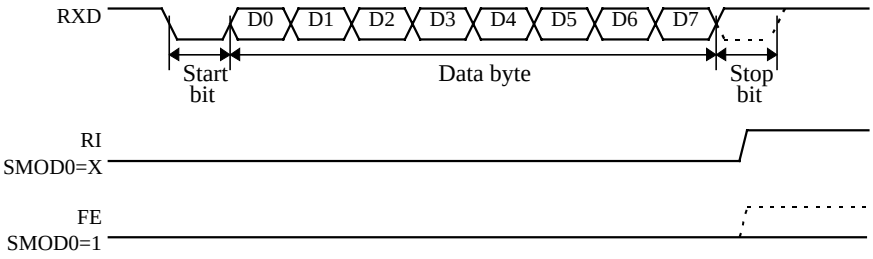


Figure 8. UART Timings in Mode 1

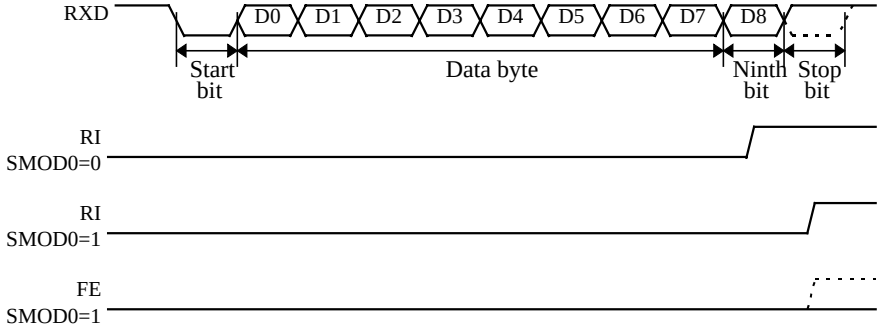


Figure 9. UART Timings in Modes 2 and 3

7.5.2 Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

NOTE: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).

7.5.3 Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed. To address a device by its individual address, the SADEN mask byte must be `1111 1111b`.
For example:

```
           SADDR      0101 0110b
           SADEN      1111 1100b
           Given      0101 01XXb
```

The following is an example of how to use given addresses to address different slaves:

```
Slave A:   SADDR      1111 0001b
           SADEN      1111 1010b
           Given      1111 0X0Xb

Slave B:   SADDR      1111 0011b
           SADEN      1111 1001b
           Given      1111 0XX1b

Slave C:   SADDR      1111 0010b
           SADEN      1111 1101b
           Given      1111 00X1b
```

The SADEN byte is selected so that each slave may be addressed separately.
For slave A, bit 0 (the LSB) is a don't-care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g. `1111 0000b`).
For slave A, bit 1 is a 1; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves B and C, but not slave A, the master must send an address with bits 0 and 1 both set (e.g. `1111 0011b`).
To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e.g. `1111 0001b`).

7.5.4 Broadcast Address

A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-care bits, e.g.:

```
           SADDR            0101 0110b
           SADEN            1111 1100b
Broadcast =SADDR OR SADEN   1111 111Xb
```

The use of don't-care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh. The following is an example of using broadcast addresses:

```
Slave A:   SADDR      1111 0001b
           SADEN      1111 1010b
           Broadcast  1111 1X11b,

Slave B:   SADDR      1111 0011b
           SADEN      1111 1001b
           Broadcast  1111 1X11B,

Slave C:   SADDR=     1111 0010b
           SADEN      1111 1101b
           Broadcast  1111 1111b
```

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send an address FFh. To communicate with slaves A and B, but not slave C, the master can send and address FBh.

7.5.5 Reset Addresses

On reset, the SADDR and SADEN registers are initialized to 00h, i.e. the given and broadcast addresses are XXXX XXXXb (all don't-care bits). This ensures that the serial port will reply to any address, and so, that it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.

SADEN - Slave Address Mask Register (B9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b
Not bit addressable

SADDR - Slave Address Register (A9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b
Not bit addressable

Table 8. SCON Register

SCON - Serial Control Register (98h)

7	6	5	4	3	2	1	0
FE/SM0	**SM1**	**SM2**	**REN**	**TB8**	**RB8**	**TI**	**RI**

Bit Number	Bit Mnemonic	Description
7	FE	**Framing Error bit (SMOD0=1)** Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected. SMOD0 must be set to enable access to the FE bit
	SM0	**Serial port Mode bit 0** Refer to SM1 for serial port mode selection. SMOD0 must be cleared to enable access to the SM0 bit
6	SM1	**Serial port Mode bit 1** SM1 SM0 Mode Description Baud Rate 0 0 0 Shift Register F_{XTAL}/12 (/6 in X2 mode) 0 1 1 8-bit UART Variable 1 0 2 9-bit UART F_{XTAL}/64 or F_{XTAL}/32 (/32, /16in X2 mode) 1 1 3 9-bit UART Variable
5	SM2	**Serial port Mode 2 bit / Multiprocessor Communication Enable bit** Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.
4	REN	**Reception Enable bit** Clear to disable serial reception. Set to enable serial reception.
3	TB8	**Transmitter Bit 8 / Ninth bit to transmit in modes 2 and 3.** Clear to transmit a logic 0 in the 9th bit. Set to transmit a logic 1 in the 9th bit.
2	RB8	**Receiver Bit 8 / Ninth bit received in modes 2 and 3** Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1. In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used.
1	TI	**Transmit Interrupt flag** Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.
0	RI	**Receive Interrupt flag** Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0, see Figure 8. and Figure 9. in the other modes.

Reset Value = 0000 0000b
Bit addressable

Table 9. PCON Register

PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	**SMOD0**	**-**	**POF**	**GF1**	**GF0**	**PD**	**IDL**

Bit Number	Bit Mnemonic	Description
7	SMOD1	**Serial port Mode bit 1** Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	**Serial port Mode bit 0** Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	POF	**Power-Off Flag** Clear to recognize next reset type. Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	**Power-Down mode bit** Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	**Idle mode bit** Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b
Not bit addressable

Power-off flag reset value will be 1 only after a power on (cold reset). A warm reset doesn't affect the value of this bit.

7.6 Interrupt System

The T8xC5101/02 family has a total of 6 interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (timers 0, 1 and 2) and the serial port interrupt. These interrupts are shown in Figure 10. The addresses of the interrupt vectors are the same as in the standard C52.

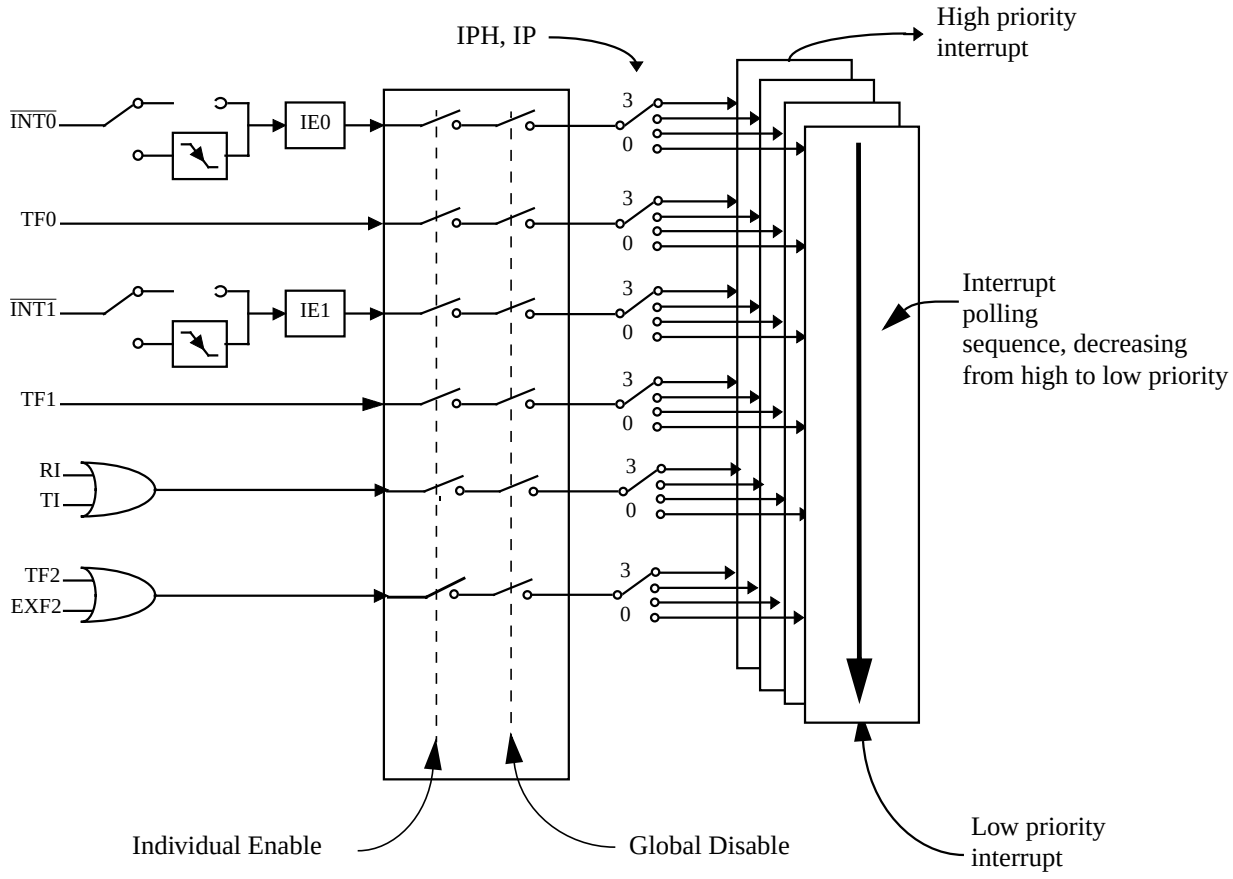


Figure 10. Interrupt Control System

Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 11.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 12.) and in the Interrupt Priority High register (See Table 13.). shows the bit values and priority levels associated with each combination.

Table 10. Priority Level Bit Values

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

Table 11. IE Register

IE - Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	**-**	**ET2**	**ES**	**ET1**	**EX1**	**ET0**	**EX0**

Bit Number	Bit Mnemonic	Description
7	EA	**Enable All interrupt bit** Clear to disable all interrupts. Set to enable all interrupts. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its own interrupt enable bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	ET2	**Timer 2 overflow interrupt Enable bit** Clear to disable timer 2 overflow interrupt. Set to enable timer 2 overflow interrupt.
4	ES	**Serial port Enable bit** Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	**Timer 1 overflow interrupt Enable bit** Clear to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.
2	EX1	**External interrupt 1 Enable bit** Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	**Timer 0 overflow interrupt Enable bit** Clear to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.
0	EX0	**External interrupt 0 Enable bit** Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0X00 0000b
Bit addressable

Table 12. IP Register

IP - Interrupt Priority Register (B8h)

7	6	5	4	3	2	1	0
-	-	PT2	PS	PT1	PX1	PT0	PX0

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	PT2	**Timer 2 overflow interrupt Priority bit** Refer to PT2H for priority level.
4	PS	**Serial port Priority bit** Refer to PSH for priority level.
3	PT1	**Timer 1 overflow interrupt Priority bit** Refer to PT1H for priority level.
2	PX1	**External interrupt 1 Priority bit** Refer to PX1H for priority level.
1	PT0	**Timer 0 overflow interrupt Priority bit** Refer to PT0H for priority level.
0	PX0	**External interrupt 0 Priority bit** Refer to PX0H for priority level.

Reset Value = XX00 0000b
Bit addressable

Table 13. IPH Register

IPH - Interrupt Priority High Register (B7h)

7	6	5	4	3	2	1	0
-	-	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	PT2H	**Timer 2 overflow interrupt Priority High bit** PT2H PT2 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
4	PSH	**Serial port Priority High bit** PSH PS Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
3	PT1H	**Timer 1 overflow interrupt Priority High bit** PT1H PT1 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
2	PX1H	**External interrupt 1 Priority High bit** PX1H PX1 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
1	PT0H	**Timer 0 overflow interrupt Priority High bit** PT0H PT0 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
0	PX0H	**External interrupt 0 Priority High bit** PX0H PX0 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest

Reset Value = XX00 0000b
Not bit addressable

7.7 Idle mode

An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirely : the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits GF0 and GF1 can be used to give an indication if an interrupt occured during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

7.8 Power-Down Mode

To save maximum power, a power-down mode can be invoked by software (Refer to Table 9., PCON register).

In power-down mode, the oscillator is stopped and the instruction that invoked power-down mode is the last instruction executed. The internal RAM and SFRs retain their value until the power-down mode is terminated. V_{CC} can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from power-down. To properly terminate power-down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

Only external interrupts $\overline{INT0}$ and $\overline{INT1}$ are useful to exit from power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input.
Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 11. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and power down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed.
Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put T8xC5101/02 into power-down mode.

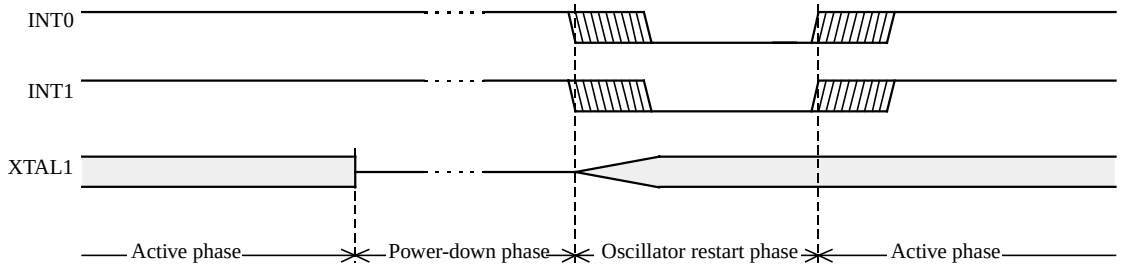


Figure 11. Power-Down Exit Waveform

Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does no affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content.
NOTE: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.

Table 14. The state of ports during idle and power-down modes

Mode	Program Memory	PORT1	PORT3	PORT4
Idle	Internal	Port Data	Port Data	Port Data
Power Down	Internal	Port Data	Port Data	Port Data

7.9 Reduced EMI mode

As there is no Port 0 nor Port 2 outputted from this device, there is no need to output ALE. EMI are then reduced intrinsically.

The bit which controls ALE disabling in Rx devices is A0 (bit 0) in register AUXR. As explained earlier for bit EXTRAM, writing any value to AO will have no effect on the device behavior.

Table 15. AUXR Register

AUXR - Auxiliary Register (8Eh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	**EXTRAM**	**AO**

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	EXTRAM	**EXTRAM bit** Writing to this bit will have no effect. The value read from this bit is indeterminate.
0	AO	**ALE Output bit** Writing to this bit will have no effect. The value read from this bit is indeterminate.

Reset Value = XXXX XX00b
Not bit addressable

8. T83C5101/02 ROM

8.1 ROM Structure

The T83C5101/02 ROM memory is divided in three different arrays:

- the code array
  - T83C5101: . . . . . 16 Kbytes.
  - T83C5102: . . . . . 8 Kbytes.
- the encryption array: . . . . . 64 bytes.
- the signature array: . . . . . 4 bytes.

8.2 ROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

8.2.1 Encryption Array

Within the ROM array are 64 bytes of encryption array. Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values.

8.2.2 Program Lock Bits

The lock bits when programmed according to Table 16. will provide different level of protection for the on-chip code and data.

Table 16. Program Lock bits

Program Lock Bits				Protection description
Security level	**LB1**	**LB2**	**LB3**	
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed.
2	P	U	U	Not applicable as usually this protection deals with executing MOVC from external memory (impossible) and sampling EA pin (doesn't exist any more)
3	U	P	U	Verify disable. This security level is available because ROM integrity will be verified thanks to another method.

U: unprogrammed
P: programmed

8.2.3 Signature bytes

The T8xC5101/02 family contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in sections 9.3.2 and 9.5.1.

8.2.4 Verify Algorithm

Refer to section Table 9.3.5

9. T87C5101 EPROM

9.1 EPROM Structure

The T87C5101 EPROM is divided into two different arrays:

- the code array: . . . . . 16 Kbytes.
- the encryption array: . . . . . 64 bytes.

In addition a third non programmable array is implemented:

- the signature array: . . . . . 4 bytes.

9.2 EPROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

9.2.1 Encryption Array

Within the EPROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values.

9.2.2 Program Lock Bits

The three lock bits, when programmed according to Table 17., will provide different level of protection for the on-chip code and data.

Table 17. Program Lock bits

Program Lock Bits				Protection description
Security level	**LB1**	**LB2**	**LB3**	
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed.
2	P	U	U	Further programming of the program memory is disabled.
3	U	P	U	Same as security level 2 + verify disabled.
4	U	U	P	Not applicable as usually this protection deals with external execution, which is impossible with this device.

U: unprogrammed,
P: programmed

WARNING: Security level 2 and higher should only be programmed after EPROM verification.

9.2.3 Signature bytes

The T8xC5101/02 family contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 9.3.2 and 9.5.1.

9.3 EPROM Programming

9.3.1 Set-up modes

In order to program and verify the EPROM or to read the signature bytes, the T87C5101 is placed in specific test modes (See Figure 12.).

Control and program signals must be held at the levels indicated in Table 18.

9.3.2 Definition of terms

Address and Control Lines: RST, $\overline{\text{TEST}}$, Port 3

Data Lines: Port 1

Program Signals: Vpp, $\overline{\text{PROG}}$

Table 18. EPROM Set-Up Modes

Mode	RST	$\overline{\text{TEST}}$	$\overline{\text{PROG}}$	VPP	P3.7	P3.6	P3.3	P3.2	P3.1
Program Code data	1	0/1	⊔	0/ 12.75V	1	1	1	1	0
Verify Code data	1	0/1	1	0/1	1	1	0	0	0
Program Encryption Array Address 0-3Fh	1	0/1	⊔	0/ 12.75V	1	0	1	1	0
Read Signature Bytes	1	0	1	0	0	0	0	0	0
Program Lock bit 1	1	0/1	⊔	0/ 12.75V	1	1	1	1	1
Program Lock bit 2	1	0/1	⊔	0/ 12.75V	0	0	1	1	1
Program Lock bit 3	NA	NA	NA	NA	NA	NA	NA	NA	NA
Read lock bits	1	0	1	0	1	0	0	0	0

NA: not applicable

TCODE = Test code, ADH = address high, ADL = address low

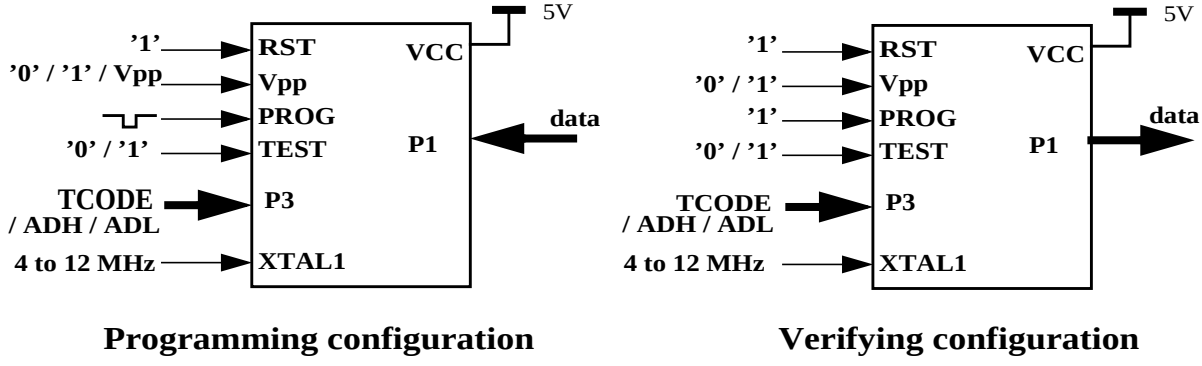


Figure 12. Programming and Verifying Modes Configuration

9.3.3 EPROM Programming and Verification Characteristics

T_A = 21°C to 27°C; V_{SS} = 0V; V_{CC} = 5V ± 10% while programming. V_{CC} = operating range while verifying

Table 19. EPROM Programming Parameters

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13	V
I_{PP}	Programming Supply Current		75	mA
$1/T_{CLCL}$	Oscillator Frequency	4	12	MHz

9.3.4 Programming Algorithm

- step 1: Vpp and TEST low, present T code for programming on P3 and raise Vpp to 12.75V
- step 2: present Address High on P3 and pulse TEST high
- step 3: present address Low on P3 and data on P1
- step 4: pulse PROG low
- step 5: back to step 3 if the next byte to program is in the same 256 byte page

OR

- step 5: back to step 2 if the next byte to program is in a different page

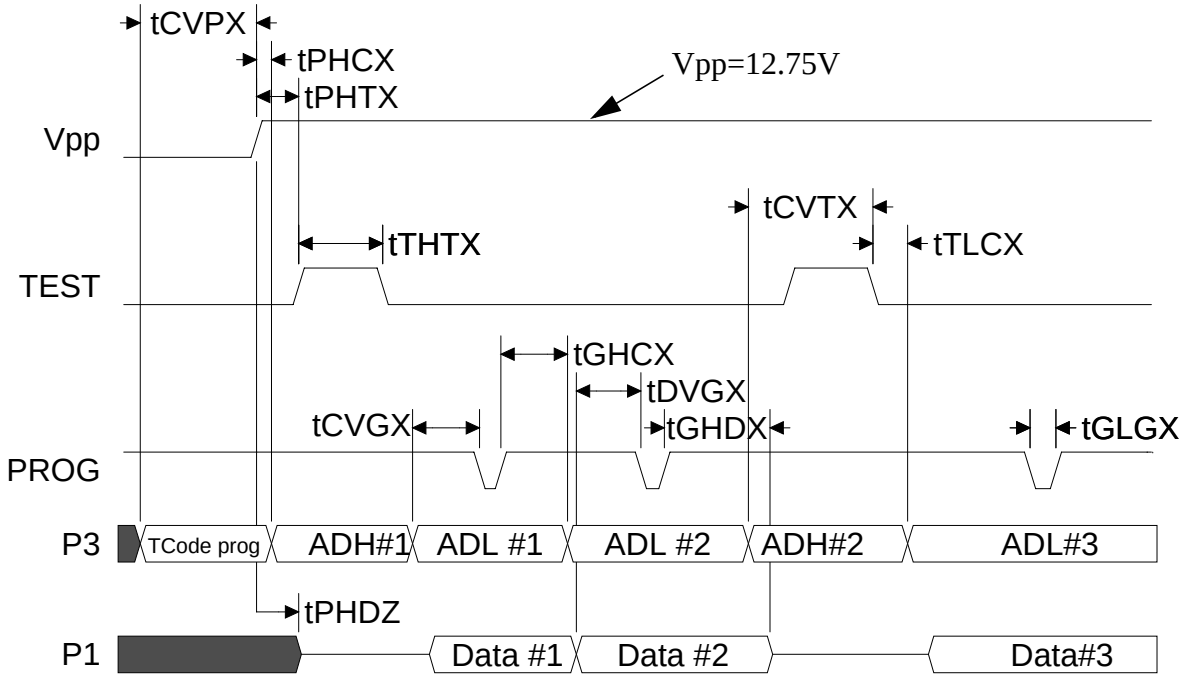


Figure 13. Programming signals'waveform

			12 MHz		
Symbol	**Parameter**	**Formula**	**Min**	**Max**	**Unit**
tOSC	Oscillator period	-		83.3	ns
tCVPX	Code input Valid to Vpp rising edge setup time	36 tOSC	3		µs
tPHCX	Code input valid from Vpp High hold time	1 tOSC	83.3		ns
tPHTX	Test input valid from Vpp High hold time	1 tOSC	83.3		ns
tTHTX	Test High pulse width	36 tOSC	3		µs
tCVTX	Address high Valid to Test falling edge setup time	36 tOSC	3		µs
tTLCX	Address input Valid from Test falling edge hold time	1 tOSC	83.3		ns
tPHDZ	Data output Hi-Z from Vpp high delay			0	
tGLGX	Prog Low pulse width		90	110	µs
tCVGX	Address valid to Prog falling edge setup time	36 tOSC	3		µs
tDVGX	Data input Valid to Prog falling edge setup time	36 tOSC	3		µs
tGHCX	Address valid from Prog rising edge hold time	1 tOSC	83.3		ns
tGHDX	Data input valid from Prog rising edge hold time	1 tOSC	83.3		ns

9.3.5 Verifying algorithm

- step 1: Vpp and TEST low, present T code for verification on P3 and Raise Vpp to Vcc
- step 2: present address High and pulse TEST high
- step 3: present address Low on P3 and read data on P1
- step 4: back to step 3 if the next byte is in the same 256 byte page

OR

- step 4: back to step 2 if the next byte to program is in a different page

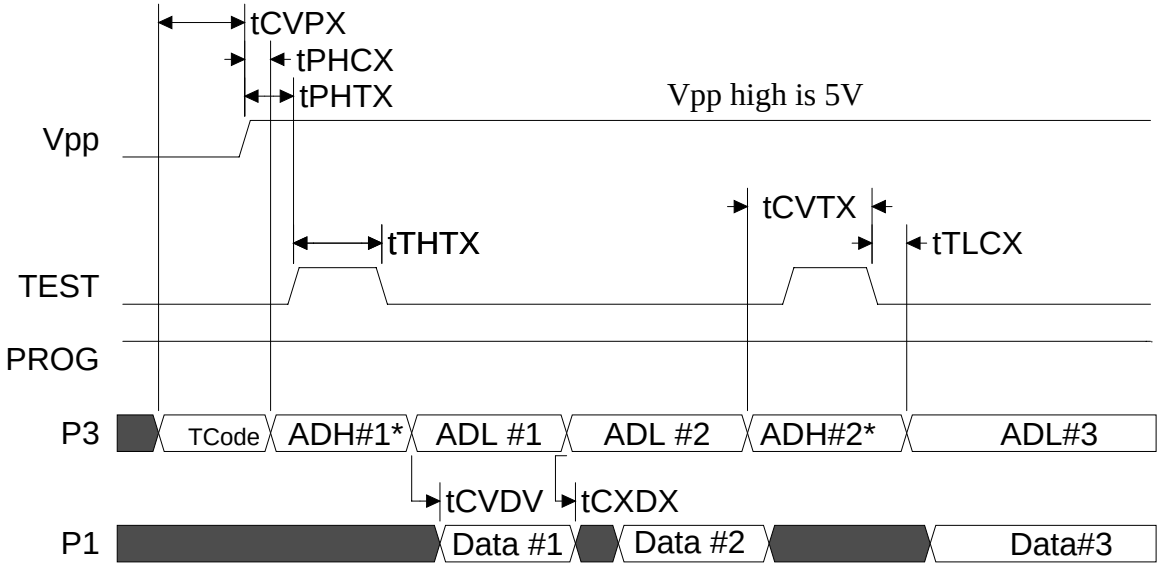


Figure 14. Verifying signals'waveform

**** ADH is egal to 0 when addressing signature bytes***

			12 MHz		
Symbol	**Parameter**	**Formula**	**Min**	**Max**	**Unit**
tOSC	Oscillator period			83.3	ns
tCVPX	Code input Valid to Vpp rising edge setup time	36 tOSC	3		µs
tPHCX	Code input valid from Vpp High hold time	1 tOSC	83.3		ns
tPHTX	Test input valid from Vpp High hold time	1 tOSC	83.3		ns
tTHTX	Test High pulse width	36 tOSC	3		µs
tCVTX	Address high Valid to Test falling edge setup time	36 tOSC	3		µs
tTLCX	Address input Valid from Test falling edge hold time	1 tOSC	83.3		ns
tCVDV	Address Valid to Data output Valid delay	36 tOSC		3	µs
tCXDX	Data valid from Address Invalid hold time		0		

9.3.6 Programming / Verify Algorithm

- step 1: Vpp and TEST low, present T code for programming on P3 and raise Vpp to 12.75V
- step 2: present Address High on P3 and pulse TEST high
- step 3: present address Low on P3 and data on P1
- step 4: pulse PROG low
- step 5: present T code for verifying on P3 and lower Vpp to 0V
- step 6: read previous data
- step 7: present T code for programming on P3 and raise Vpp to 12.75V
- step 8: goto step 3 if the next byte to program is in the same 256 byte page

OR

- step 8: goto step 2 if the next byte to program is in a different page

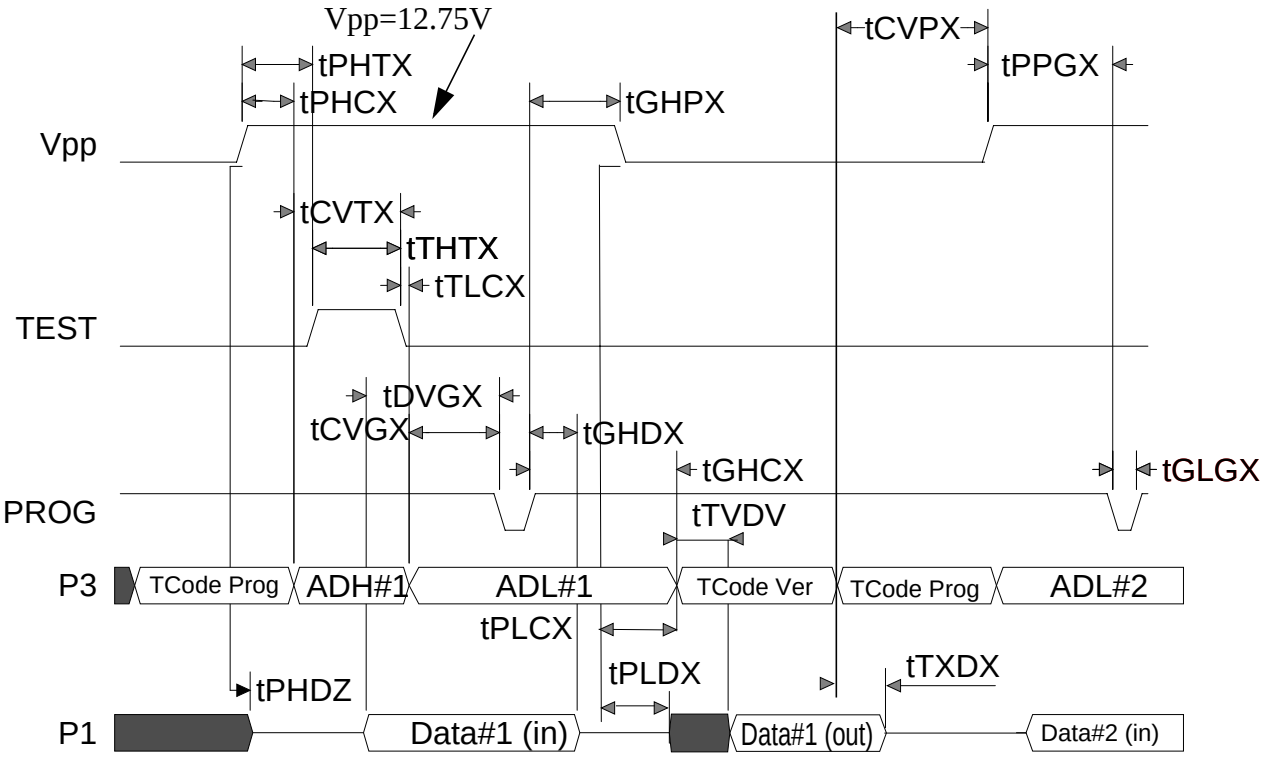


Figure 15. Programming / Verifying signals'waveform

Note: after programming, addresses high and low are already latched in the device, and when switching to verify, the device outputs directly the last written data.

			12 MHz		
Symbol	**Parameter**	**Formula**	**Min**	**Max**	**Unit**
tOSC	Oscillator period	-		83.3	ns
tCVPX	Code input Valid to Vpp rising edge setup time	36 tOSC	3		µs
tPHCX	Code input valid from Vpp High hold time	1 tOSC	83.3		ns
tPHTX	Test input valid from Vpp High hold time	1 tOSC	83.3		ns
tTHTX	Test High pulse width	36 tOSC	3		µs
tCVTX	Address high Valid to Test falling edge setup time	36 tOSC	3		µs
tTLCX	Address input Valid from Test falling edge hold time	1 tOSC	83.3		ns
tPHDZ	Data output Hi-Z from Vpp high delay			0	
tGLGX	Prog Low pulse width		90	110	µs
tCVGX	Address valid to Prog falling edge setup time	36 tOSC	3		µs
tDVGX	Data input Valid to Prog falling edge setup time	36 tOSC	3		µs
tGHCX	Address valid from Prog rising edge hold time	1 tOSC	83.3		ns
tGHDX	Data input valid from Prog High hold time	1 tOSC	83.3		ns
tGHPX	Vpp on Vpp pin from Prog High hold time	36 tOSC	3		µs
tTXDX	Data output valid from T code invalid hold time		0		
tTVDV	Data output valid from T code valid delay	36 tOSC		3	µs
tPLCX	Address valid from Vpp falling edge hold time	36 tOSC	3		µs
tPPGX	Vpp on Vpp pin to Prog falling edge setup time	36 tOSC	3		µs
tPLDX	Data output from Vpp Low delay		0		µs

9.3.7 Lock bits programmation and verification

9.3.7.1 Programmation :

- step 1: Vpp and TEST low, present T code for Lock bits programming on P3 and raise Vpp to 12.75V
- step 2: pulse PROG low

9.3.7.2 Verification :

- step 1 : Vpp and TEST low, present T code for Lock bits verification
- step 2 : read data

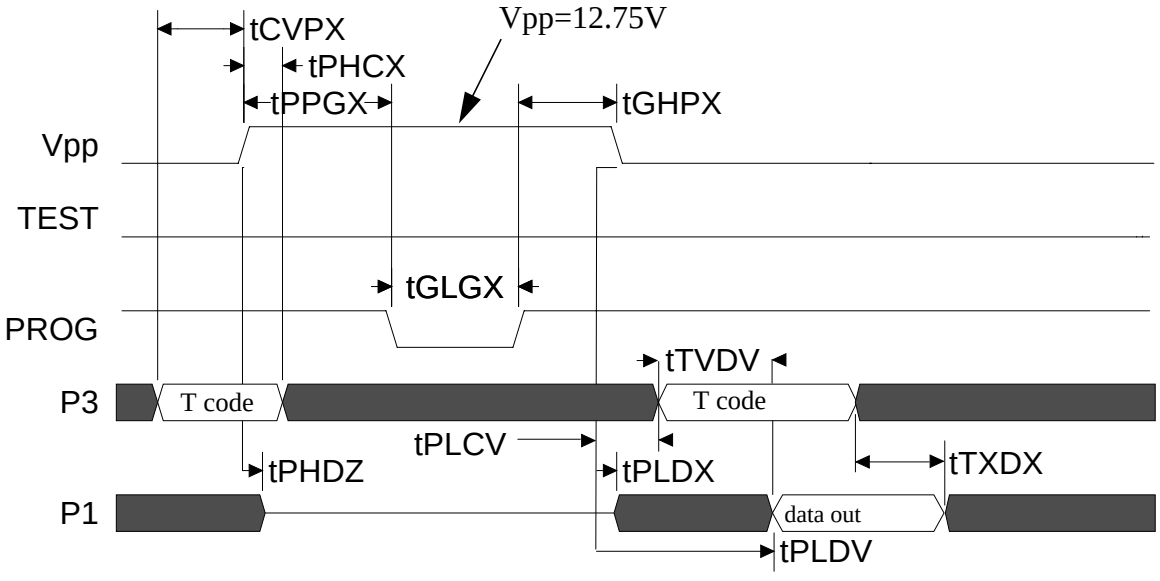


Figure 16. Lock bits programming signals'waveform and Lock bits verifying signals'waveform

			12 MHz		
Symbol	**Parameter**	**Formula**	**Min**	**Max**	**Unit**
tOSC	Oscillator period	-		83.3	ns
tCVPX	Code input valid to Vpp rising edge setup time	36 tOSC	3		µs
tPHCX	Code input valid from Vpp high hold time	1 tOSC	83.3		ns
tPPGX	Vpp on Vpp pin to PROG Low setup time	36 tOSC	3		µs
tGLGX	Prog Low pulse width		90	110	µs
tGHPX	Vpp on Vpp pin from PROG High hold time	36 tOSC	3		µs
tPLDV	Data Output Valid from Vpp Low delay	36 tOSC		3	µs
tPLDX	Data output from Vpp Low delay		0		
tTVDV	Data output valid from T code valid delay	36 tOSC		3	µs
tTXDX	Data output valid from T code invalid hold time		0		
tPHDZ	Data output Hi-Z from Vpp high delay			0	
tPLCV	Vpp low to T code valid setup time	36 tOSC	3		µs

•Vpp pin in driven :

-to 0V when P3 contains the test code

-to 5V when P3 contains high order or low order addresses

-to Vpp during programming cycled

•Test pin is driven :

-to 5V when P3 contains high order address

-to 0V in the other cases

9.4 EPROM Erasure (Windowed Packages Only)

Erasing the EPROM erases the code array, the encryption array and the lock bits returning the parts to full functionality.

Erasure leaves all the EPROM cells in a 1's state (FF).

9.4.1 Erasure Characteristics

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Å) to an integrated dose at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 µW/cm^2 rating for 30 minutes, at a distance of about 25 mm, should be sufficient. An exposure of 1 hour is recommended with most of standard erasers.

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Å. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

9.5 Signature Bytes

9.5.1 Signature bytes content

The T8xC5101/02 has four signature bytes in location 30h, 31h, 60h and 61h. To read these bytes follow the procedure for EPROM verify but activate the control lines provided in Table 18. for Read Signature Bytes. Table 20. shows the content of the signature byte for the T8xC5101/02.

Table 20. Signature Bytes Content

Location	Contents	Comment
30h	58h	Manufacturer Code: TEMIC SEMICONDUCTORS
31h	57h	Family Code: C51 X2
60h	3Bh	Product name: T83C5101/02 8K or 16K ROM version
60h	BBh	Product name: T87C5101 16K OTP version
61h	EFh	Product revision number : T8xC5101/02 Rev.0

10. Electrical Characteristics

10.1 Absolute Maximum Ratings (1)

Ambiant Temperature Under Bias:	
C = commercial	0°C to 70°C
I = industrial	-40°C to 85°C
Storage Temperature	-65°C to + 150°C
Voltage on V_{CC} to V_{SS}	-0.5 V to + 7 V
Voltage on V_{PP} to V_{SS}	-0.5 V to + 13 V
Voltage on Any Pin to V_{SS}	-0.5 V to V_{CC} + 0.5 V
Power Dissipation	1 W(2)

NOTES

1. Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

2. This value is based on the maximum allowable die temperature and the thermal resistance of the package.

10.2 Power consumption measurement

Since the introduction of the first C51 devices, every manufacturer made operating Icc measurements under reset, which made sense for the designs were the CPU was running under reset. In TEMIC new devices, the CPU is no more active during reset, so the power consumption is very low but is not really representative of what will happen in the customer system. That's why, while keeping measurements under Reset, TEMIC presents a new way to measure the operating Icc:

Using an internal test ROM, the following code is executed:

Label: SJMP Label (80 FE)

Ports 1, 3, 4 are disconnected, RST = Vss, XTAL2 is not connected and XTAL1 is driven by the clock.

This is much more representative of the real operating Icc.

10.3 DC Parameters for Standard Voltage

T_A = 0°C to +70°C; V_{SS} = 0 V; V_{CC} = 5 V ± 10%; F = 0 to 40 MHz.
T_A = -40°C to +85°C; V_{SS} = 0 V; V_{CC} = 5 V ± 10%; F = 0 to 40 MHz.

Table 21. DC Parameters in Standard Voltage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		0.2 V_{CC} - 0.1	V	
V_{IH}	Input High Voltage except XTAL1, RST	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage, XTAL1, RST	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage, ports 1, 3, 4.2-4.5 (6)			0.3 0.45 1.0	V V V	I_{OL} = 100 µA I_{OL} = 1.6 mA I_{OL} = 3.5 mA
V_{OL1}	Output Low Voltage, port 4.0-4.1 (6)		0.76(5)	 0.5 1.0	V V V	I_{OL} = 10.0 mA I_{OL} = 6.0 mA I_{OL} = 12.0 mA
V_{OH}	Output High Voltage, ports 1, 3, 4.2-4.5 (6)	V_{CC} - 0.3 V_{CC} - 0.7 V_{CC} - 1.5			V V V	I_{OH} = -10 µA I_{OH} = -30 µA I_{OH} = -60 µA V_{CC} = 5 V ± 10%
R_{RST}	RST Pulldown Resistor	50	90 (5)	200	kΩ	
I_{IL}	Logical 0 Input Current ports 1, 3 and 4			-50 TBD	µA	Vin = 0.45 V, port 1 & 3 Vin = 0.45 V, port 4
I_{LI}	Input Leakage Current			±10	µA	0.45 V < Vin < V_{CC}
I_{TL}	Logical 1 to 0 Transition Current, ports 1, 3			-650 TBD	µA	Vin = 2.0 V, port 1 & 3 Vin = 2.0 V, port 4
C_{IO}	Capacitance of I/O Buffer			10	pF	Fc = 1 MHz T_A = 25°C
I_{PD}	Power Down Current	to be confirmed	20 (5)	50	µA	2.0 V < V_{CC} < 5.5 V(3)
I_{CC} under RESET	Power Supply Current Maximum values, X1 mode: (7)		to be confirmed	1 + 0.4 Freq (MHz) @12MHz 5.8 @16MHz 7.4	mA	V_{CC} = 5.5 V(1)
I_{CC} operating	Power Supply Current Maximum values, X1 mode: (7)		to be confirmed	3 + 0.6 Freq (MHz) @12MHz 10.2 @16MHz 12.6	mA	V_{CC} = 5.5 V(8)
I_{CC} idle	Power Supply Current Maximum values, X1 mode: (7)		to be confirmed	0.25+0.3Freq (MHz) @12MHz 3.9 @16MHz 5.1	mA	V_{CC} = 5.5 V(2)

10.4 DC Parameters for Low Voltage

T_A = 0°C to +70°C; V_{SS} = 0 V; V_{CC} = 2.7 V to 5.5 V; F = 0 to 30 MHz.
T_A = -40°C to +85°C; V_{SS} = 0 V; V_{CC} = 2.7 V to 5.5 V; F = 0 to 30 MHz.

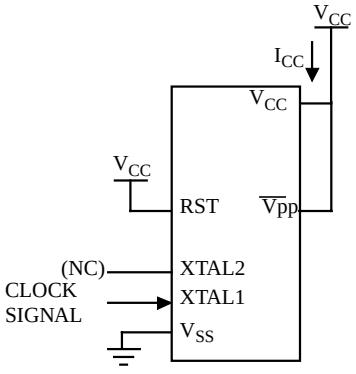
Table 22. DC Parameters for Low Voltage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		0.2 V_{CC} - 0.1	V	
V_{IH}	Input High Voltage except XTAL1, RST	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage, XTAL1, RST	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage, ports 1, 3, 4.2-4.5 (6)			0.45	V	I_{OL} = 0.8 mA
V_{OL1}	Output Low Voltage, port 4.0-4.1(6)		0.83(5)	0.5	V V	I_{OL} = 10.0 mA I_{OL} = 4.8 mA
V_{OH}	Output High Voltage, ports 1, 3, 4.2-4.5 (6)	0.9 V_{CC}			V	I_{OH} = -10 µA
I_{IL}	Logical 0 Input Current ports 1, 2 and 3			-50 TBD	µA	Vin = 0.45 V, port 1 & 3 Vin = 0.45 V, port 4
I_{LI}	Input Leakage Current			±10	µA	0.45 V < Vin < V_{CC}
I_{TL}	Logical 1 to 0 Transition Current, ports 1, 3			-650 TBD	µA	Vin = 2.0 V, port 1 & 3 Vin = 2.0 V, port 4
R_{RST}	RST Pulldown Resistor	50	90 (5)	200	kΩ	
CIO	Capacitance of I/O Buffer			10	pF	Fc = 1 MHz T_A = 25°C
I_{PD}	Power Down Current	to be confirmed	20 (5) 10 (5)	50 30	µA	V_{CC} = 2.0 V to 5.5 V(3) V_{CC} = 2.0 V to 3.3 V(3)
I_{CC} under RESET	Power Supply Current Maximum values, X1 mode: (7)		to be confirmed	1 + 0.2 Freq (MHz) @12MHz 3.4 @16MHz 4.2	mA	V_{CC} = 3.3 V(1)
I_{CC} operating	Power Supply Current Maximum values, X1 mode: (7)		to be confirmed	1 + 0.3 Freq (MHz) @12MHz 4.6 @16MHz 5.8	mA	V_{CC} = 3.3 V(8)
I_{CC} idle	Power Supply Current Maximum values, X1 mode: (7)		to be confirmed	0.15 Freq (MHz) + 0.2 @12MHz 2 @16MHz 2.6	mA	V_{CC} = 3.3 V(2)

NOTES

1. *I_{CC} under reset is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, T_{CHCL} = 5 ns (see Figure 21.), V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} - 0.5V; XTAL2 N.C.; Vpp = RST = V_{CC}. I_{CC} would be slightly higher if a crystal oscillator used.*
2. *Idle I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, T_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} - 0.5 V; XTAL2 N.C; Vpp = RST = V_{SS} (see Figure 19.).*
3. *Power Down I_{CC} is measured with all output pins disconnected; Vpp = V_{SS}; XTAL2 NC.; RST = V_{SS} (see Figure 20).*
4. *Not Applicable*
5. *Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.*

6. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 6 and 8-bit port:
Port 4.0 + 4.1: 20 mA
Port 4.2 to 4.5 : 8 mA
Ports 1 and 3: 15 mA
Maximum total I_{OL} for all output pins: 58 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
7. For other values, please contact your sales office.
8. Operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, T_{CHCL} = 5 ns (see Figure 21.), V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} - 0.5V; XTAL2 N.C.; Vpp= V_{CC}; RST = V_{SS}. The internal ROM runs the code 80 FE (label: SJMP label). I_{CC} would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.



All other pins are disconnected.

Figure 17. I_{CC} Test Condition, under reset

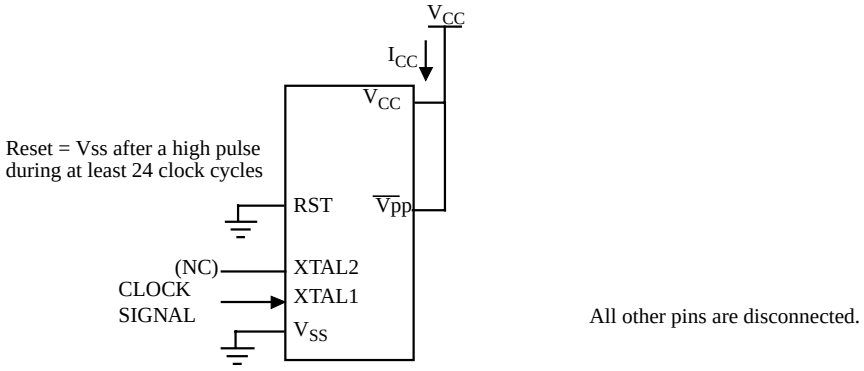


Figure 18. Operating I_{CC} Test Condition

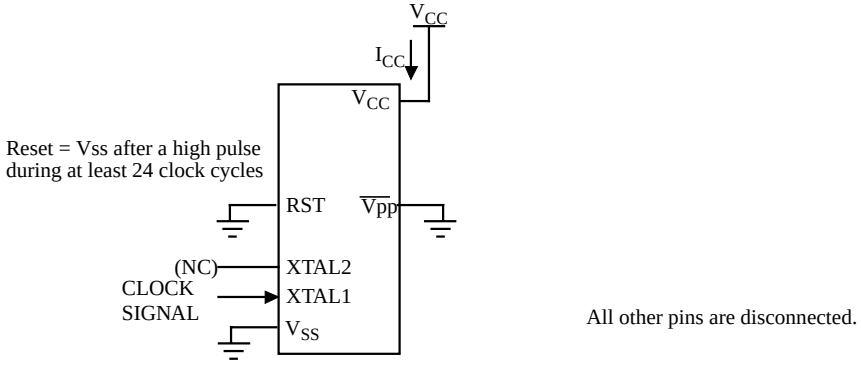


Figure 19. I_{CC} Test Condition, Idle Mode

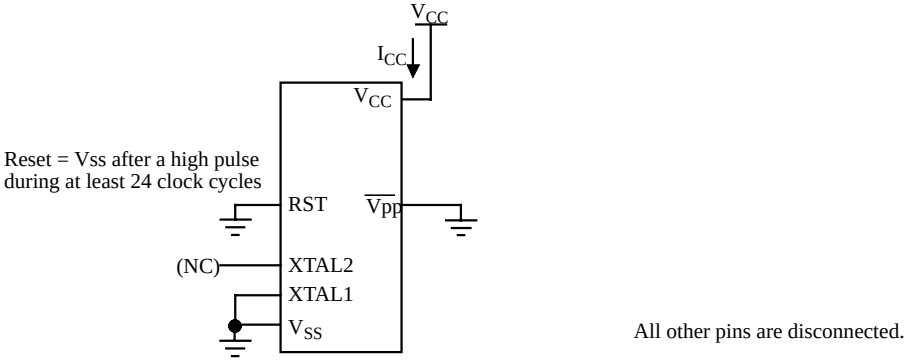


Figure 20. I_{CC} Test Condition, Power-Down Mode

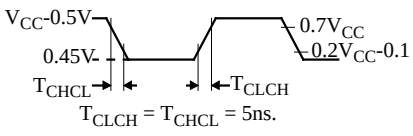


Figure 21. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes

10.5 AC Parameters

10.5.1 Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a “T” (stands for Time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example:T_{XHDV} = Time from clock rising edge to input data valid.

T_A = 0 to +70°C (commercial temperature range); V_{SS} = 0 V; V_{CC} = 5 V ± 10%; -V ranges.
T_A = 0 to +70°C (commercial temperature range); V_{SS} = 0 V; 2.7 V < V_{CC} < 5.5 V; -L range.
T_A = -40°C to +85°C (industrial temperature range); V_{SS} = 0 V; 2.7 V < V_{CC} < 5.5 V; -L range.

Table 23. gives the maximum applicable load capacitance for Port 1, 3 and 4. Timings will be guaranteed if these capacitances are respected. Higher capacitance values can be used, but timings will then be degraded.

Table 23. Load Capacitance versus speed range, in pF

	-V	-L
Port 1, 3 & 4	50	80

Table 25. gives the description of each AC symbols.

Table 26. gives for each range the AC parameter.

Table 27. gives the frequency derating formula of the AC parameter. To calculate each AC symbols, take the x value corresponding to the speed grade you need (-V or -L) and replace this value in the formula. Values of the frequency must be limited to the corresponding speed grade:

Table 24. Max frequency for derating formula regarding the speed grade

	-V X1 mode	-V X2 mode	-L X1 mode	-L X2 mode
Freq (MHz)	40	33	40	20
T (ns)	25	30	25	50

Example:
T_{XHDV} in X2 mode for a -V part at 20 MHz (T = $1/20^{E6}$ = 50 ns):
x= 133 (Table 27.)
T= 50ns
T_{XHDV}= 5T - x = 5 x 50 - 133 = 117ns

10.5.2 Serial Port Timing - Shift Register Mode

Table 25. Symbol Description

Symbol	Parameter
T_{XLXL}	Serial port clock cycle time
T_{QVHX}	Output data set-up to clock rising edge
T_{XHQX}	Output data hold after clock rising edge
T_{XHDX}	Input data hold after clock rising edge
T_{XHDV}	Clock rising edge to input data valid

Table 26. AC Parameters for a Fix Clock

Speed	-V X2 mode 33 MHz 66 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 40 MHz		Units
Symbol	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
T_{XLXL}	180		300		300		300		ns
T_{QVHX}	100		200		200		200		ns
T_{XHQX}	10		30		30		30		ns
T_{XHDX}	0		0		0		0		ns
T_{XHDV}		17		117		117		117	ns

Table 27. AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-V	-L	Units
T_{XLXL}	Min	12 T	6 T			ns
T_{QVHX}	Min	10 T - x	5 T - x	50	50	ns
T_{XHQX}	Min	2 T - x	T - x	20	20	ns
T_{XHDX}	Min	x	x	0	0	ns
T_{XHDV}	Max	10 T - x	5 T- x	133	133	ns

10.5.3 Shift Register Timing Waveforms

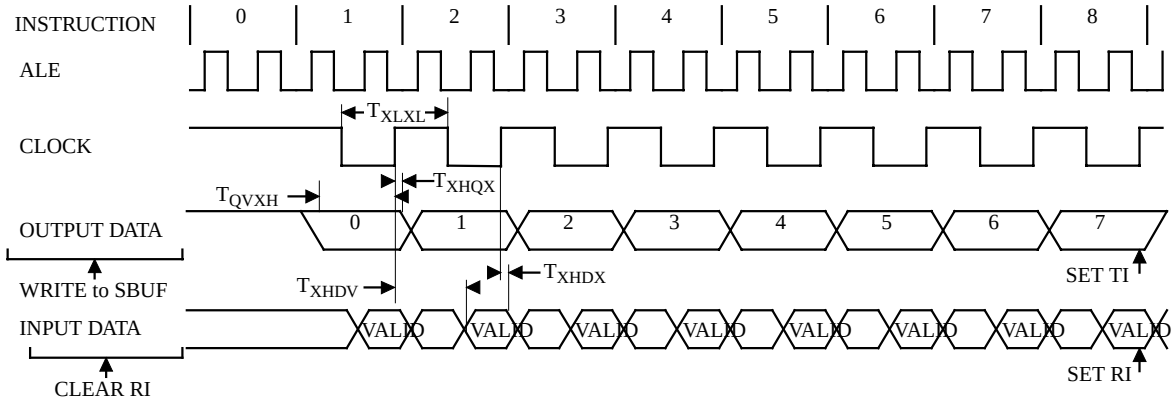


Figure 22. Shift Register Timing Waveforms

10.5.4 External Clock Drive Characteristics (XTAL1)

Table 28. AC Parameters

Symbol	Parameter	Min	Max	Units
T_{CLCL}	Oscillator Period	25		ns
T_{CHCX}	High Time	5		ns
T_{CLCX}	Low Time	5		ns
T_{CLCH}	Rise Time		5	ns
T_{CHCL}	Fall Time		5	ns
T_{CHCX}/T_{CLCX}	Cyclic ratio in X2 mode	40	60	%

10.5.5 External Clock Drive Waveforms

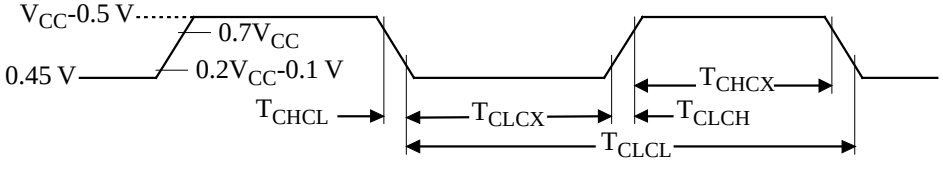


Figure 23. External Clock Drive Waveforms

10.5.6 AC Testing Input/Output Waveforms

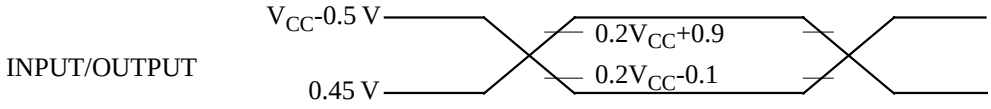


Figure 24. AC Testing Input/Output Waveforms

AC inputs during testing are driven at V_{CC} - 0.5 for a logic “1” and 0.45V for a logic “0”. Timing measurement are made at V_{IH} min for a logic “1” and V_{IL} max for a logic “0”.

10.5.7 Float Waveforms

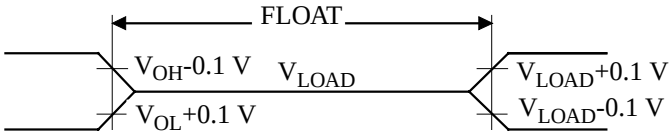


Figure 25. Float Waveforms

For timing purposes as port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm$ 20mA.

10.5.8 Clock Waveforms

Valid in normal clock mode. In X2 mode XTAL2 signal must be changed to XTAL2 divided by two.

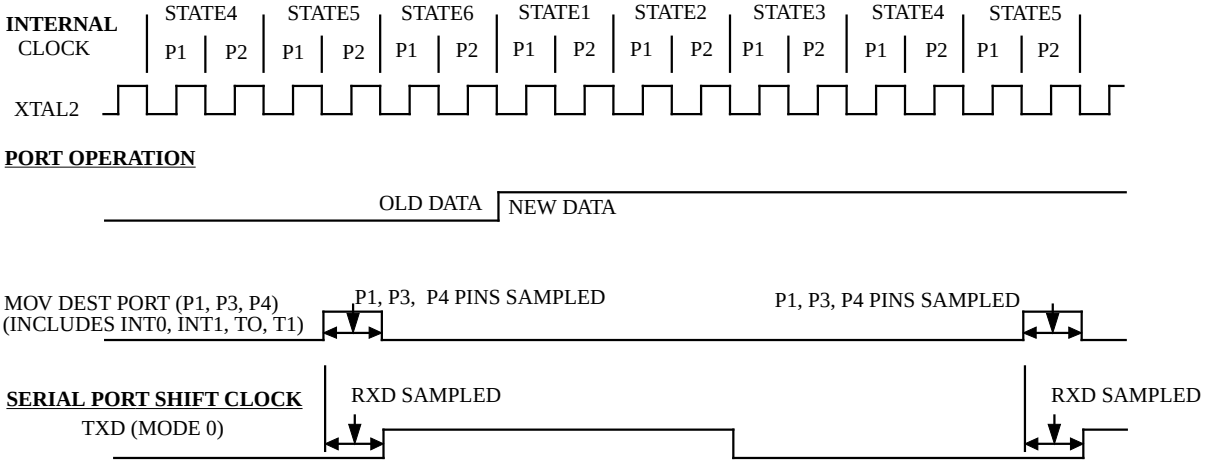
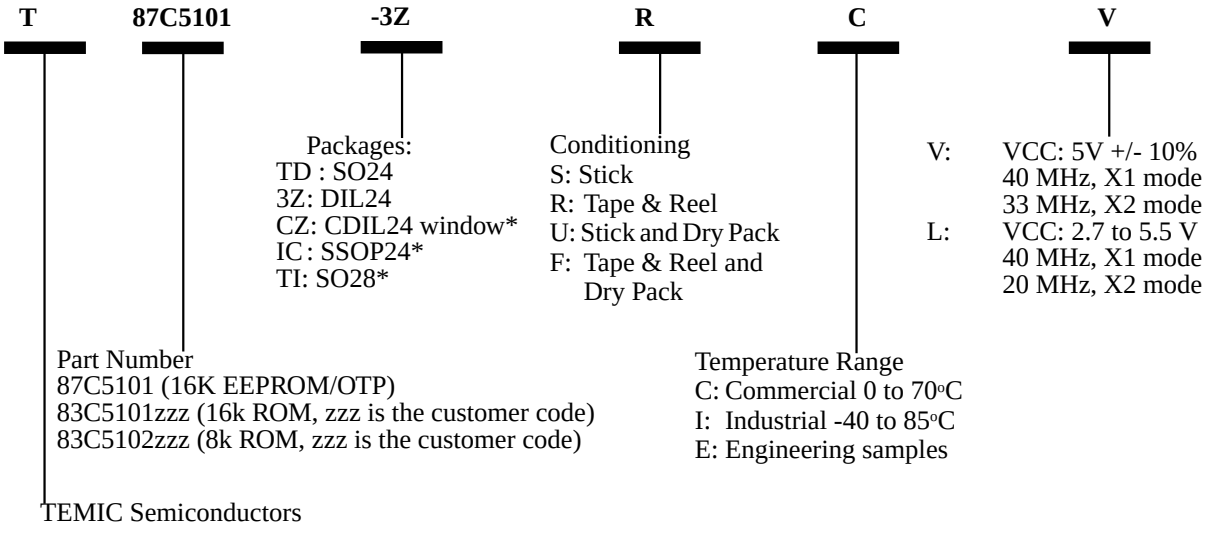


Figure 26. Clock Waveforms

This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though (T_A=25°C fully loaded) $\overline{RD}$ and $\overline{WR}$ propagation delays are approximately 50ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

11. Ordering Information



(*) Check with TEMIC Sales Office for availability

Table 29. Maximum Clock Frequency

Code	-V	-L	Unit
Standard Mode, oscillator frequency Standard Mode, internal frequency	40 40	40 40	MHz
X2 Mode, oscillator frequency X2 Mode, internal equivalent frequency	33 **66**	20 **40**	MHz

Table 30. Possible order entries

Extension	Type	T83C5101 T83C5102 Mask ROM	T87C5101 OTP
-3ZSCL	DIL24, Stick, Comm. 2.7-5.5V, 40 MHz	X	X
-3ZSCV	DIL24, Stick, Comm. 5V, 66MHz	X	X
-3ZSIL	DIL24, Stick, Ind. 2.7-5.5V, 40 MHz	X	X
-TDSCL	SO24, Stick, Comm. 2.7-5.5V, 40 MHz	X	X
-TDSCV	SO24, Stick, Comm. 5V, 66MHz	X	X
-TDSIL	SO24, Stick, Ind. 2.7-5.5V, 40 MHz	X	X
-TDRCL	SO24, Tape & Reel, Comm. 2.7-5.5V, 40 MHz	X	X
-TDRCV	SO24, Tape & Reel, Comm. 5V, 66MHz	X	X
-TDRIL	SO24, Tape & Reel, Ind. 2.7-5.5V, 40 MHz	X	X
-TISCL	SO28, Stick, Comm. 2.7-5.5V, 40 MHz	X	X
-TISCV	SO28, Stick, Comm. 5V, 66MHz	X	X
-TISIL	SO28, Stick, Ind. 2.7-5.5V, 40 MHz	X	X
-TIRCL	SO28, Tape & Reel, Comm. 2.7-5.5V, 40 MHz	X	X
-TIRCV	SO28, Tape & Reel, Comm. 5V, 66MHz	X	X
-TIRIL	SO28, Tape & Reel, Ind. 2.7-5.5V, 40 MHz	X	X
-ICUCL	SSOP24, Stick & Dry Pack, Comm. 2.7-5.5V, 40 MHz	X	X
-ICUCV	SSOP24, Stick & Dry Pack, Comm. 5V, 66MHz	X	X
-ICUIL	SSOP24, Stick & Dry Pack, Ind. 2.7-5.5V, 40 MHz	X	X
-ICFCL	SSOP24, Tape & Reel & Dry Pack, Comm. 2.7-5.5V, 40 MHz	X	X
-ICFCV	SSOP24, Tape & Reel & Dry Pack, Comm. 5V, 66MHz	X	X
-ICFIL	SSOP24, Tape & Reel & Dry Pack, Ind. 2.7-5.5V, 40 MHz	X	X
-3ZSEL	Engineering sample, DIL24, Stick, 2.7-5.5V, 40MHz		X
-TDSEL	Engineering sample, SO24, Stick, 2.7-5.5V, 40MHz		X
CZSEL	Engineering sample, Ceramic windowed DIL24, Stick, 2.7-5.5V, 40MHz		X