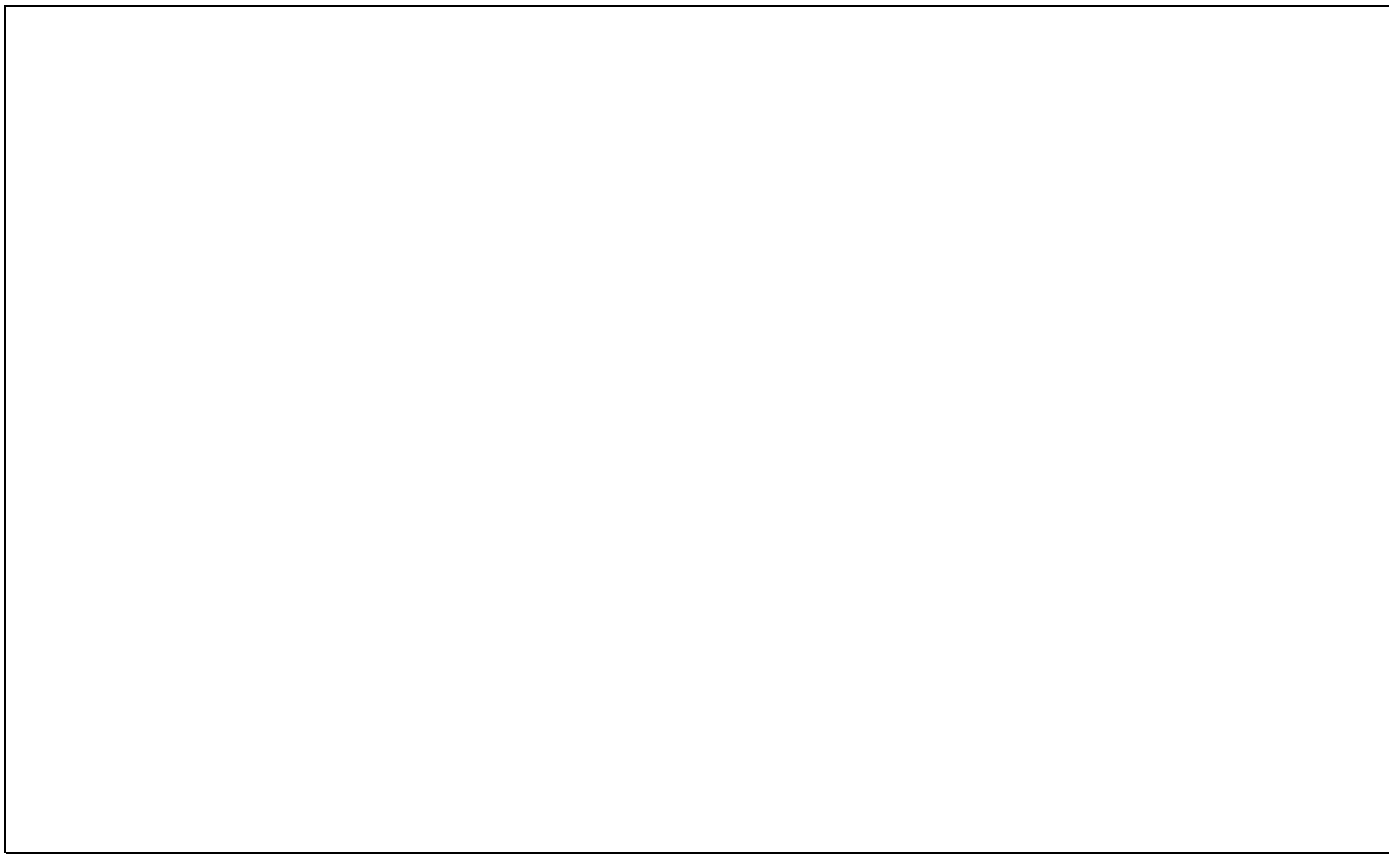
SIEMENS



ICs for Consumer Electronics

Display Processor
SDA 9280 B22

Data Sheet 1998-02-01

Edition 1998-02-01

This edition was realized using the software system FrameMaker®

Published by Siemens AG, Bereich Halbleiter, Marketing-Kommunikation, Balanstraße 73, 81541 München

Attention please!

As far as patents or other rights of third parties are concerned, liability is only assumed for components, not for applications, processes and circuits implemented within components or assemblies.

The information describes the type of component and shall not be considered as assured characteristics.

Terms of delivery and rights to change design reserved.

For questions on technology, delivery and prices please contact the Semiconductor Group Offices in Germany or the Siemens Companies and Representatives worldwide (see address list).

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Siemens Office, Semiconductor Group.

Siemens AG is an approved CECC manufacturer.

Packing

Please use the recycling operators known to you. We can also help you – get in touch with your nearest sales office. By agreement we will take packing material back, if it is sorted. You must bear the costs of transport.

For packing material that is returned to us unsorted or which we are not obliged to accept, we shall have to invoice you for any costs incurred.

Components used in life-support devices or systems must be expressly authorized for such purpose!

Critical components[1] of the Semiconductor Group of Siemens AG, may only be used in life-support devices or systems[2] with the express written approval of the Semiconductor Group of Siemens AG.

1 A critical component is a component used in a life-support device or system whose failure can reasonably be expected to cause the failure of that life-support device or system, or to affect its safety or effectiveness of that device or system.

2 Life support devices or systems are intended (a) to be implanted in the human body, or (b) to support and/or maintain and sustain human life. If they fail, it is reasonable to assume that the health of the user may be endangered.

SDA 9280 B22 Revision History:		Current Version: 1998-02-01
Previous Version:		1997-11-01
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
31	33	ESD protection: Except: Pin 36 (SDA) ±300V added

Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Recommended Operating Conditions

Under this conditions the functions given in the circuit description are fulfilled. Nominal conditions specify mean values expected over the production spread and are the proposed values for interface and application. If not stated otherwise, nominal values will apply at T_A=25°C and the nominal supply voltage.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit.

Edition 1998-02-01

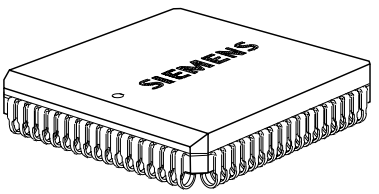
Published by Siemens AG, Semiconductor Group

SIEMENS

Display Processor SDA 9280 B22

MOS

1 Overview



P-LCC-68-1

1.1 Features

- 8-Bit amplitude resolution of each input component
  Input sample frequency up to 30 MHz
  Application in flicker reduction systems possible
- Four input data formats
  4:1:1 luminance and chrominance parallel (8 + 4 wires)
  4:2:2 CCIR 656-format (8 wires)
  4:2:2 luminance and chrominance parallel (2 x 8 wires)
  4:4:4 all components parallel (3 x 8 wires)
- Two different representations of input data
  Positive dual code
  2’s complement code
- Three D/A converters on-chip
  9-Bit amplitude resolution
  80 MHz maximal clock frequency
- DCTI (digital color transient improvement)
  A digital algorithm improves the sharpness of vertical color edges avoiding the artifacts of analog CTI-circuits
- Luminance peaking
  Separate programmable lowpass, bandpass, and highpass digital filters
- High performance digital interpolation for anti-imaging
  Two-fold oversampling
  Simplification of external analog postfiltering
- 16:9 compatibility
  Signal compression for displaying 4:3-signals on16:9-screens
  Signal expansion for displaying 16:9-signals on 4:3-screens
  Full screen display of 4:3 letter box pictures

Type	Ordering Code	Package
SDA 9280 B22	Q67101-H5039-B502-35	P-LCC-68-1

- Programmable delay for the luminance signal
  Phase adjustment between luminance and chrominance signals
- Signal manipulations
  Inverted display
  Graphic display
- Insertion of colored areas
  Programmable color and position
- Insertion of an arbitrary pattern
  Control by an external signal
  One of 4096 colors programmable
  Frame insertion for multi picture display
- N-Fold zoom facility for image memory systems
- Programmable internal PLL for clock generation
  Control of compression and expansion factors
- I^2C-Bus control
- P-LCC-68-1 package
- 5 V supply voltage

1.2 General Description

The Display Processor SDA 9280 is an integrated triple 9 Bit D/A converter which performs digital enhancements and manipulations of digital video component signals. Multiple input data formats are accepted. Operation with normal as well as doubled horizontal deflection frequency is supported. 4:3 or 16:9 display formats are possible.

1.3 Pin Configuration

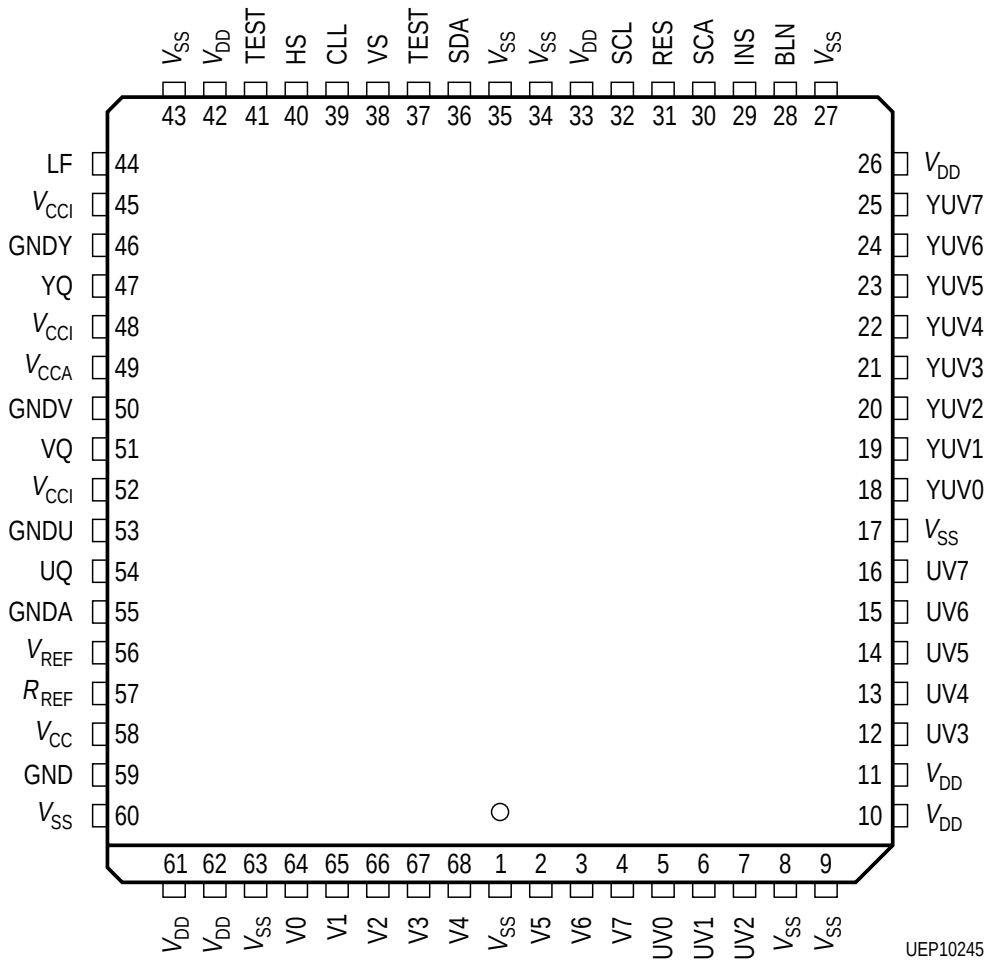


Figure 1

1.4 Pin Description

Pin No.	Symbol	Type	Description
1,17,35	V_{SS}	S	Supply voltage (V_{SS}) for input stages
8,9,27,34,43, 60,63	V_{SS}	S	Supply voltage (V_{SS}) for digital parts and PLL ***Note**: no internal connection to pins No 1,17,35*
10,11,26,33, 42,61,62	V_{DD}	S	Supply voltage (V_{DD}) for digital parts, PLL and input stages ***Note**: internal connection to V_{CCI}, V_{CCA} (about 2 Ω)*
64 ... 68, 2 ... 4	V0 ... 7	I/TTL	Data input V (see Data Input Formats)
5,6,7,12 ... 16	UV0 ... 7	I/TTL	Data input UV (see Data Input Formats)
18 ... 25	YUV0 ... 7	I/TTL	Data input YUV (see Data Input Formats)
28	BLN	I/TTL	Blanking signal, high level indicates active video line
29	INS	I/TTL	Control signal for insertion of an arbitrary pattern (frame insertion)
30	SCA	I/TTL	Clock signal for data input
31	RES	I/TTL	Reset signal (active low) for I^2C Bus
32	SCL	I	I^2C-Bus clock line
36	SDA	IQ	I^2C-Bus data line
37	TEST		Don’t connect
38	VS	I/TTL	Vertical synchronization signal for synchronizing I^2C Bus (active: HIGH)
39	CLL	I/TTL	System clock
40	HS	I/TTL	Control signal for black level insertion (line frequency)
41	TEST		Connect to VSS
44	LF		PLL-filter connection
45,48,52	V_{CCI}	S	Analog supply voltage for DACs internally connected to V_{DD}, V_{CCA} (about 2 Ω)
46	GNDY	S	Return path for YQ
47	YQ	Q/ana	Analog output: luminance signal Y
49	V_{CCA}	S	Analog supply voltage internally connected to V_{DD}, V_{CCI} (about 2 Ω)
50	GNDV	S	Return path for VQ

1.4 Pin Description (cont'd)

Pin No.	Symbol	Type	Description
51	VQ	Q/ana	Analog output: chrominance signal -(R-Y)
53	GNDU	S	Return path for UQ
54	UQ	Q/ana	Analog output: chrominance signal -(B-Y)
55	GNDA	S	Analog supply voltage
56	V_{REF}	I/ana	Analog reference voltage for DACs
57	R_{REF}		Reference resistor for DACs
58	V_{CC}	S	Analog supply voltage
59	GND	S	Analog supply voltage

S: supply, I: input, Q: output, TTL: digital (TTL)

1.5 Block Diagram

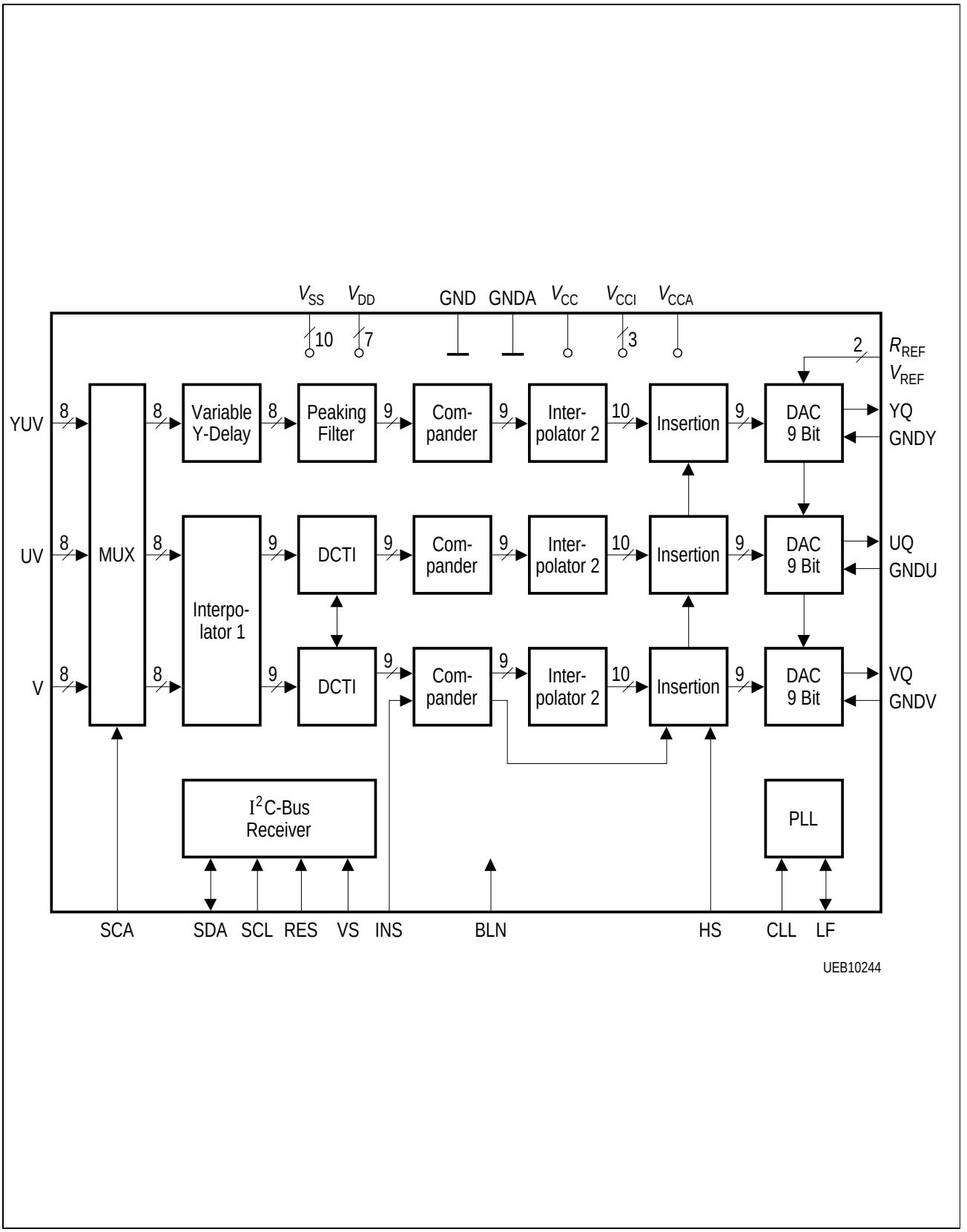


Figure 2

2 System Description

2.1 Data Input Formats

Input Pin	Data Format 4:1:1 INFOR = 01				4:2:2 Parallel INFOR = 10		CCIR 656 INFOR = 00				4:4:4 INFOR = 11
YUV7	Y_{07}	Y_{17}	Y_{27}	Y_{37}	Y_{07}	Y_{17}	U_{07}	Y_{07}	V_{07}	Y_{17}	Y_{07}
YUV6	Y_{06}	Y_{16}	Y_{26}	Y_{36}	Y_{06}	Y_{16}	U_{06}	Y_{06}	V_{06}	Y_{16}	Y_{06}
YUV5	Y_{05}	Y_{15}	Y_{25}	Y_{35}	Y_{05}	Y_{15}	U_{05}	Y_{05}	V_{05}	Y_{15}	Y_{05}
YUV4	Y_{04}	Y_{14}	Y_{24}	Y_{34}	Y_{04}	Y_{14}	U_{04}	Y_{04}	V_{04}	Y_{14}	Y_{04}
YUV3	Y_{03}	Y_{13}	Y_{23}	Y_{33}	Y_{03}	Y_{13}	U_{03}	Y_{03}	V_{03}	Y_{13}	Y_{03}
YUV2	Y_{02}	Y_{12}	Y_{22}	Y_{32}	Y_{02}	Y_{12}	U_{02}	Y_{02}	V_{02}	Y_{12}	Y_{02}
YUV1	Y_{01}	Y_{11}	Y_{21}	Y_{31}	Y_{01}	Y_{11}	U_{01}	Y_{01}	V_{01}	Y_{11}	Y_{01}
YUV0	Y_{00}	Y_{10}	Y_{20}	Y_{30}	Y_{00}	Y_{10}	U_{00}	Y_{00}	V_{00}	Y_{10}	Y_{00}
UV7	U_{07}	U_{05}	U_{03}	U_{01}	U_{07}	V_{07}					U_{07}
UV6	U_{06}	U_{04}	U_{02}	U_{00}	U_{06}	V_{06}					U_{06}
UV5	V_{07}	V_{05}	V_{03}	V_{01}	U_{05}	V_{05}					U_{05}
UV4	V_{06}	V_{04}	V_{02}	V_{00}	U_{04}	V_{04}					U_{04}
UV3					U_{03}	V_{03}					U_{03}
UV2					U_{02}	V_{02}					U_{02}
UV1					U_{01}	V_{01}					U_{01}
UV0					U_{00}	V_{00}					U_{00}
V7											V_{07}
V6											V_{06}
V5											V_{05}
V4											V_{04}
V3											V_{03}
V2											V_{02}
V1											V_{01}
V0											V_{00}

X_{AB}: X: signal component A: sample number B: bit number

The SDA 9280 accepts four different data input formats (I^2C signal: INFOR). Three sample frequency relations of Y:(B-Y):(R-Y) are possible (4:1:1 or 4:2:2 or 4:4:4).

The representation of the samples is programmable separately for luminance and chrominance signals as positive dual code or 2's complement code
(I^2C signals: INCODL, INCODC)

The amplitude resolution for each input is 8 Bit, the maximal clock frequency is 30 MHz. Consequently the SDA 9280 is dedicated for applications in high quality digital video systems. The data input stages and the internal data multiplexer operate with a special data input clock (SCA). For applications in the Siemens MEGAVISION® System the SCA-clock is identical with the memory output clock. A separation of the data input clock and the system clock is relevant to handle the special data format occurring at "zoom" operation mode. For other applications SCA can be connected with CLL.

***Note**: Zoom mode causes a greater signal delay time of the whole IC. Zoom mode identification is performed automatically.*

2.2 Chrominance Interpolation (Interpolator 1)

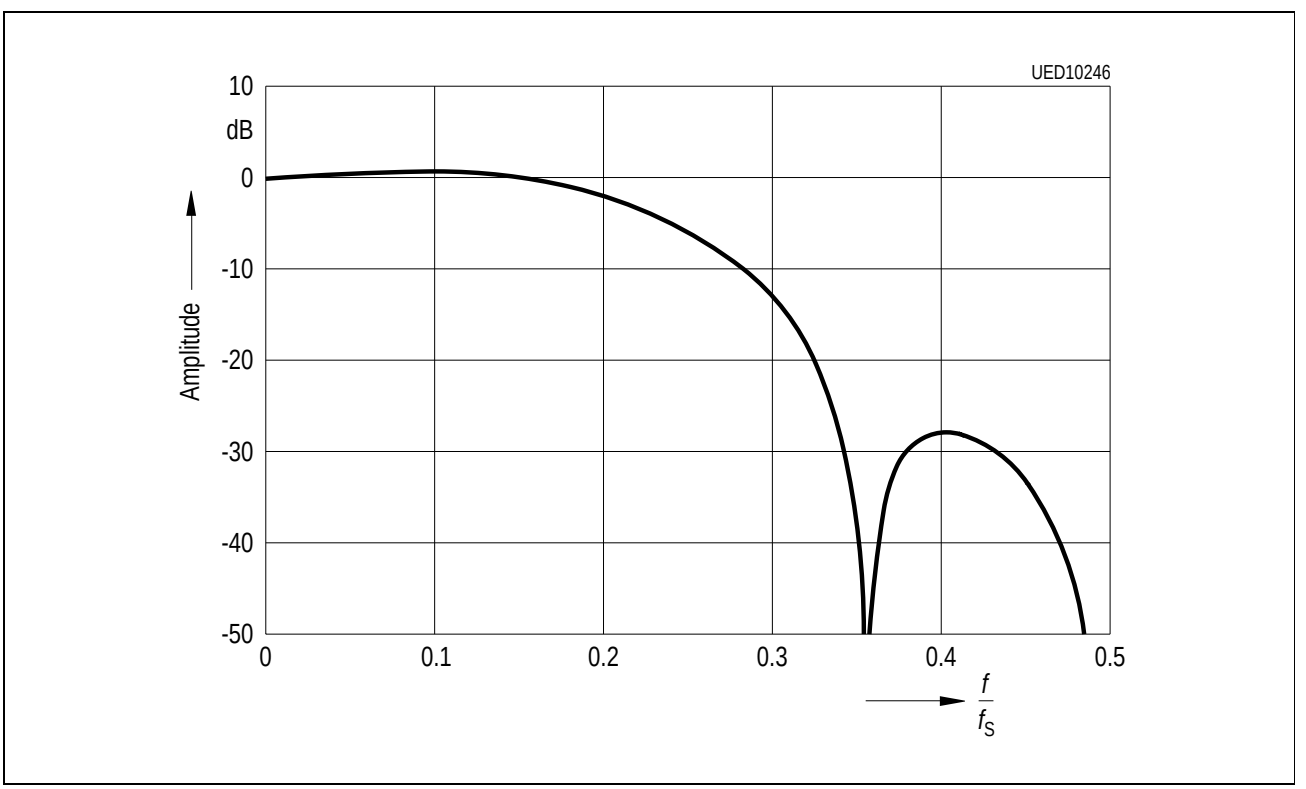


Figure 3
Frequency Response of a Filter Stage of Interpolator 1
(f_s is the sampling frequency at the output of the interpolation filter stage)

For internal processing the 4:4:4 parallel format is used. The 4:1:1 data are interpolated by two interpolation filters having the same frequency response (**see figure 3**) to the 4:4:4 format. Each filter performs a doubling of the sample frequency. The 4:4:4 interpolation of 4:2:2 data is done by the second filter stage. The diagram shows the frequency response of one filter stage.

Interpolation filtering can be switched off for each stage separately (I^2C signals: INT422, INT444). Then each sample is simply repeated twice. Activation of interpolation filtering is recommended because analog postfiltering of chrominance signals then can be greatly simplified (**see also Interpolator 2**).

2.3 Luminance Peaking Filter

The luminance peaking filter improves the over all frequency response of the luminance channel. It consists of three filters working in parallel. They have low pass (LP(z)), band pass (BP(z)) and high pass (HP(z)) characteristics. Their gain factors are separately programmable (I^2C signals: LCOF, BCOF, HCOF) according to the following equations:

$$LCOF * LP(z) + BCOF * BP(z) + HCOF * HP(z)$$

with:
$LCOF = 0 \ldots [1/4] \ldots 3/2, 2$
$BCOF = 0 \ldots [1/4] \ldots 3, 7/2, 4, 5$
$HCOF = 0 \ldots [1/4] \ldots 3, 7/2, 4, 5$
$LP(z) = 1/16 * (1 + z^{-1})^4$
$BP(z) = -1/8 * (1 - z^{-2})^2$
$HP(z) = 1/16 * (1 - z^{-1})^4$

An amplification of up to 14 dB at the half of the sample frequency is available. The high pass and band pass filters are equipped with a common coring algorithm. It is optimized to achieve a smooth display of grey scales, not to improve the signal-to-noise ratio. Therefore no artifacts are produced. Coring can be switched off (I^2C signal: COR).

***Note**: The peaking filter may shift the black level of the signal. This has to be considered for black level insertion (**see Insertion Facilities**).*

A delay line for the luminance signal enables an adaption to the delay of the chrominance signals. A range of -8 to +7 clock periods of the system clock CLL is programmable (I^2C signal: YDEL1).

An additional special filtering is available for compensating a non linear phase response of the analog part of the signal path.

$$(1 + PHACOM) * z^{-1} - PHACOM$$

Three adjustments are I^2C-Bus programmable: PHACOM = 0, 1/4, 1/8.

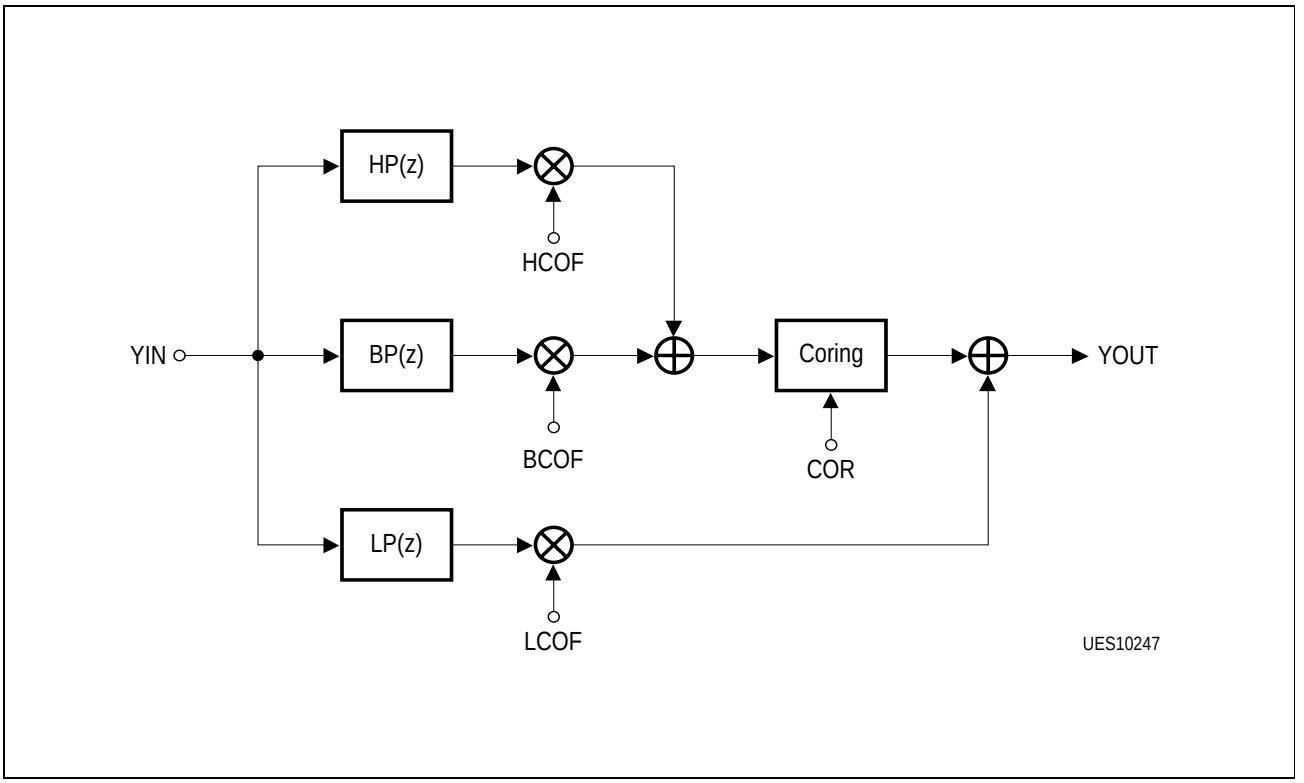


Figure 4
Luminance Peaking

2.4 Digital Color Transient Improvement (DCTI)

A new digital algorithm is implemented to improve horizontal transitions of the chrominance signals resulting in a better picture sharpness. A slow change from one color to another by reason of small chrominance bandwidth is replaced by a steep transition.

The exact position of a color transition (POS) is calculated by detecting the corresponding zero transition of the second derivative of both chrominance signals. Low pass filtering (LPU, LPV, LPUV) is performed to avoid noise sensitivity. The width of a transition is derived from a threshold detector signal. It indicates an area around the detected position where the first derivatives of the chrominance signals exceed a programmable threshold (I^2C signal: THRESH). The parameter THRESH modifies the sensitivity of the DCTI-circuit. High values cause that only significant color transitions are improved. Small color variations remain unchanged. The detected transition width can be limited by the programmable parameter TRAWID. This parameter performs an adaption to the input chrominance band width. For signals with small chrominance bandwidth (e.g. video recorders) the DCTI-performance is optimized using high values for TRAWID. Input signals with high chrominance bandwidth should be processed with small values for TRAWID. If standard 4:1:1 video signals are processed, it is recommended to choose values of the mid range for both parameters THRESH and TRAWID.

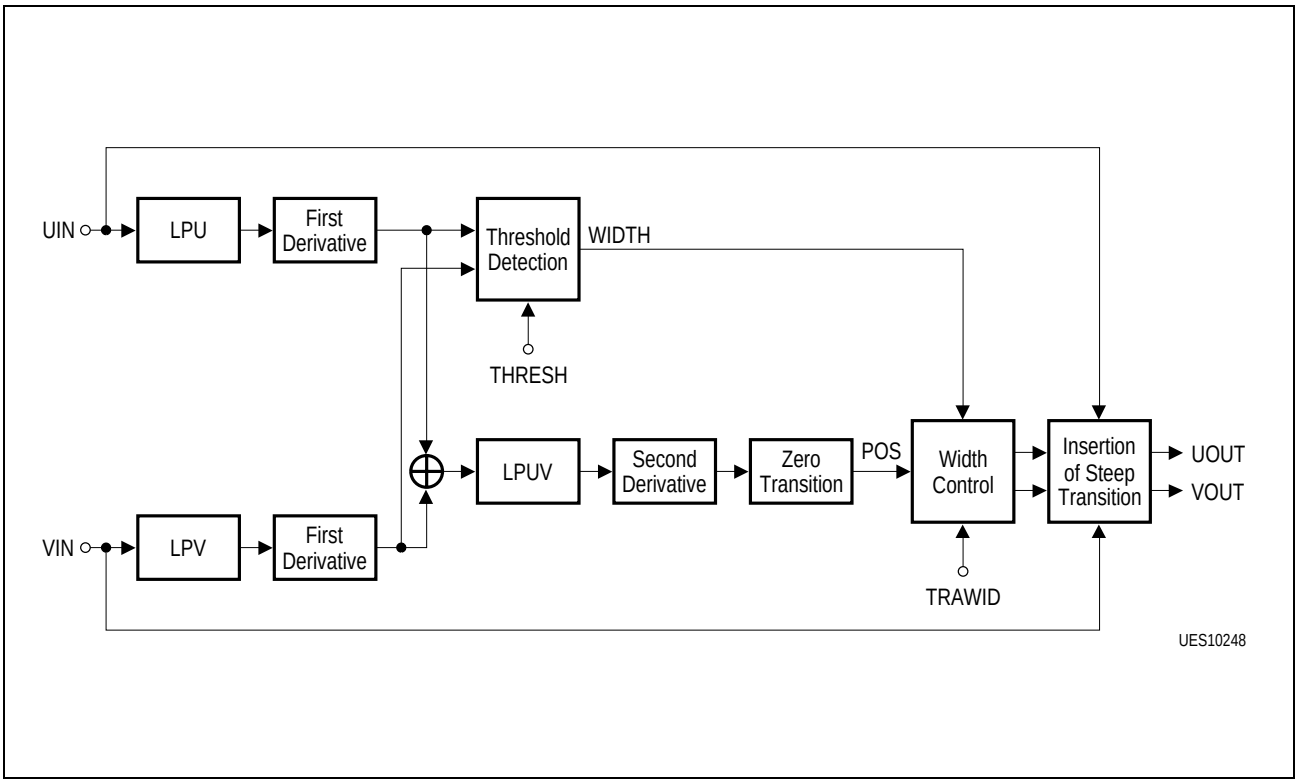


Figure 5
Digital Color Transient Improvement

2.5 Picture Manipulations

A graphic display effect is realized by programmable reduction of amplitude resolution (I^2C signals: YGR, YGRRES, CGR, CGRRES). A resolution of 1 to 4 bits is available. A special characteristic avoids a reduction of picture brightness and color saturation.

The inverted display mode is attained by a programmable bit inversion for each signal component (I^2C signals: YINV, UINV, VINV).

Multiple combinations of both manipulations supply very amazing effects on the display.

2.6 16:9-Operation, Signal Compander

The compander enables a display with correct geometric proportions of 4:3 signals on 16:9-screens or 16:9-signals on 4:3-screens. A full screen display of 4:3-letterbox signals on 16:9-screens is also practicable. Having a full screen display of such signals on 4:3-screens only a part of the picture can be shown. In this operation mode a horizontal shift of the picture part used for display is programmable (I^2C signal: READD). Expansion in vertical direction must be realized by manipulation of the vertical deflection current.

To satisfy all these demands a horizontal compression or expansion of the video signals is performed by raising or reducing the sample frequency. The data are written into a memory using the system clock CLL and read with a clock of higher or lower frequency.

This realization does not effect the horizontal detail resolution of the picture because no filtering is executed.

The highest read frequency is 4/3 of the CLL-frequency for signal compression, the lowest is 3/4 of the CLL-frequency for signal expansion. The reading clock is supplied by the internal PLL.

The compander operation mode is programmable via I^2C signals COMP and COMEX.

***Note**: Positioning of a 4:3-signal on a 16:9-screen is realized by delaying the HS-signal. HS also controls the deflection circuit. In the Siemens MEGAVISION® System a programmable HS-delay is available in the Memory Sync Controller (MSC) circuit.*

2.7 Oversampling, Interpolator 2

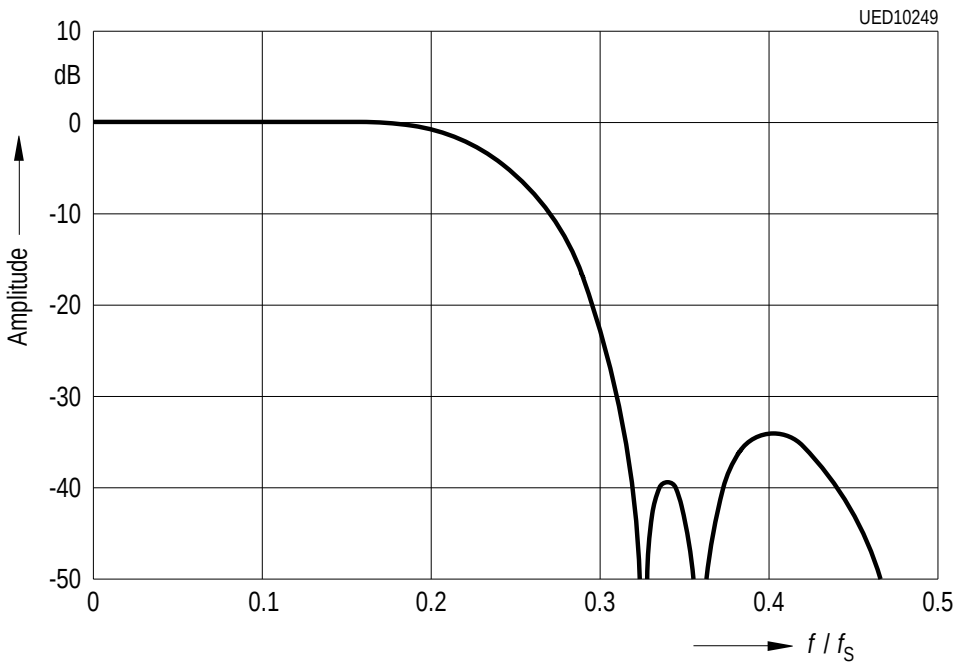


Figure 6
Frequency Response of Interpolator 2
(f_S is the sampling frequency at the output of the interpolation filter)

In general D/A conversion requires postfiltering to avoid non-harmonic distortions caused by intermodulations of the signal with its spectral images. These intermodulations may come from non-linear characteristics of subsequent amplifier stages or of the display. The spectral images are duplicates of the signal spectrum around multiples of the sampling frequency. These images, a counterpart of aliasing in the A/D conversion, become visible after D/A conversion. They are only reduced by the sinx/x characteristic of the D/A converter.

An example of such non-harmonic distortions are periodic stripes with a frequency of 900 kHz appearing in a 4.8 MHz test pattern which is sampled with 13.5 MHz clock frequency (2 ∗ 4.8 MHz – (13.5 – 4.8) MHz = 900 kHz).

The ideal postfiltering comprises an ideal lowpass filter with an edge frequency at the maximum signal frequency and a stop band rejection of at least 30 or 40 dB. In practice the postfilter can be greatly simplified when a large transition band is allowed. For this purpose a digital interpolator is implemented with a steep transition at the half of the sampling frequency and an out of band rejection of more than 30 dB before D/A conversion. Combined with a two-fold oversampling the first image appears around twice the sampling frequency, thus leaving considerably more space for the transition band of an analog postfilter. There is another good reason for using a digital interpolation. Since the output frequency may vary with different compression or expansion factors an analog filter with varying edge frequencies is necessary. This requirement can only be fulfilled in the digital domain because the edge frequency is linearly controlled by the sample frequency.

The amplification factor of the implemented interpolation filter is 65/64. The maximal output clock frequency is 8/3 times of the input sample frequency. The diagram (**figure 6**) shows the frequency response.

Oversampling can be switched off (I^2C signal: OVSAMP). Then the 4:4:4 format is directly D/A converted. With activated oversampling it is possible to switch off oversampling filtering (I^2C signal: OVFILT). In this operation mode the input clock frequency is doubled but each sample is simply repeated twice.

2.8 Insertion Facilities

Three different values are inserted into the video signal: black level, a colored background area and an arbitrary colored pattern.

The blanking interval of the input signal is not processed by the compander. Therefore the black level shifting in the luminance signal, caused by the peaking filter (coefficient LCOF) and the amplification factor of the oversampling filter, has to be restored by inserting the correct value (BLACK). BLACK is programmable and must be computed according to the coding of the input data using the following formulas:

BLACK = 128 + 65/128 ∗ LCOF ∗ (BLACKIN – 128) for positive dual coding
BLACK = 128 + 65/128 ∗ LCOF ∗ BLACKIN for 2’s complement

BLACKIN is the black level of the input signal, LCOF is the Lowpass coefficient of the Luminance Peaking Filter: 0 ... [1/4] ... 1.5, 2

Black level insertion is controlled by the external signal HS. This signal also controls the deflection circuit, consequently it has a stable phase referring to the horizontal blanking interval. The value BLACK is inserted during 80 clock periods of the clock CLL. In the Siemens MEGAVISION® System HS is supplied by the MSC-circuit. To adjust the right insertion phase a programmable delay of HS is available (I^2C signal: HSDEL).

The second insertion facility produces a colored background area on the display controlled by I^2C Bus. Activating this insertion mode (I^2C signal: BACKGR) parts of the display area are covered with a constant color (I^2C signals: COLBY, COLBU, COLBV). Starting at a programmable pixel position of each line (I^2C signal: BCKPOS) the following part is covered with the background values. The width of the insertion is also programmable (I^2C signal: BCKWID). To realize for example two vertical background stripes at the left and right side of the display BCKPOS should be set to a high value. Then the background color is inserted over the blanking interval (except the black level phases) up to the first active pixels of the following line fixed by BCKWID. An example for application is the display of a 4:3-picture on a 16:9-screen. The free parts of the display and also the noisy start and end of the picture can be filled with background color. An opening and closing curtain can also be realized using background insertion mode.

Insertion of an arbitrary pattern is controlled by the external signal INS. The color of the pattern is programmable (I^2C signals: COLFY, COLFU, COLFV). The insertion raster corresponds to the 4:4:4 format. A fixed phase to the video signal is guaranteed by processing the INS-signal by the compander. Using this insertion mode a colored framing for multi-picture mode can be realized. The MSC of the Siemens MEGAVISION® System supplies a suited signal (FRM). A connection of the BLN2-signal supplied by the MSC to the INS-input enables a complete blanking of the horizontal and vertical inactive parts of the video signal.

The polarity of the INS-signal is programmable by I^2C Bus (INSNEG).

All insertions are performed after oversampling resulting in sharp transitions without overshooting.

2.9 Amplification, D/A Conversion

Before D/A conversion a fine adjustment of the phase of the luminance signal is performed (I^2C signal: YDEL2). The delay of the luminance signal can be varied by one period of the D/A converter clock.

The amplification factors of each signal component can be reduced by a factor of 0.5 (I^2C signals: AMPY, AMPU, AMPV). This reduction of nominal amplification reserves one bit for D/A conversion of overshooting, resulting from strong peaking or interpolation filtering. The input amplitude resolution of 8 Bit is not reduced. For conversion of signals without or with only small overshooting a reduction of the amplification factor is not necessary. A digital limiter circuit prevent the D/A converters from possible overdriving by clipping.

Note: *Clipping causes a non-linear deformation with interferences between multiples of the signal frequency and the sample rate of the signal and should be avoided by reducing the amplification factor.*

A triple 9 Bit D/A converter is implemented on the SDA 9280. The DACs are short circuit protected converters with current outputs.

The Full Range Output Current of the Y, U, and V channels (I_{OFR}) is determined by the current I_{REF} at the R_{REF} pin by

$I_{OFR} \cong (4/3)\ I_{REF}$

The voltage at pin R_{REF} is generated via pin V_{REF} by an internal operational amplifier and follows the voltage at pin V_{REF}. Thus I_{REF} is given by

$I_{REF} \cong V_{VREF}/R_{REF}$

where R_{REF} is a resistor between pin R_{REF} and analog ground. Another way to define I_{REF} is the application of a current sink at the R_{REF} point. For recommended values of V_{VREF} and I_{REF} see chapter 'Recommended Operation Conditions'. For applications with lower requirements there is still another way to define I_{OFR}: Connect pin V_{REF} to the positive supply and apply a resistor against ground. Since in this operation mode the internal reference amplifier goes into saturation, the exact value of I_{REF} is not so well predictable

2.10 PLL Circuit

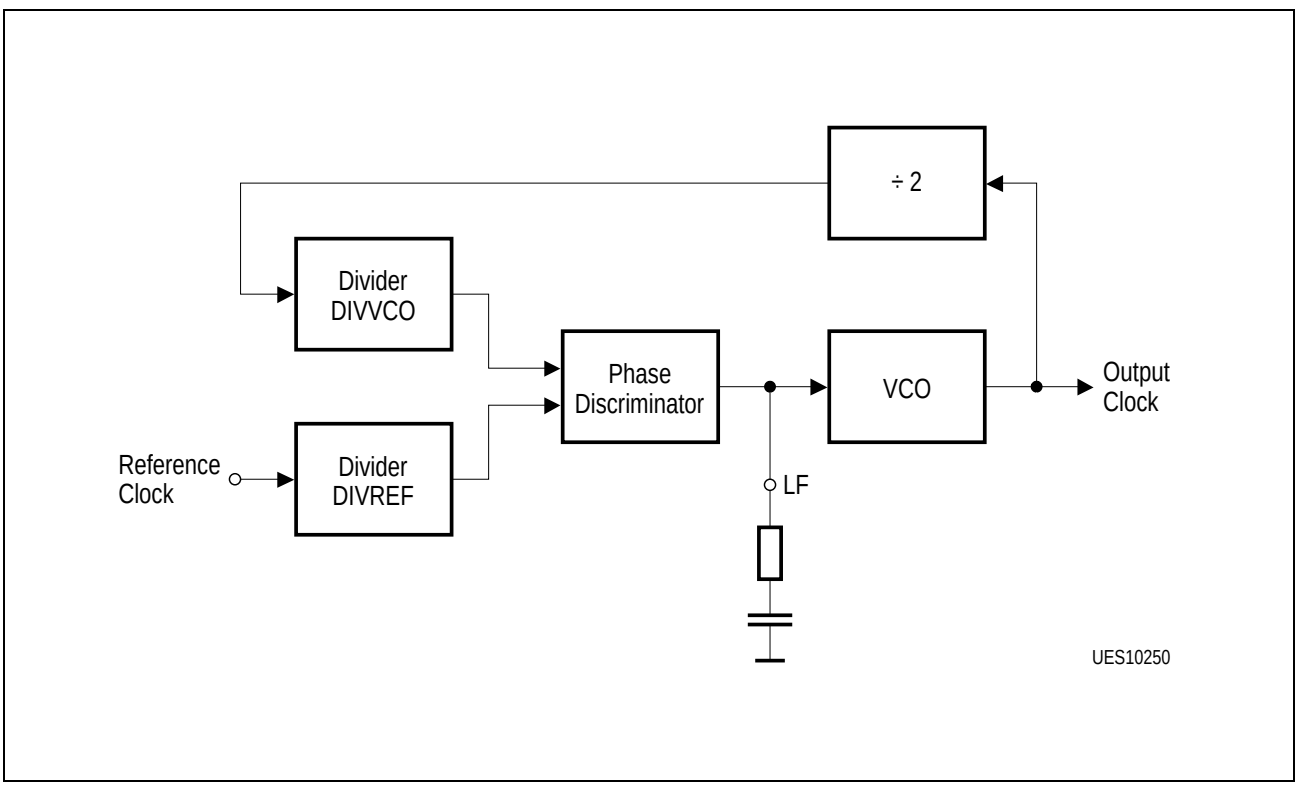


Figure 7

The internal PLL supplies the clock signals needed for compander operation, output processing and D/A conversion. The output frequency of the PLL is defined by programming the divider factors of the reference clock and of the VCO clock
(I^2C signals: DIVREF, DIVVCO). The PLL always supplies the frequency needed for oversampling. The clocks used in the other output processing parts are derived from this oversampling clock. Even if no oversampling is programmed (OVSAMP = 0) DIVREF

and DIVVCO must be set according to the respective oversampling frequency. The reference clock of the PLL is the system clock CLL. The output frequency of the PLL f_{OUTPUT} is calculated by the following equation:

$$f_{OUTPUT} = f_{REFERENCE} * (2 * DIVVCO) / DIVREF$$

***Note**: An arbitrary setting of the output frequency is not allowed. It has to be observed that there is resulting an integer number of clock periods per line. E.g. the input signal has 858 clock periods per line, 3:4 signal expansion results in 858 * 3/4 = 643.5 clock periods per line, which is not an integer number. Therefore this adjustment results in phase jumps of the output clock and in an unstable working condition of the PLL.*

The following table gives an overview of possible PLL modes referred to an input signal with 864 pixels per line and a clock frequency of 13.5 MHz.

Compression-/ Expansion-Factor	**Resulting Clock Periods per Line**	**Compander Read Frequency [MHz]**	**DIVVCO**	**DIVREF**
4:3	1152	18	4	3
5:4	1080	16.875	5	4
11:9	1056	16.5	11	9
7:6	1008	15.75	7	6
9:8	972	15.1875	9	8
10:9	960	15	10	9
13:12	936	14.625	13	12
1:1	864	13.5	4	4
15:16	810	12.65625	15	16
11:12	792	12.375	11	12
8:9	768	12	8	9
7:8	756	11.8125	7	8
5:6	720	11.25	5	6
13:16	702	10.96875	13	16
7:9	672	10.5	7	9
3:4	648	10.125	3	4

The PLL circuit can be switched inactive (I^2C signal: PLLON). In this mode the system clock is also used for output processing and D/A conversion.

To achieve an optimal PLL operation an adaption to the required frequency range can be programmed (I^2C signal: PLLRAN).

2.11 Input-Output Signal Delay Time

Due to several digital signal processing stages transients of the digital input signal at the YUV inputs appear with a certain delay at the analog YUV outputs. In the following table are defined the values for two typical circuit configurations. The configuration of the circuit is defined as the total configuration of all programmable signal processing stages on the device, the programming itself is performed via the I^2C Bus.

Name	Function	Time delay
Internal PLL	Switched OFF (Subaddress 10_H, Bit D5 ... D0 = 00 0000)	120 CLL typ
Compander	Bypassed (Subaddress 06_H, Bit D1 = 0)	
Oversampling	No (Subaddress 07_H, Bit D1 ... D0 = 00)	
Input data format	(Subaddress 00_H, Bit D5 ... D4 = 01 or 10 or 11)	
Zoom	No (frequency of SCA and CLL is identical)	
Internal PLL	Switched ON (Subaddress 10_H, Bit D5 ... D0 = 00 0010) (Subaddress 14_H, Bit D7 ... D0 = 0100 0100)	126 CLL typ
Compander	Active without compression or expansion (Subaddress 06_H, Bit D0 = 0) (Subaddress 06_H, Bit D7 ... D2 = 000001)	
Oversampling	Yes (Subaddress 07_H, Bit D1 ... D0 = 11)	
Input data format	(Subaddress 00_H, Bit D5 ... D4 = 01 or 10 or 11)	
Zoom	No (frequency of SCA and CLL is identical)	

2.12 I²C-Bus Control

2.12.1 I²C-Bus Address

0	0	1	0	1	1	0

2.12.2 I²C-Bus Format

write:

S	0	0	1	0	1	1	0	0	A	Subaddress	A	Data Byte	A	*****	A	P

read:

S	0	0	1	0	1	1	0	1	A	Data Byte n	A	Data Byte (n+1)	A	*****	NA	P

Reading starts at the last write address n. Specification of a subaddress in reading mode is not possible.

S: Start condition
A: Acknowledge
P: Stop condition
NA: Not acknowledge

An automatical address increment function is implemented.

After switching on the IC (RES = 0), all bits are set to defined states. Except the following bits the reset state is “0”. The bits YDEL13, BCOF2, LCOF2, HCOF2, DIVREF2, DIVVCO2 are set to “1” to ensure a basic working condition.

In order to avoid distortions of the picture during the active lines, the following bits are updated internally only during the HIGH-phase of VS (the programming of the I²C-Bus interface however is not affected by this synchronisation):

Subaddress	**Bit**	**Subaddress**	**Bit**
00_H	D1 ... D0	07_H	D2 ... D0
02_H	D4 ... D0	09_H	D7 ... D0
03_H	D7 ... D0	$0A_H$	D7 ... D0
04_H	D6 ... D0	$0B_H$	D6 ... D0
05_H	D6 ... D0	$0F_H$	D0
06_H	D7 ... D0		

2.12.3 I²C-Bus Commands

Subadd. (Hex.)	Data Byte							
	D7	D6	D5	D4	D3	D2	D1	D0
00_H	INSNEG	0	INFOR1	INFOR0	INCODL	INCODC	INT422	INT444
01_H	THRESH3	THRESH2	THRESH1	THRESH0	TRAWID3	TRAWID2	TRAWID1	TRAWID0
02_H	0	0	0	CGR	CGRRES1	CGRRES0	UINV	VINV
03_H	YGR	YGRRES1	YGRRES0	YINV	YDEL13	YDEL12	YDEL11	YDEL10
04_H	0	LCOF2	LCOF1	LCOF0	BCOF3	BCOF2	BCOF1	BCOF0
05_H	0	COR	PHACOM1	PHACOM0	HCOF3	HCOF2	HCOF1	HCOF0
06_H	READD5	READD4	READD3	READD2	READD1	READD0	COMP	COMEX
07_H	0	0	0	0	0	BACKGR	OVFILT	OVSAMP
08_H	0	0	HSDEL5	HSDEL4	HSDEL3	HSDEL2	HSDEL1	HSDEL0
09_H	BCKPOS7	BCKPOS6	BCKPOS5	BCKPOS4	BCKPOS3	BCKPOS2	BCKPOS1	BCKPOS0
$0A_H$	BCKWID7	BCKWID6	BCKWID5	BCKWID4	BCKWID3	BCKWID2	BCKWID1	BCKWID0
$0B_H$	0	BLACK6	BLACK5	BLACK4	BLACK3	BLACK2	BLACK1	BLACK0
$0C_H$	COLFY3	COLFY2	COLFY1	COLFY0	COLBY3	COLBY2	COLBY1	COLBY0
$0D_H$	COLFU3	COLFU2	COLFU1	COLFU0	COLBU3	COLBU2	COLBU1	COLBU0
$0E_H$	COLFV3	COLFV2	COLFV1	COLFV0	COLBV3	COLBV2	COLBV1	COLBV0
$0F_H$	0	0	0	0	AMPY	AMPU	AMPV	YDEL2
10_H	PLLRAN1	PLLRAN0	0	0	0	0	PLLON	0
11_H	0	1	0	0	0	0	0	0
12_H	0	0	0	0	0	0	0	0
13_H	0	0	0	0	0	0	1	0
14_H	DIVREF3	DIVREF2	DIVREF1	DIVREF0	DIVVCO3	DIVVCO2	DIVVCO1	DIVVCO0

2.12.4 Detailed Description

Subaddress 00_H: Interpolation Mode and Input Format

Bit	Name	Function
D0	INT444	4:4:4 Interpolation filtering: 0: interpolation 4:2:2 –> 4:4:4 OFF 1: interpolation 4:2:2 –> 4:4:4 ON
D1	INT422	4:2:2 Interpolation filtering: 0: interpolation 4:1:1 –> 4:2:2 OFF 1: interpolation 4:1:1 –> 4:2:2 ON
D2	INCODC	Coding of chrominance input data: 0: positive dual code 1: 2’s complement
D3	INCODL	Coding of luminance input data: 0: positive dual code 1: 2’s complement
D5, D4	INFOR	Input data format: 00: CCIR 656 01: 4:1:1luminance, chrominance parallel (8 + 4 wires) 10: 4:2:2luminance, chrominance parallel (2 x 8 wires) 11: 4:4:4all components parallel (3 x 8 wires)
D6		No function assigned. Assign binary value: 0
D7	INSNEG	Polarity of INS input signal: 0: positive polarity 1: negative polarity

Subaddress 01_H: Digital Color Transition Improvement Control

Bit	Name	Function
D3 ... D0	TRAWID	DCTI: maximal length of an improved transition: 0000: DCTI OFF 0001: 2 pixel : : 1100: 24 pixel
D7 ... D4	THRESH	DCTI: sensitivity threshold: 0000: lowest threshold (highest sensitivity) : : 1111: highest threshold (lowest sensitivity)

Subaddress 02_H: Color Feature Control

Bit	Name	Function
D0	VINV	Inversion of (R-Y)-signal: 0: inversion OFF 1: inversion ON
D1	UNIV	Inversion of (B-Y)-signal: 0: inversion OFF 1: inversion ON
D3, D2	CGRRES	Amplitude resolution of chrominance signals (CGR = 1): 00: 1 Bit 01: 2 Bit 10: 3 Bit 11: 4 Bit
D4	CGR	Chrominance graphic display: 0: OFF 1: ON
D7 ... D5		No function assigned. Assign binary value : 000

Subaddress 03_H: Luminance Feature Control

Bit	Name	Function
D3 ... D0	YDEL1	Delay adjustment of luminance signal: 0000: -8 clock periods (CLL) 0001: -7 clock periods (CLL) : : 1000: no delay : : 1111: +7 clock periods (CLL)
D4	YINV	Inversion of luminance signal: 0: inversion OFF 1: inversion ON
D6, D5	YGRRES	Amplitude resolution of luminance signal (YGR = 1): 00: 1 Bit 01: 2 Bit 10: 3 Bit 11: 4 Bit
D7	YGR	Luminance graphic display: 0: OFF 1: ON

Subaddress 04_H: Luminance Peaking Control

Bit	Name	Function
D3 ... D0	BCOF	Luminance peaking, gain of band pass filter: 0000: 0 0001: 1/4 : : : [1/4] : : 1100: 12/4 1101: 14/4 1110: 16/4 1111: 20/4
D6 ... D4	LCOF	Luminance peaking, gain of low pass filter: 000: 0 001: 1/4 : : : [1/4] : : 110: 6/4 111: 8/4
D7		No function assigned. Assign binary value: 0

Subaddress 05_H: Luminance Peaking Control

Bit	Name	Function
D3 ... D0	HCOF	Luminance peaking, gain of high pass filter: 0000: 0 0001: 1/4 : : : [1/4] : : 1100: 12/4 1101: 14/4 1110: 16/4 1111: 20/4
D5, D4	PHACOM	Filter coefficient for compensation of non-linear phases: 00: 0 01: 1/8 10: 2/8
D6	COR	Luminance peaking, coring for high- and band-pass filter: 0: OFF 1: ON
D7		No function assigned. Assign binary value: 0

Subaddress 06_H: Compander Control

Bit	Name	Function
D0	COMEX	Compander working condition: 0: signal compression 1: signal expansion ***Note:*** *For oversampling without compression or expansion COMEX = 0 is recommended in order to minimize the signal delay time.*
D1	COMP	Compander activation: 0: bypass 1: compander active
D7 ... D2	READD	Compander, displayed picture part: (shifting raster: 4 pixels) 000000: not recommended 000001: left part of the picture : : 111111: right part of the picture ***Note:*** *For signal compression READD = 101101 is required. For oversampling without compression or expansion READD = 000001 is required.*

Subaddress 07_H: Oversampling Control (Interpolator 2) and Background Activation

Bit	Name	Function
D0	OVSAMP	Oversampling control: 0: doubling of sample frequency OFF 1: doubling of sample frequency ON
D1	OVFILT	Oversampling control (OVSAMP = 1): 0: interpolation filtering OFF 1: interpolation filtering ON
D2	BACKGR	Activation of background insertion: 0: insertion OFF 1: insertion ON
D7 ... D3		No function assigned. Assign binary value: 00000

Subaddress 08_H: Black Level Insertion Control

Bit	Name	Function
D5 ... D0	HSDEL	Start of black level insertion, delay to HS-signal: 000000: no delay 000001: 16 clock periods (CLL) delay : : 111111: 1008 clock periods (CLL) delay ***Note:*** *If HSDEL is greater than the number of samples per line there is no insertion of black level.*
D7 ... D6		No function assigned. Assign binary value: 00

Subaddress 09_H: Background Insertion Control

Bit	Name	Function
D7 ... D0	BCKPOS	Background insertion, positioning of inserted area: 00000000:starting at pixel 290 00000001:starting at pixel 292 : : 11111111:starting at pixel 800

Subaddress $0A_H$: Background Insertion Control

Bit	Name	Function
D7 ... D0	BCKWID	Background insertion, horizontal width of inserted area: 00000000:136 pixel 00000001:140 pixel : : 11111111:1156 pixel ***Note****: If BCKWID is greater than the number of pixels per line the whole line is filled with background color.*

Subaddress $0B_H$: Black Level Coding

Bit	Name	Function
D6 ... D0	BLACK	Coding of inserted black level (Y-channel), computation see chapter 'Insertion Facilities': 0000000: 0 0000001: 1 : : 1111111: 127
D7		No function assigned. Assign binary value: 0

Subaddress $0C_H$: Background Color/Y Signal

Bit	Name	Function
D3 ... D0	COLBY	Background color (luminance):4 MSBs
D7 ... D4	COLFY	Color of inserted pattern (luminance):4 MSBs

Subaddress $0D_H$: Background Color/B-Y Signal

Bit	Name	Function
D3 ... D0	COLBU	Background color (B-Y):4 MSBs
D7 ... D4	COLFU	Color of inserted pattern (B-Y):4 MSBs

Subaddress $0E_H$: Background Color/R-Y Signal

Bit	Name	Function
D3 ... D0	COLBV	Background color (R-Y):4 MSBs
D7 ... D4	COLFV	Color of inserted pattern (R-Y):4 MSBs

Subaddress $0F_H$: Signal Amplification

Bit	Name	Function
D0	YDEL2	Delay fine adjustment of luminance signal: 0: no delay 1: 1 D/A converter clock period
D1	AMPV	Amplification of (R-Y) signal path: 0: amplification = 0.5 1: amplification = 1
D2	AMPU	Amplification of (B-Y) signal path: 0: amplification = 0.5 1: amplification = 1
D3	AMPY	Amplification of luminance signal path: 0: amplification = 0.5 1: amplification = 1
D7 ... D4		No function assigned. Assign binary value: 0000

Subaddress 10_H: PLL Control

Bit	Name	Function
D0		No function assigned. Assign binary value: 0
D1	PLLON	Activation of internal PLL: 0: PLL OFF 1: PLL ON
D5 ... D2		No function assigned. Assign binary value: 0000
D7, D6	PLLRAN	Frequency range of internal PLL: 00: 9 ... 13 MHz 01: 11 ... 40 MHz 10: 29 ... 60 MHz 11: 44 ... 80 MHz

Subaddress 11_H: Test Control

Bit	Name	Function
D7 ... D0	TEST11	Only for test conditions

Subaddress 12_H: Test Control

Bit	Name	Function
D7 ... D0	TEST12	Only for test conditions

Subaddress 13_H: Test Control

Bit	Name	Function
D7 ... D0	TEST13	Only for test conditions

Subaddress 14_H: PLL Control/VCO and Reference Clock

Bit	Name	Function
D3 ... D0	DIVVCO	PLL-frequency programming, divider of VCO-clock: 0000: 16 0001: not allowed 0010: 2 : : 1111: 15
D7 ... D4	DIVREF	PLL-frequency programming, divider of reference clock: 0000: 16 0001: not allowed 0010: 2 : : 1111: 15

3 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remark
		min.	max.		
Operating temperature	T_A	0	70	°C	
Storage temperature	T_{stg}	-65	125	°C	
Junction temperature	T_j		125	°C	
Soldering temperature	T_S		260	°C	
Soldering time			10	s	
Input voltage	V_I	-0.3 V	V_{DD} + 0.3 V	1	V_{CC} respectively
Output voltage	V_Q	-0.3 V	V_{DD} + 0.3 V	1	V_{CC} respectively
Supply voltages	V_{DD}	-0.3	6	V	
Supply voltage differentials		-0.25	0.25	V	Between any internally non-connected supply pins of the same kind, see Pin Description
DAC output current		-30		mA	For any single output
R_{REF} output current		-30		mA	For any single output
Total power dissipation	P_{tot}		1.7	W	
ESD protection		-2	2	kV	MIL STD 883C method 3015.6, 100 pF, 1500 Ω Except: Pin 36 (SDA) ±300 V
Latch-up protection		-100	100	mA	All inputs/outputs

All voltages listed are referenced to ground (0 V, V_{SS}) except where noted.

***Note**: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions or at any other condition beyond those indicated in the operational sections of this specification is not implied.*

3.1 Recommended Operating Conditions

Parameter	Symbol	Limit Values			Unit	Remark
		min.	nom.	max.		
Supply voltages	V_{DDxx} V_{CCxx}	4.75	5	5.25	V	
Ambient temperature	T_A	0	25	70	°C	
All TTL Inputs						
H-input voltage	V_{IH}	2.0		V_{DD}	V	
L-input voltage	V_{IL}	0		0.8	V	
Serial Clock TTL Input SCA						
SCA clock frequency	f_{SCA}	0.02	27	30	MHz	
SCA low time	t_{LOW}	10			ns	Rise/fall time ≥ 5 ns
SCA high time	t_{HIGH}	10			ns	
Line Locked Clock TTL Input CLL						
CLL clock frequency	f_{CLL}	6	27	30	MHz	
CLL low time	t_{LOW}	10			ns	Rise/fall time ≥ 5 ns
CLL high time	t_{HIGH}	10			ns	
SCA-CLL skew time	t_{SK}	0		15	ns	Diagram on page 40
Digital to Analog Conversion						
DAC sample rate		4.5	54	80	MHz	
R_{REF} output current	I_{REF}	-17	-14	-11	mA	
V_{REF} input voltage	V_{VREF}	1.8	2.1	2.4	V	
I²C Bus (All Values are Referred to min.(V_{IH}) and max.(V_{IL}))						
H-input voltage	V_{IH}	3		V_{DD}	V	
L-input voltage	V_{IL}	0		1.5	V	
SCL clock frequency	f_{SCL}	0		100	kHz	
Inactive time before start of transmission	t_{BUF}	4.7			µs	
Set-up time start condition	$t_{SU;STA}$	4.7			µs	
Hold time start condition	$t_{HD;STA}$	4.0			µs	
SCL low time	t_{LOW}	4.7			µs	

3.1 Recommended Operating Conditions (cont'd)

Parameter	Symbol	Limit Values			Unit	Remark
		min.	nom.	max.		
SCL high time	t_{HIGH}	4.0			µs	
Set-up time DATA	$t_{SU;DAT}$	250			µs	
Hold time DATA	$t_{HD;DAT}$	0			µs	
SDA/SCL rise times	t_R			1	µs	
SDA/SCL fall times	t_F			300	ns	
Set-up time stop condition	$t_{SU;STO}$	4.7			µs	
L-output current	I_{OL}			3	mA	

3.2 Characteristics (Assuming Recommended Operating Conditions)

Parameter	Symbol	Limit Values		Unit	Remark
		min.	max.		
Average supply current	I_{CC}		320	mA	All V_{CC} and V_{DD} pins
All Digital Inputs (Including I/O Inputs)					
Input capacitance	C_I		10	pF	Not tested; max. 7 pF for SCA, CLL
Input leakage current	$I_{I(L)}$	-10	10	µA	
TTL Inputs: YUV, UV, V (Referenced to SCA); BLN, INS (Referenced To CLL)					
Set-up time	t_{SU}	7		ns	See timing diagram 5.1 on page 40
Input hold time	t_{IH}		6	ns	See timing diagram 5.1 on page 40
TTL Inputs: VS, HS, RES (Asynchronous to any Clock)					
VS low time	t_{LOW}	4		µs	
VS high time	t_{HIGH}	4		µs	
HS low time	t_{LOW}	12		1	CLL periods
HS high time	t_{HIGH}	12		1	CLL periods
RES low time	t_{LOW}	100		ns	For reliable reset
Input/Output: SDA (Referenced to SCL; Open Drain Output)					
Low-level output voltage	V_{OL}		0.5	V	At I_{OL} = max
PLL: Pin LF (Analog)					
Loop filter charge Pump current		150	800	µA	V_{LF} = 2 V
		-800	-150	µA	V_{LF} = 2 V
Digital to Analog Conversion (9 Bit): Current Source Outputs YQ, UQ, VQ					
Full range output current	I_{OFR}	-19.5	-16.5	mA	V_{VREF} = nom, T_A = nom, I_{REF} = nom, R_L = 75 Ω
Full range output current matching		-1	1	mA	V_{VREF} = nom, T_A = nom, I_{REF} = nom, R_L = 75 Ω
Temperature dependency of I_{OFR}		-10	10	µA/°C	Not tested; V_{VREF} = nom, I_{REF} = nom, R_L = 75 Ω

3.2 Characteristics (Assuming Recommended Operating Conditions) (cont'd)

Parameter	Symbol	Limit Values		Unit	Remarky
		min.	max.		
Supply voltage dependency of I_{OFR}		-0.2	0.2	mA/V	V_{VREF} = nom, T_A = nom, I_{REF} = nom, R_L = 75 Ω
Current source output resistance		20		kΩ	Not tested; V_{VREF} = nom, T_A = nom, I_{REF} = nom
Full range output voltage			1.6	V	V_{VREF} = nom, T_A = nom, I_{REF} = nom, ||LE| ≤ max
DC differential nonlinearity	DLE	-1	1	LSB	
DC integral nonlinearity	ILE	-2	2	LSB	
DAC Reference Pins: V_{REF}, R_{REF} (Analog)					
Offset voltage between V_{REF} and R_{REF}	V_{VREF} - V_{RREF}	-40	40	mV	
V_{REF} input current		-10	10	µA	

4 Application Information

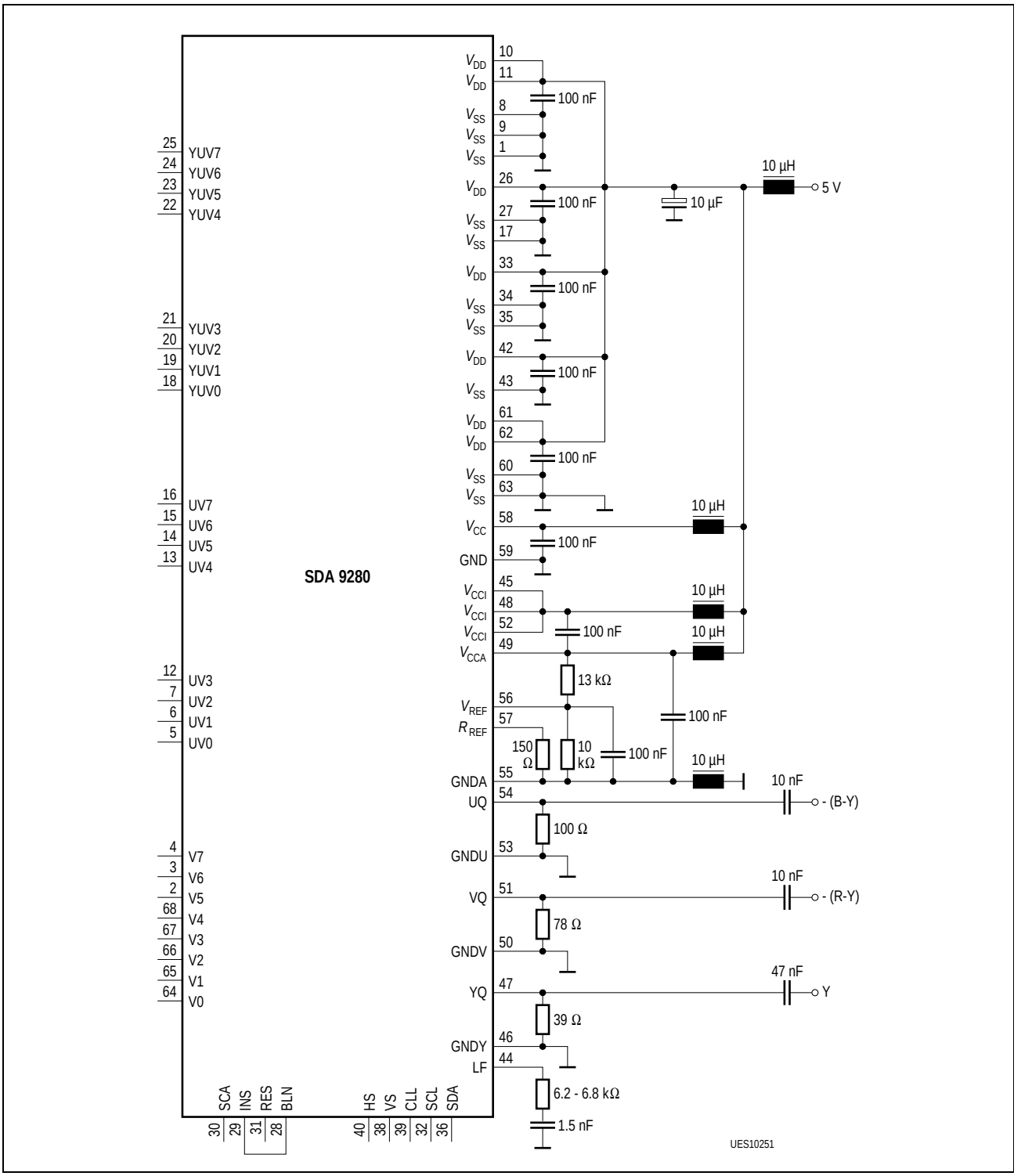


Figure 8

This application circuit is part of a Siemens MEGAVISION® application

***Note**: The input data format must be selected via I^2C Bus. Input data pins which are not used for the selected format should be connected to GND.*

Block Diagram of Standard Version

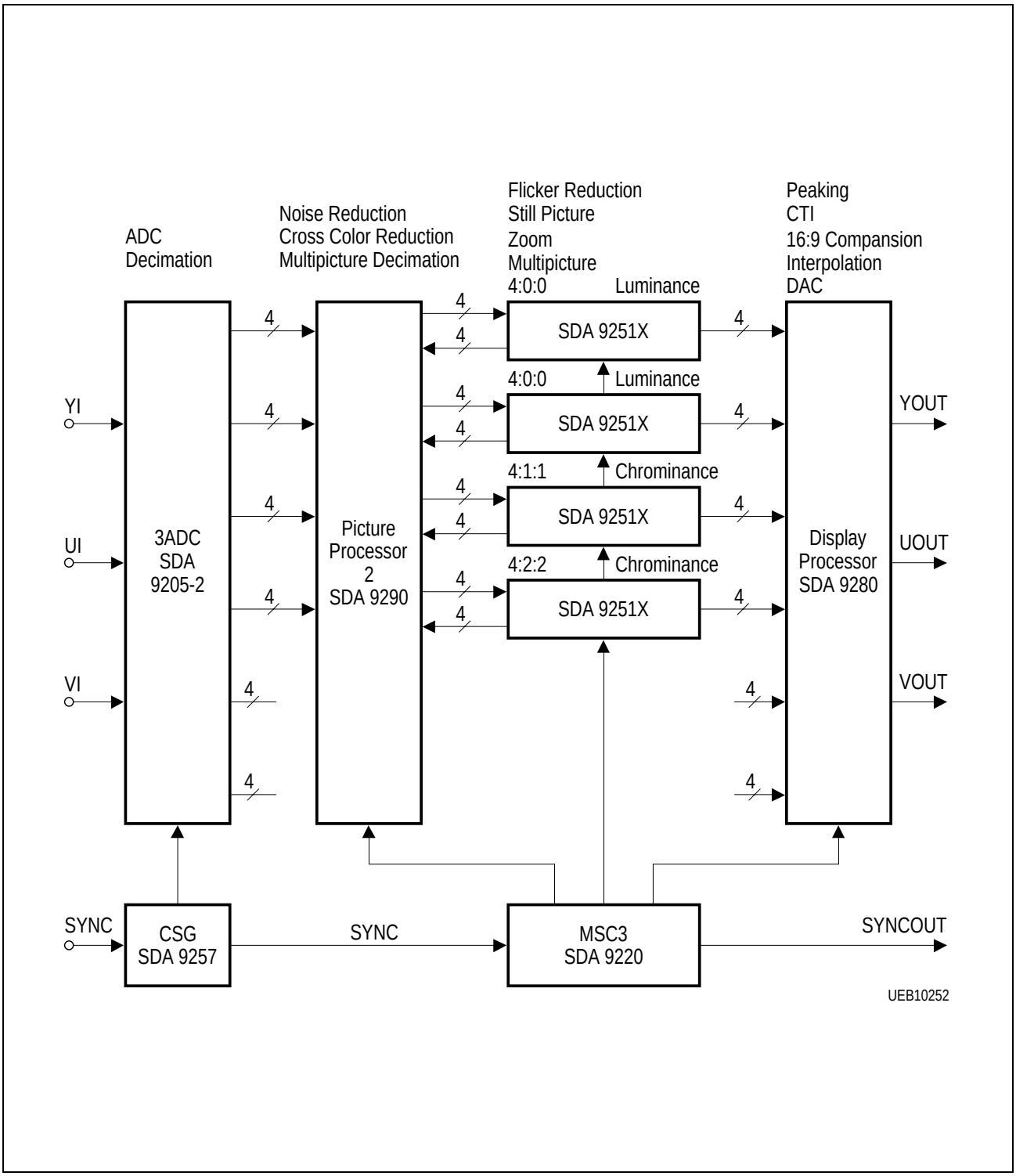


Figure 9

5 Waveforms

5.1 Timing Diagram Data Input Referenced to the Clock

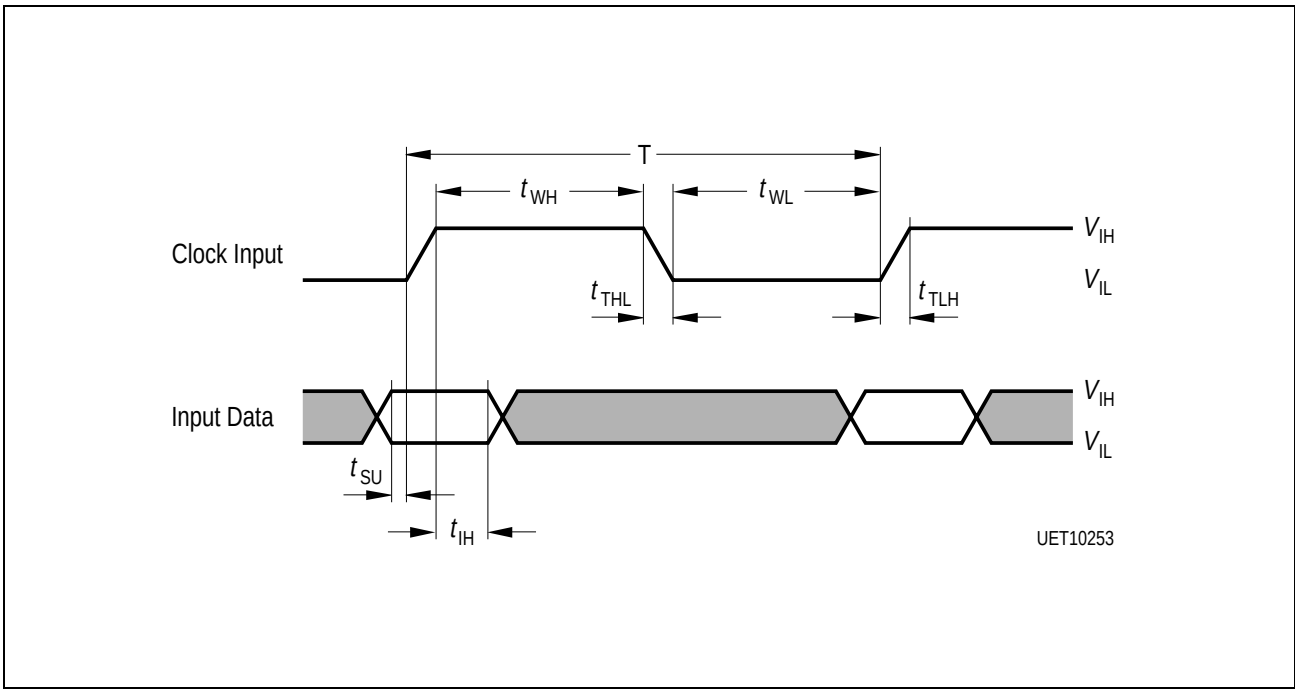


Figure 10

5.2 Timing Diagram Clock Skew SCA-CLL

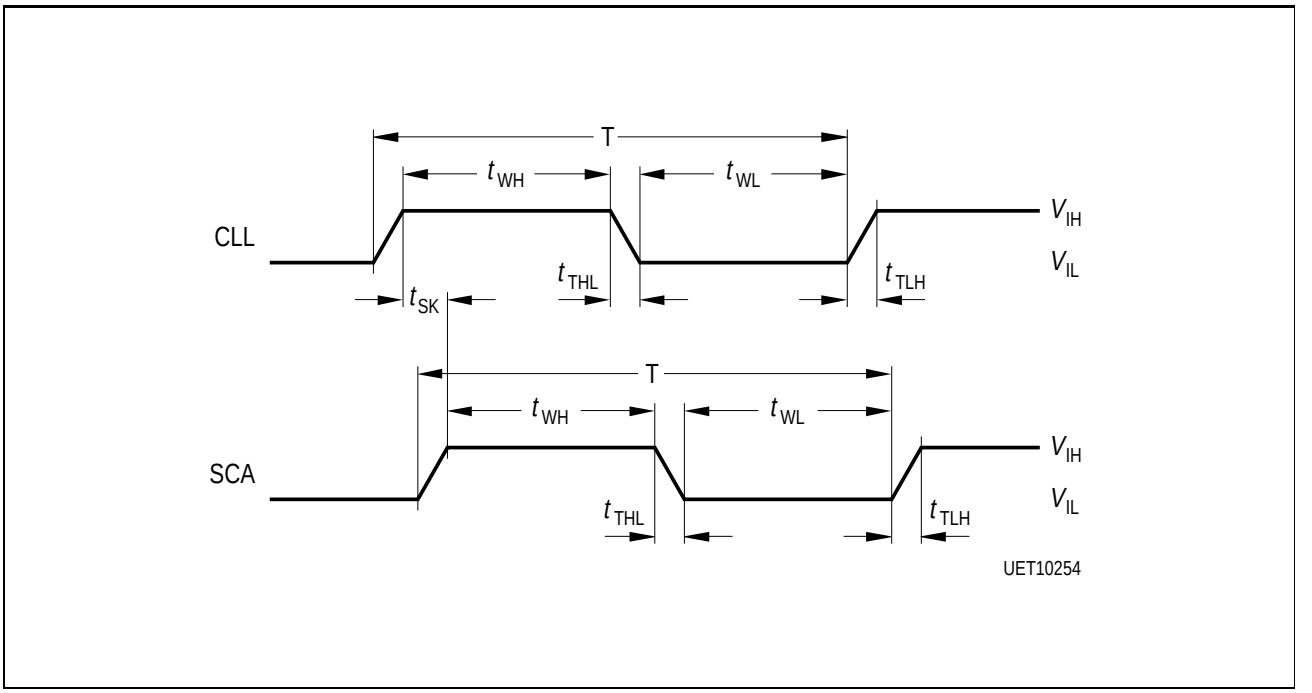


Figure 11

5.3 Input Data Format 4:1:1

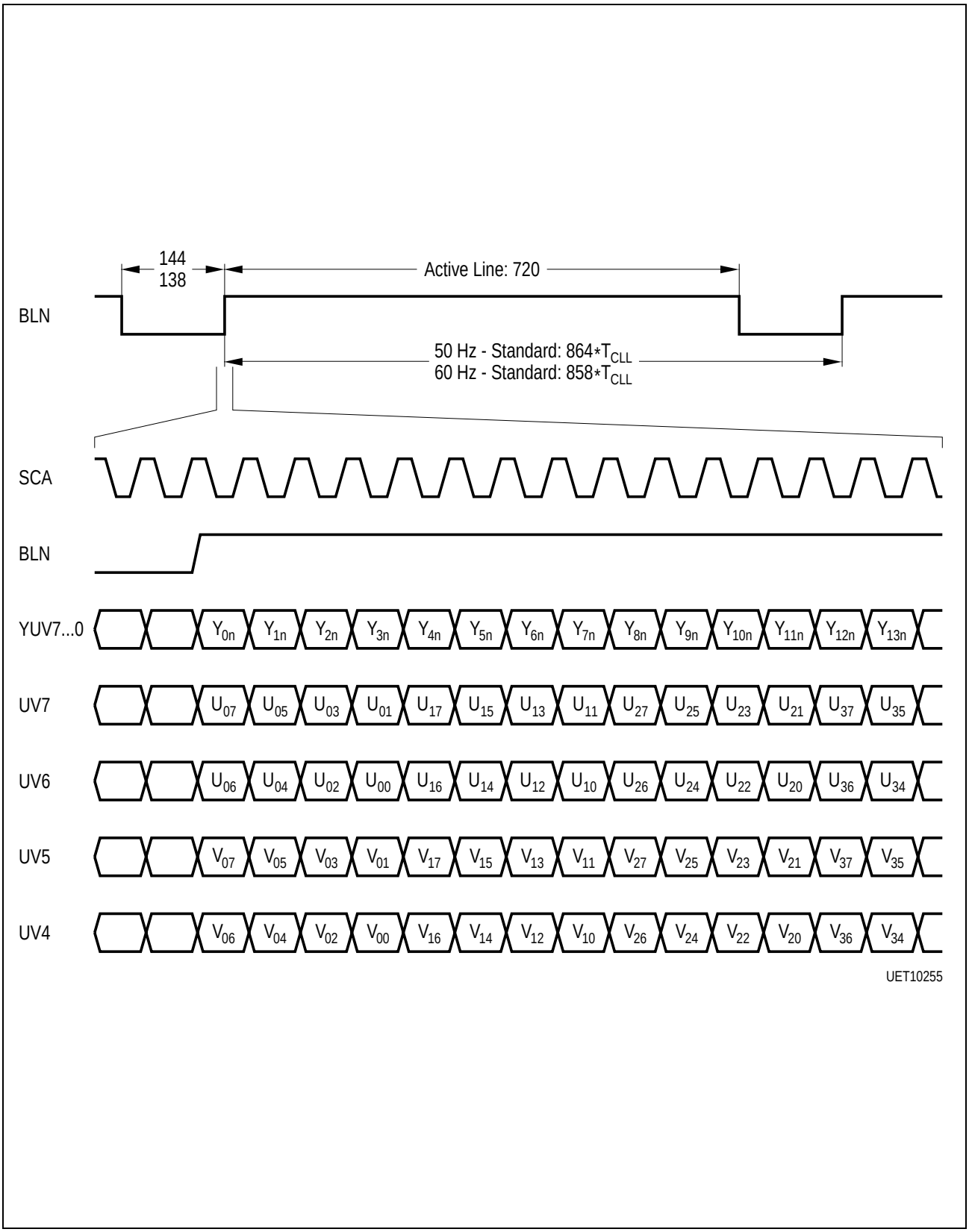


Figure 12

5.4 Input Data Format 4:2:2 Parallel

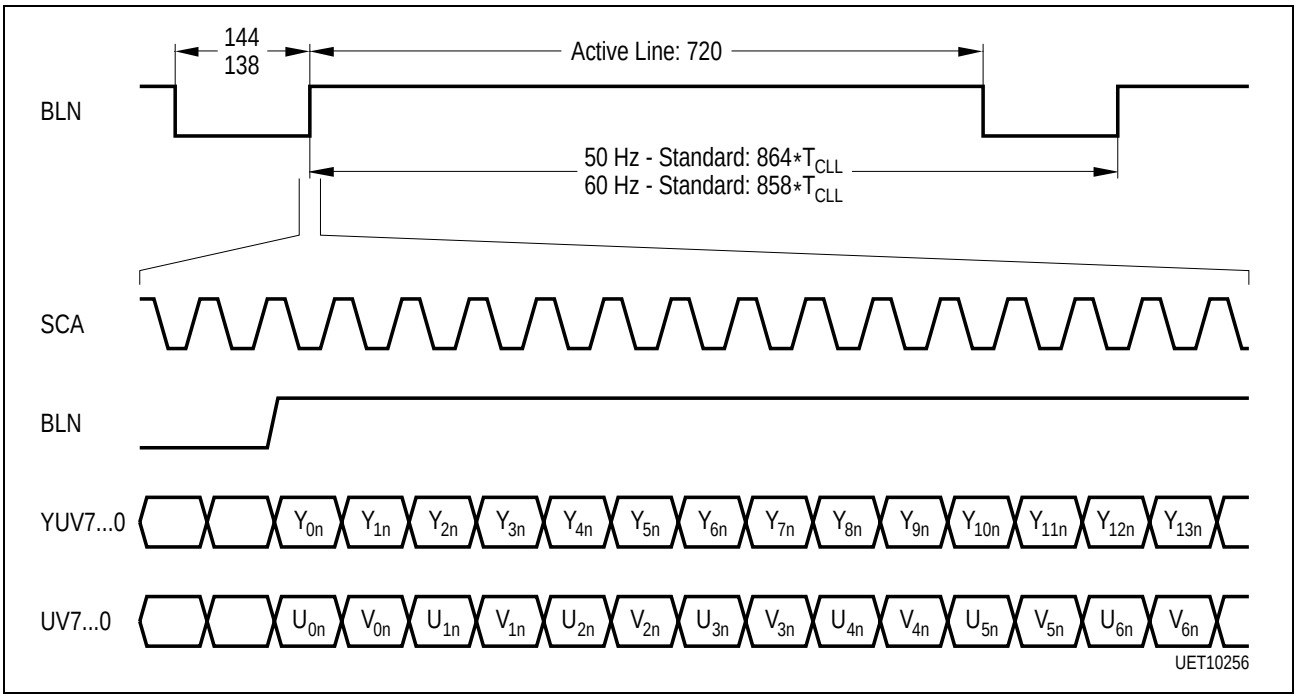


Figure 13

5.5 Input Data Format CCIR 656

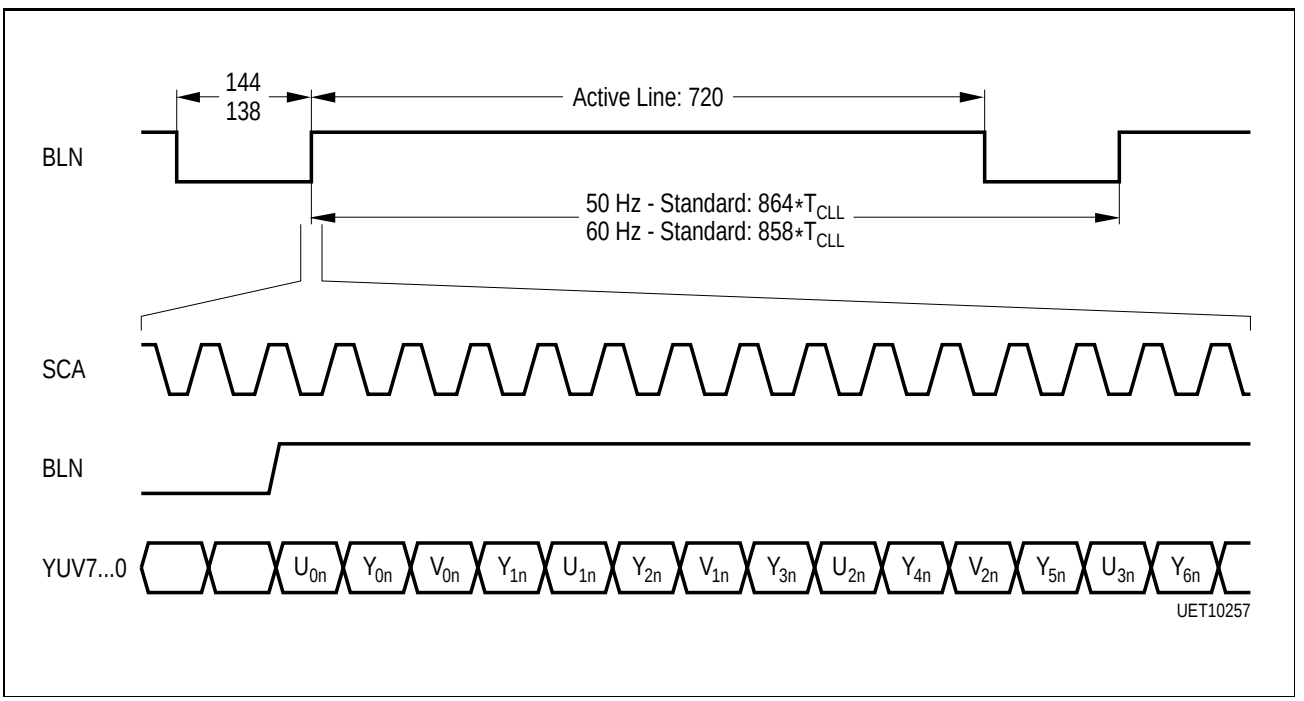
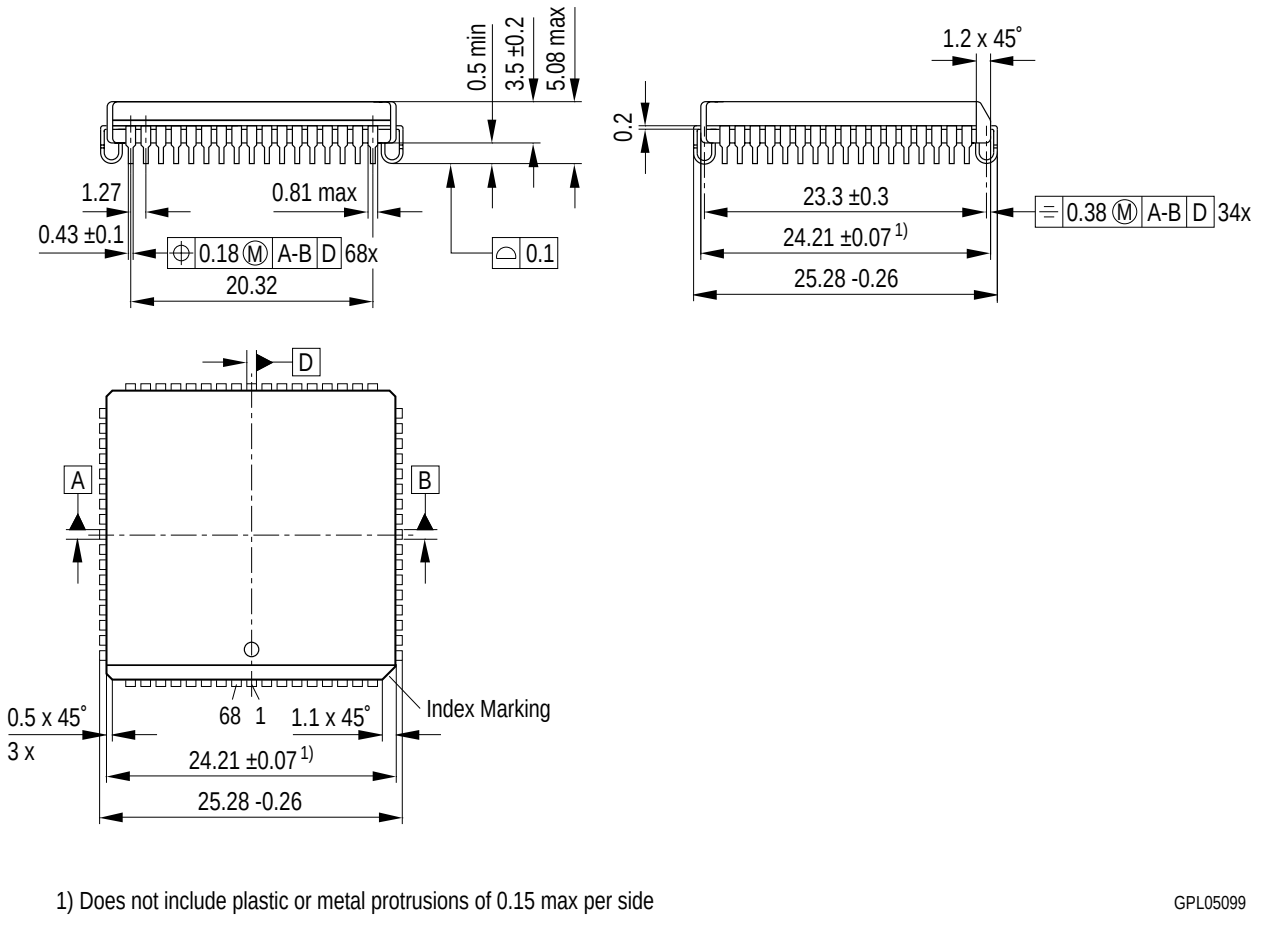


Figure 14

***Note**: X_{AB}: X: signal component A: sample number B: Bit number*

6 Package Outlines

P-LCC-68-1
(Plastic Leaded Chip Carrier)



1) Does not include plastic or metal protrusions of 0.15 max per side

GPL05099

Figure 15

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm