SILICON CONNECTIONS CORPORATION

PRELIMINARY

SC5104 - 64K X 4 BiCMOS ECL I/O STATIC RAM

GENERAL DESCRIPTION

Silicon Connection's SC5104 is a fully static, asyncronous random access memory, organized 65,536 words by 4 bits. The device is built using SCC's 1.0 micron BiCMOS and features advanced circuit techniques that result in 12 nS access times.

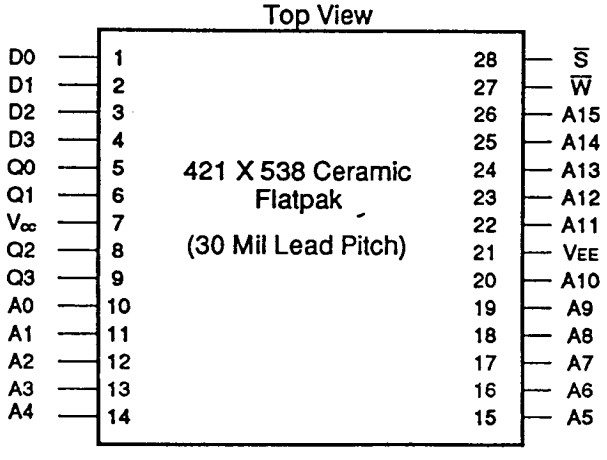
Writing and reading the memory is accomplished via industry standard timing and signals. To write the memory the device must first be selected ($\overline{S}$ pulled LOW) while enabling a write cycle ($\overline{W}$ pulled LOW). Data on the input pins (D0 - D3) will then be written into the memory address specified on the address pins (A0 - A15).

To read the memory the device is selected ($\overline{S}$ pulled LOW) while the write enable ($\overline{W}$) remains in the HIGH state. This will allow the memory contents of the current address (A0 - A15) to be presented on output pins Q0 - Q3. The output pins (Q0 - Q3) will remain LOW (inactive) if either the chip select ($\overline{S}$) is HIGH or write enable ($\overline{W}$) is LOW.

FEATURES

- **12 nS/15 nS speed grades**
- **Power Supply -5.2V ± 10%**
- **100K compatible ECL I/O's**
- **Balanced read and write cycle times**
- **Up to 33% of write cycle timing is allowed for system skews**
- **Power dissipation <1.1W**
- **Soft Error rate less than 100 FITs**
- **ESD protection greater than 2000 V with latch-up immunity > 200 mA**
- **High density, high performance 28-pin flatpack**
- **1.0 micron BICMOS Technology**

Top View



Pin Names

A0 - A15	Address Inputs
$\overline{S}$	Chip Select
Q0 - Q3	Data Outputs
D0 - D3	Data Inputs
$\overline{W}$	Write Enable
VEE	Power
Vcc	Ground

Absolute Maximum Ratings

Storage Temperature ..... -65°C to +150°C
VEE Pin Potential to Ground ..... -7.0V to +0.5V
Input Voltage (DC) ..... V_{EE} to +0.5V
Static Discharge Voltage ..... >2000V
Maximum Junction Temperature ..... +150°C
Output Current (DC Output High) ..... -50 mA
Latch-up Current ..... >200 mA

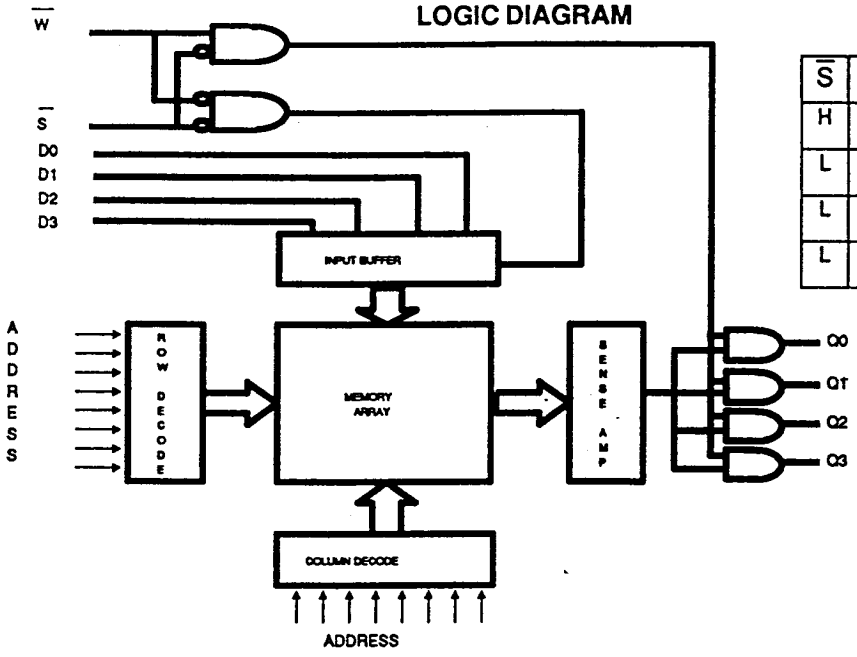
AC Test Conditions

Input Rise and Fall Times ..... 0.7 nS
Output Timing Reference ..... 50% of Input
Input Pulse Levels ..... Figure 1
AC Test Circuit ..... Figure 2

Capacitance

Input Pin (C_{IN}) ..... 5.0 pF
Output Pin (C_{OUT}) ..... 8.0 pF

LOGIC DIAGRAM



TRUTH TABLE

$\overline{S}$	$\overline{W}$	D	Q	MODE
H	X	X	L	NOT SELECTED
L	L	L	L	WRITE "0"
L	L	H	L	WRITE "1"
L	H	X	Q	READ

DC Electrical Characteristics

V_{EE} = -5.2V ± 10%, V_{CC} = Ground, T_C = 0°C to +85°C

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output HIGH Voltage	V_{IN} = $V_{IH(MAX)}$ or $V_{IL(MIN)}$	-1025	-880	mV
V_{OL}	Output LOW Voltage	Loading with 50 ohms to -2.0V	-1810	-1620	mV
V_{IH}	Input HIGH Voltage		-1165	-880	mV
V_{IL}	Input LOW Voltage		-1810	-1475	mV
V_{OHC}	Output HIGH Voltage	V_{IN} = $V_{IH(MIN)}$ or $V_{IL(MAX)}$	-1025		mV
V_{OLC}	Output LOW Voltage	Loading with 50 ohms to -2.0V		-1620	mV
I_{IH}	Input HIGH Current	V_{IN} = $V_{IH(MAX)}$		220	uA
I_{IL}	Input LOW Current	V_{IN} = $V_{IL(MAX)}$	-50	170	uA
I_{EE}	Power Supply Current	f_o = 50 MHz	-250		mA

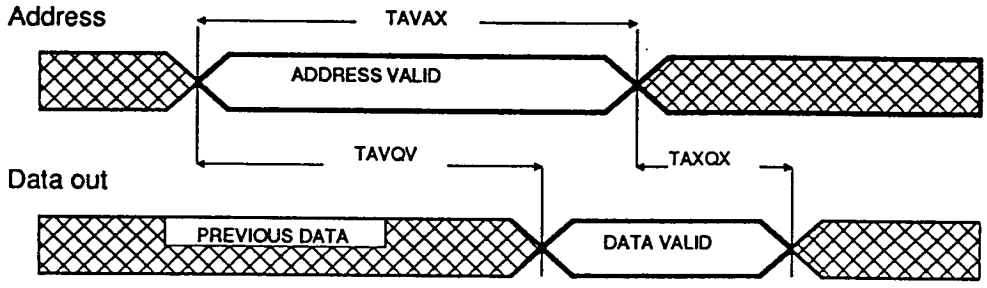
Read Cycle

AC Timing Characteristics

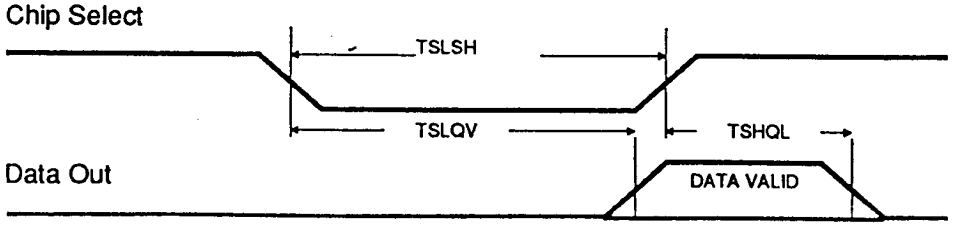
V_{EE} = -5.2V ± 10%, V_{CC} = Ground, T_C = 0°C to +85°C

		SC5104-12		SC5104-15		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
TAVAX	Address Valid to Address Invalid	12		15		nS
TAVQV	Address Valid to Output Valid		12		15	nS
TAXQX	Address Invalid to Output Invalid	3	8	3	10	nS
TSLSH	Chip Select LOW to Chip Select HIGH	7		7		nS
TSLQV	Chip Select LOW to Output Valid		4		4	nS
TSHQL	Chip Select HIGH to Output LOW		4		4	nS

Read Cycle 1 Chip Select is active prior to or within TAVQV-TSLQV after address valid



Read Cycle 2 Address is valid a minimum of TAVQV-TSLQV prior to Chip Select becoming active



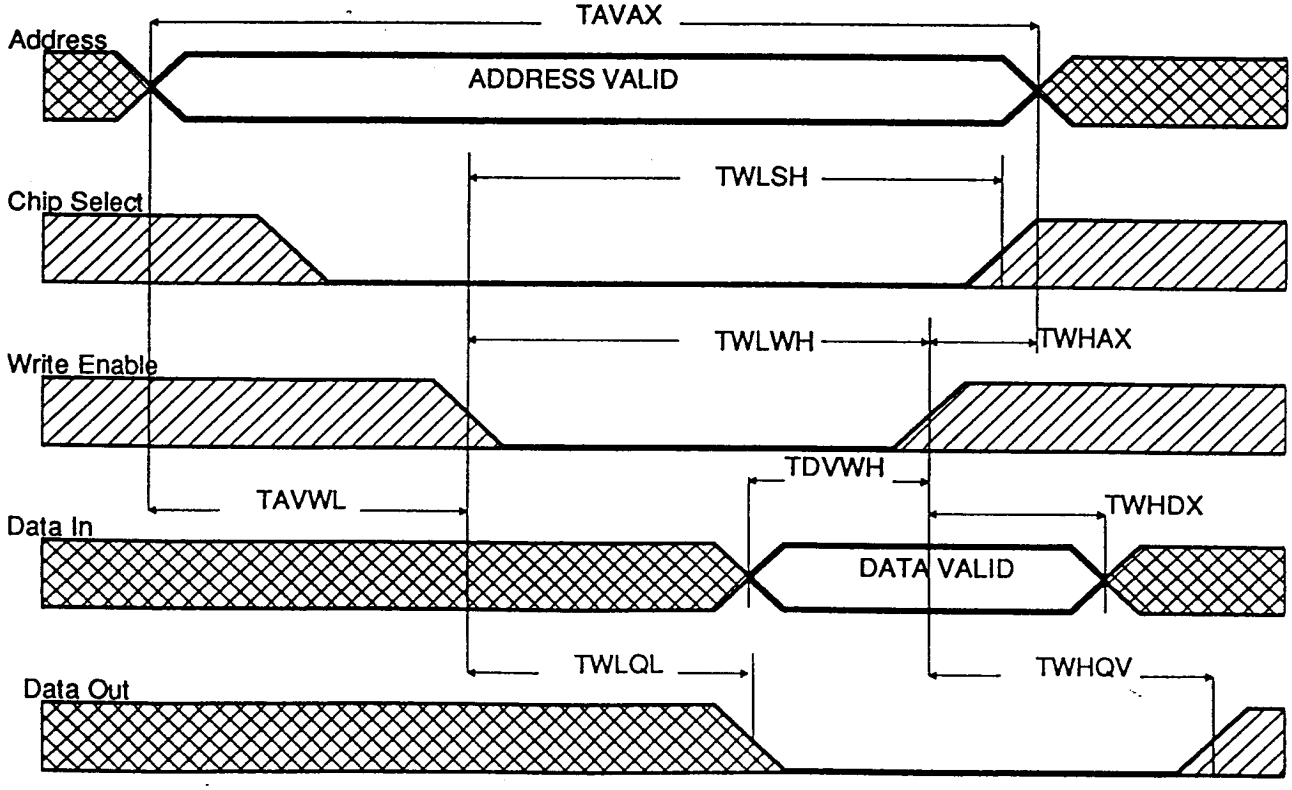
Write Cycle 1

Write Cycle 1 is $\overline{W}$ controlled. This is established by $\overline{S}$ being held active (LOW) prior to $\overline{W}$ becoming active (LOW). TWLQL must be observed in Write Cycle 1 in order to avoid data bus contention in common I/O applications. At the end of Write Cycle 1 data out may become active if W becomes inactive (HIGH) prior to S becoming inactive (HIGH)

AC Timing Characteristics

V_{EE} = -5.2V ± 10%, V_{CC} = Ground, T_C = 0°C to +85°C

		SC5104-12		SC5104-15		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
TAVAX	Address Valid to Address Invalid	12		15		nS
TWLSH	Write Enable LOW to Chip Select HIGH	8		10		nS
TWHAX	Write HIGH to Address Don't Care	0		0		nS
TWLWH	Write LOW to Write HIGH	8		10		nS
TAVWL	Address Valid to Write LOW	0		0		nS
TDVWH	Data Valid to Write HIGH	8		10		nS
TWHDX	Write HIGH to Data Don't Care	0		0		nS
TWLQL	Write LOW to Output LOW		4		4	nS
TWHQV	Write HIGH to Output Valid		12		15	nS



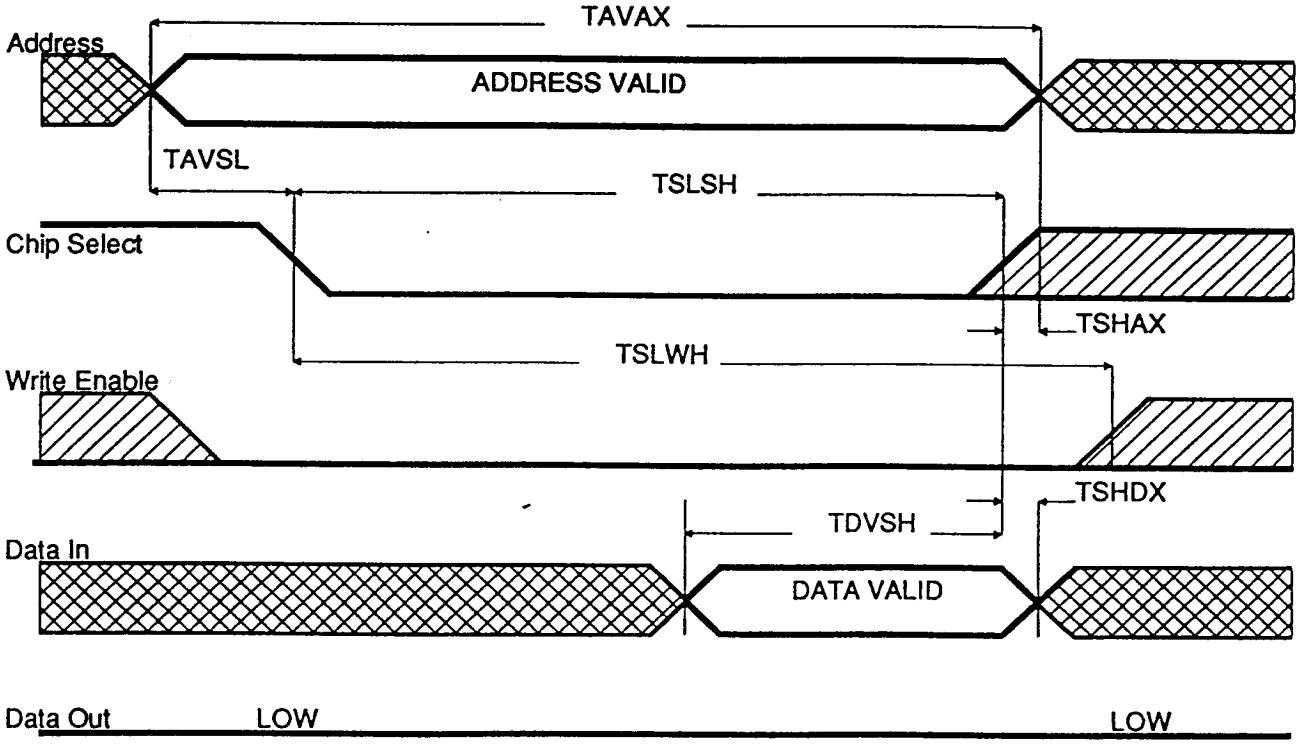
Write Cycle 2

Write Cycle 2 is $\overline{S}$ controlled. This is established by $\overline{W}$ being active coincident with or prior to $\overline{S}$ becoming active (LOW). This cycle has identical specifications to Write Cycle 1 with the exceptions of S and W being interchanged. For common I/O applications this cycle may be more appropriate, as the data bus restrictions are eliminated.

AC Timing Characteristics

V_{EE} = -5.2V ± 10%, V_{CC} = Ground, T_C = 0°C to +85°C

		SC5104-12		SC5104-15		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
TAVSL	Address Valid to Chip Select LOW	0		0		nS
TSLSH	Chip Select LOW to Chip Select HIGH	8		10		nS
TSHAX	Chip Select HIGH to Address Don't Care	0		0		nS
TSLWH	Chip Select LOW to Write Enable HIGH	8		10		nS
TDVSH	Data Valid to Chip Select HIGH	8		10		nS
TSHDX	Chip Select HIGH to Data Don't Care	0		0		nS

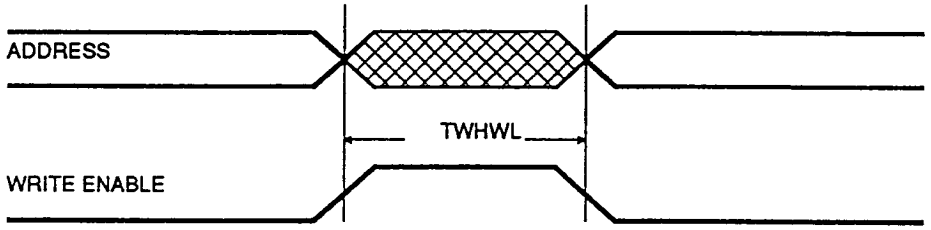


Consecutive Write Cycles
AC Timing Characteristics

V_{EE} = -5.2V ± 10%, V_{CC} = Ground, T_C = 0°C to +85°C

		SC5104-12		SC5104-15		
Symbol	Parameter	Min	Max	Min	Max	Units
TWHWL	Write Enable HIGH to Write Enable LOW	4		4		nS
TSHSL	Chip Select HIGH to Chip Select LOW	4		4		nS

Minimum Write Pulse Disable



Minimum Select Pulse Disable

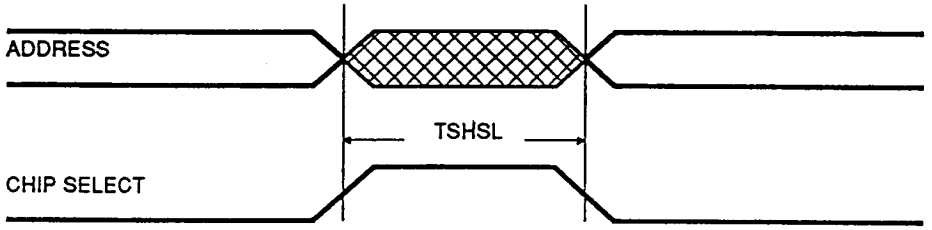
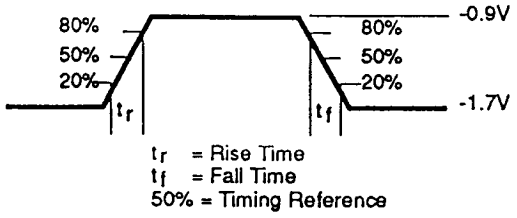


FIGURE 1



tr = Rise Time
tf = Fall Time
50% = Timing Reference

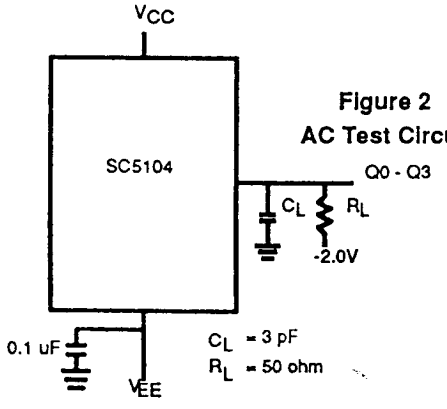
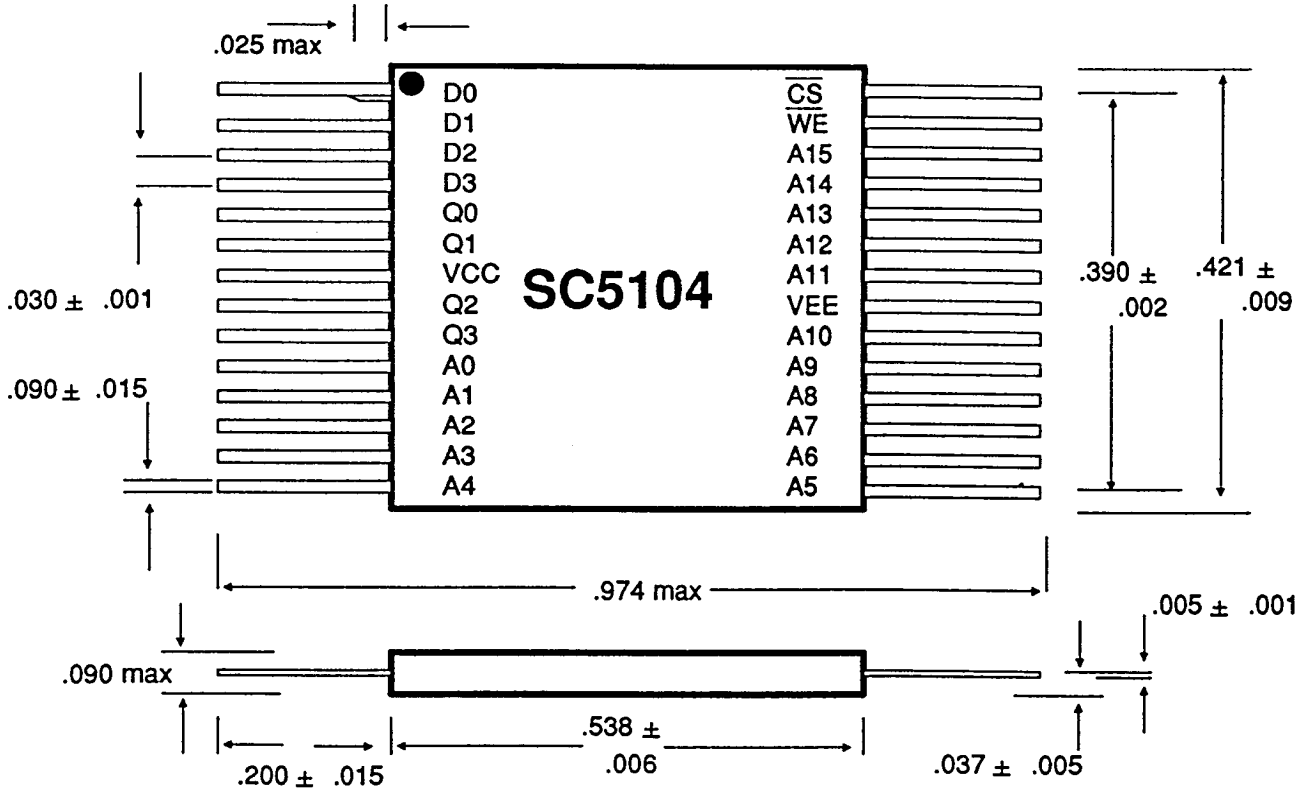


Figure 2
AC Test Circuit

Package

Flat Pack



Ordering Codes

Package Type	Part Number
28 Pin Ceramic Flatpack	SC5104F-12/15
28 Pin Ceramic Dual-In-Line Package	SC5104D-12/15

Order Placement

Attention: Order Entry

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