

25A, 50V, 0.047 Ohm, N-Channel Power MOSFET

The RFP25N05 N-channel power MOSFET is manufactured using the MegaFET process. This process which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. It was designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. This transistor can be operated directly from integrated circuits.

Formerly developmental type TA09771.

Ordering Information

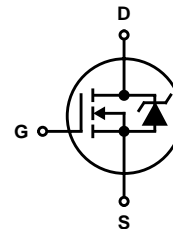
PART NUMBER	PACKAGE	BRAND
RFP25N05	TO-220AB	RFP25N05

NOTE: When ordering use the entire part number.

Features

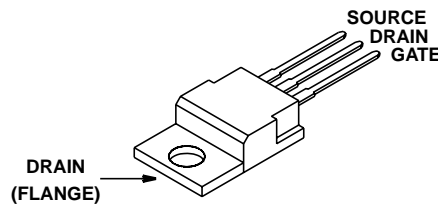
- 25A, 50V
- $r_{DS(ON)} = 0.047\Omega$
- Temperature Compensating PSPICE® Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

JEDEC TO-220AB



RFP25N05

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	RFP25N05	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	50 V
Drain to Gate Voltage	V_{DGR}	50 V
Gate to Source Voltage	V_{GS}	± 20 V
Continuous Drain Current	I_D	25 A
Pulsed Drain Current (Note 3)	I_{DM}	Refer to Peak Current Curve A
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve
Maximum Power Dissipation	P_D	72 W
Linear Derating Factor		0.48 $W/^\circ\text{C}$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175 $^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300 $^\circ\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg}	260 $^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^\circ\text{C}$ to 150°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$ (Figure 11)	50	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\text{mA}$ (Figure 10)	2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}$	-	-	1	μA
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}, T_C = 150^\circ\text{C}$	-	-	25	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 25\text{A}, V_{GS} = 10\text{V}$ (Figure 9)	-	-	0.047	Ω
Turn-On Time	t_{ON}	$V_{DD} = 25\text{V}, I_D \approx 12.5\text{A}, R_L = 2.0\Omega,$ $V_{GS} = 10\text{V}, R_G = 10\Omega$ (Figure 13)	-	-	60	ns
Turn-On Delay Time	$t_{d(ON)}$		-	14	-	ns
Rise Time	t_r		-	30	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	45	-	ns
Fall Time	t_f		-	22	-	ns
Turn-Off Time	t_{OFF}		-	-	100	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0\text{V}$ to 20V	-	-	80	nC
Gate Charge at 10V	$Q_{G(10)}$	$V_{GS} = 0\text{V}$ to 10V				
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0\text{V}$ to 2V				
Input Capacitance	C_{ISS}	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$ (Figure 12)	-	1075	-	pF
Output Capacitance	C_{OSS}		-	350	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	100	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)	-	-	2.083	$^\circ\text{C/W}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$		-	-	80	$^\circ\text{C/W}$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	$I_{SD} = 25\text{A}$	-	-	1.5	V
Reverse Recovery Time	t_{RR}	$I_{SD} = 25\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	125	ns

NOTES:

2. Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3) and Peak Current Capability Curve (Figure 5).

Typical Performance Curves

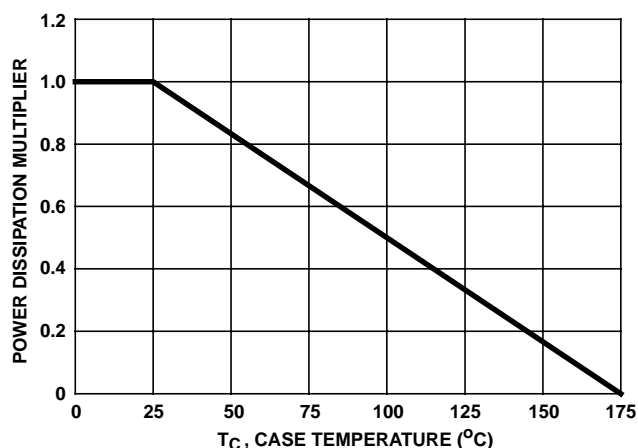


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

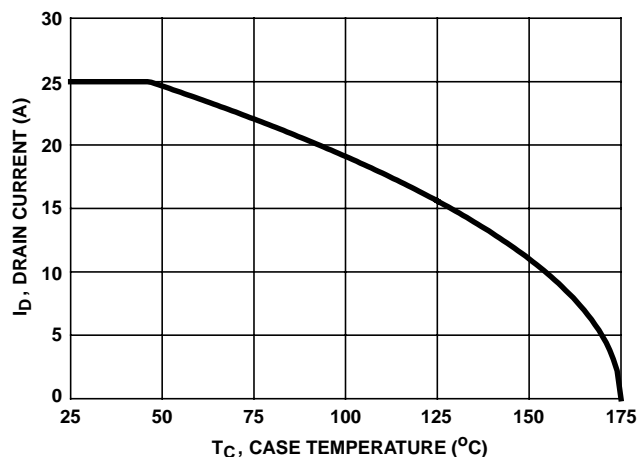


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

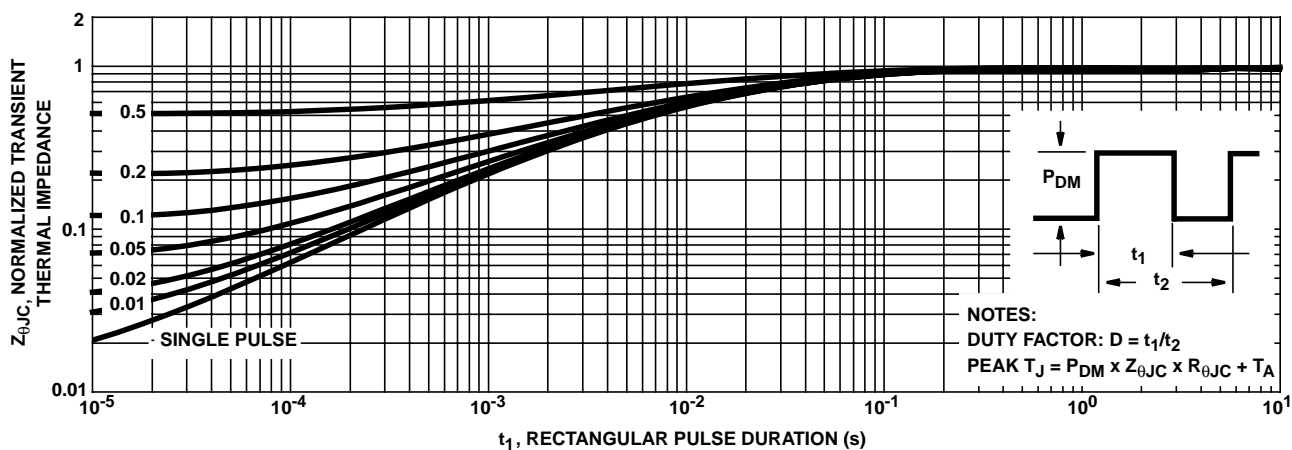


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

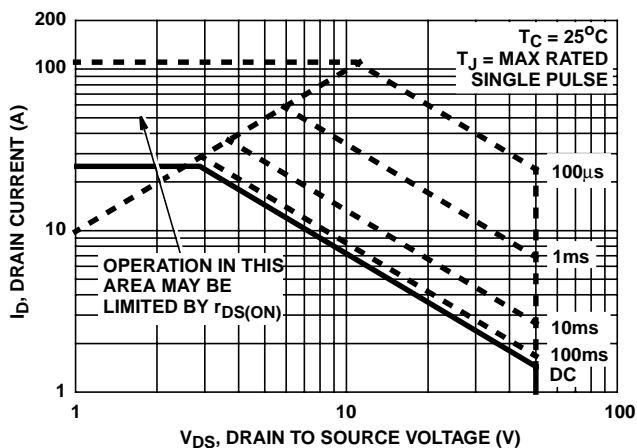


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

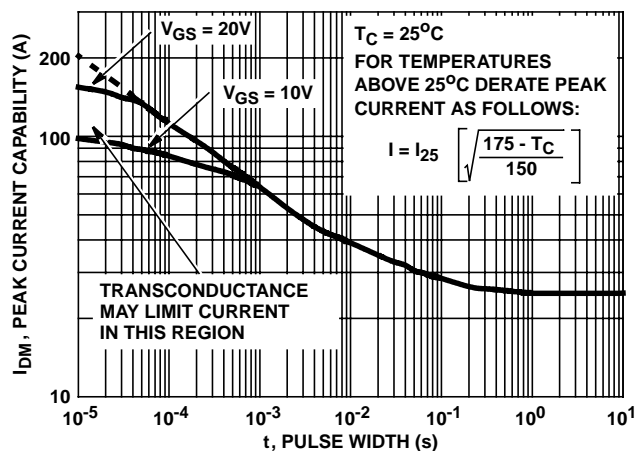
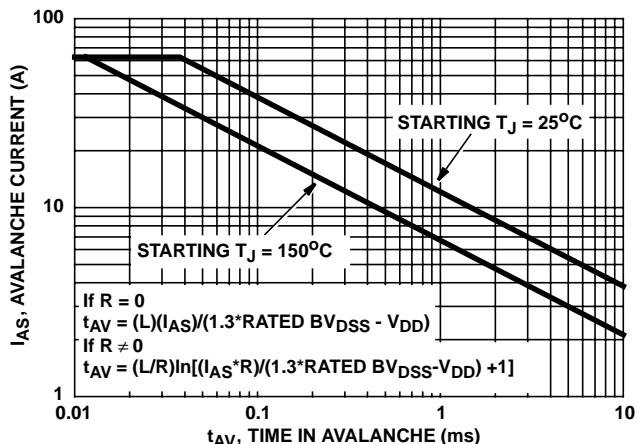


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.
FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

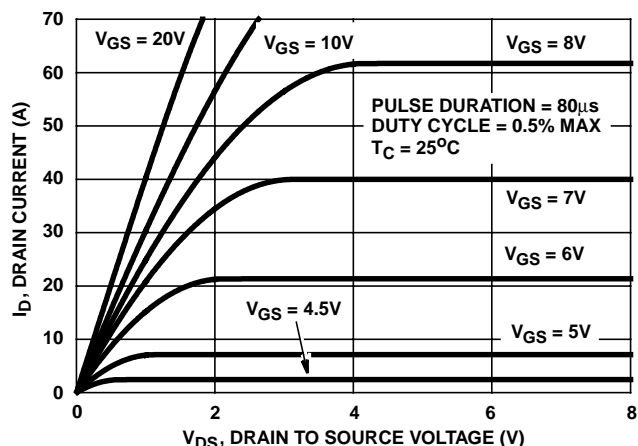


FIGURE 7. SATURATION CHARACTERISTICS

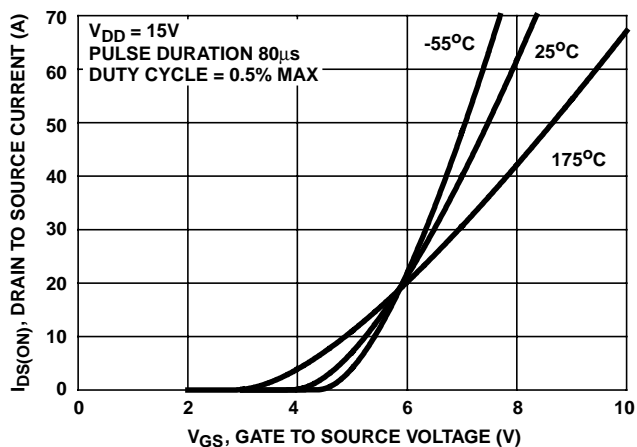


FIGURE 8. TRANSFER CHARACTERISTICS

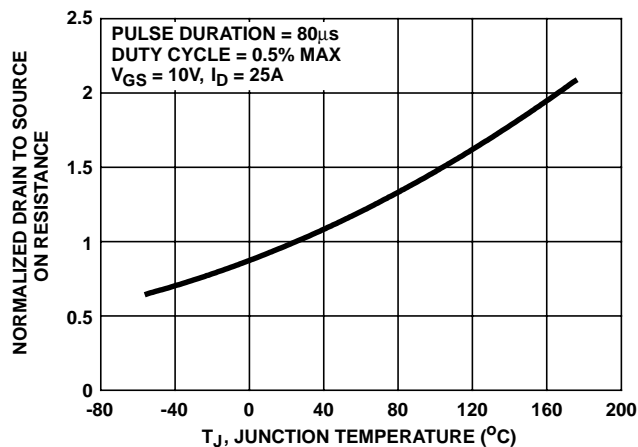


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

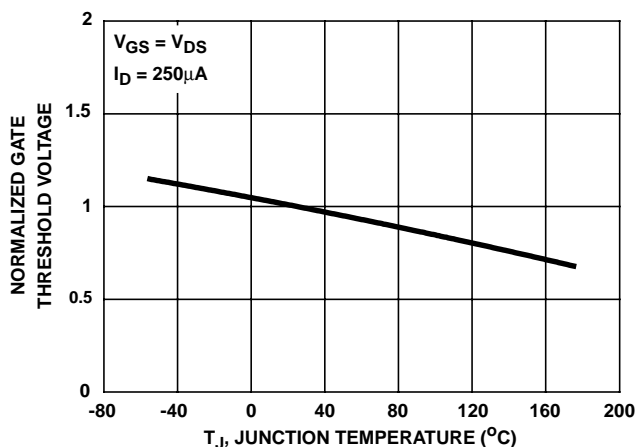


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

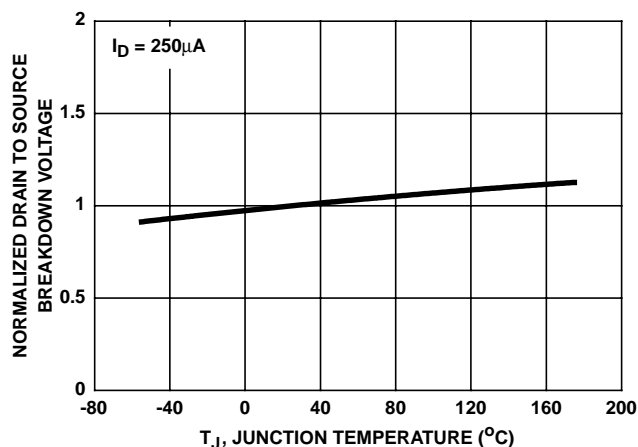


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

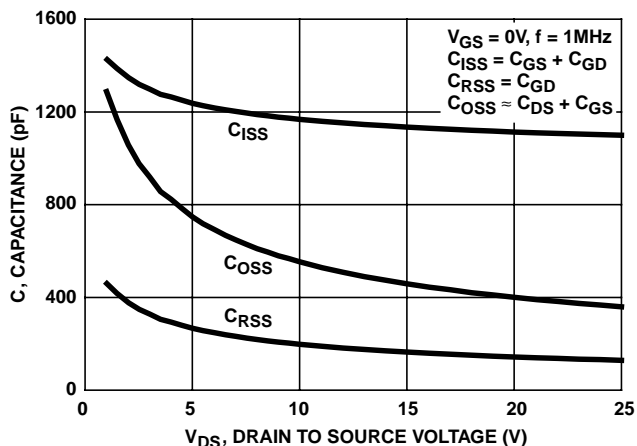
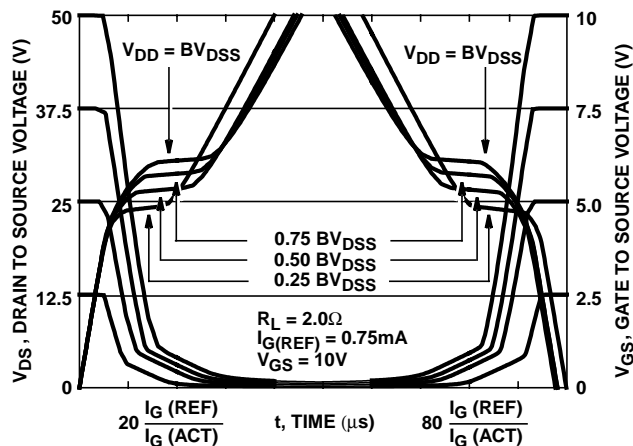


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 13. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

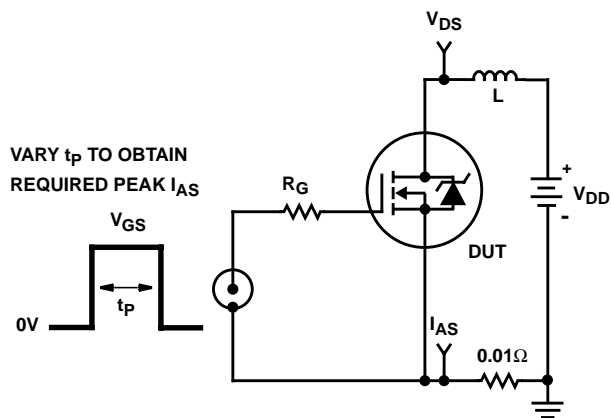


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

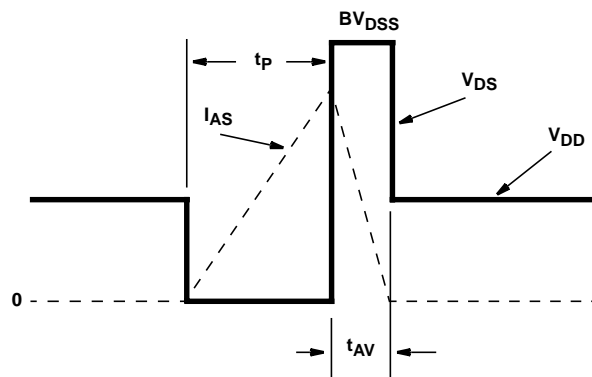


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

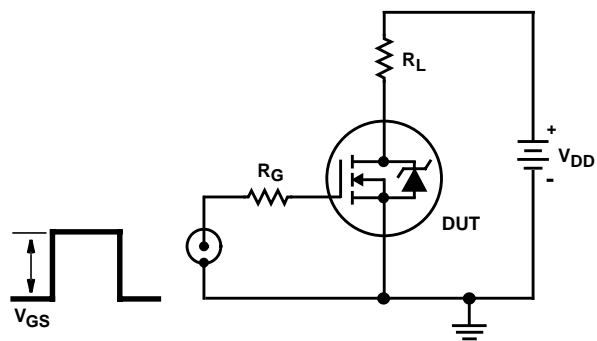


FIGURE 16. SWITCHING TIME TEST CIRCUIT

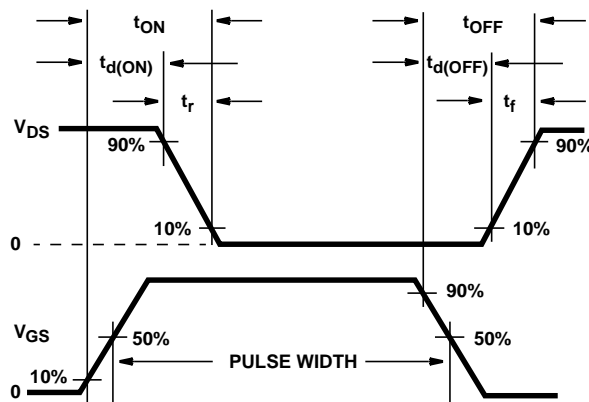


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

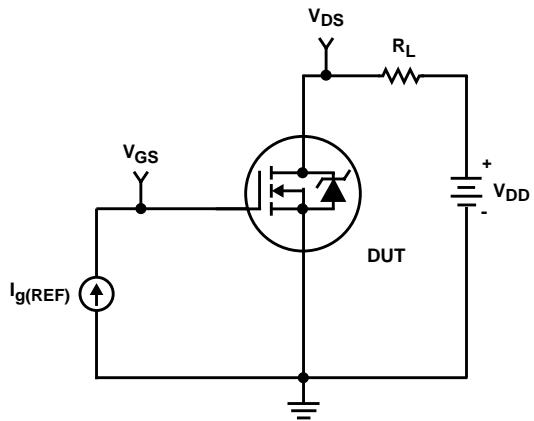


FIGURE 18. GATE CHARGE TEST CIRCUIT

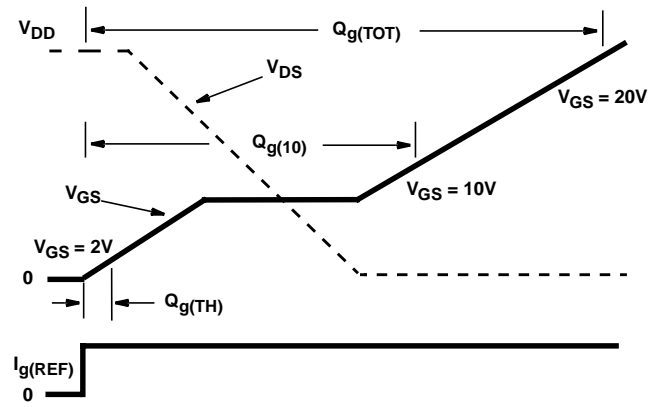


FIGURE 19. GATE CHARGE WAVEFORM

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