Section 20 Electrical Characteristics

20.1 Absolute Maximum Ratings

Table 20.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage	V_{CC}	–0.3 to +7.0	V
Program voltage	V_{PP}	–0.3 to +13.5	V
Input voltage (except port C)	Vin	–0.3 to V_{CC} + 0.3	V
Input voltage (port C)	Vin	–0.3 to AV_{CC} + 0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +7.0	V
Analog reference voltage	AV_{ref}	–0.3 to AV_{CC} + 0.3	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} + 0.3	V
Operating temperature	Topr	–20 to +75*	°C
Storage temperature	Tstg	–55 to +125	°C

Caution: Operating the LSI in excess of the absolute maximum rating may result in permanent damage.

Note: Normal Products: Topr = –40 to +85°C for wide-temperature range products

20.2 DC Characteristics

Table 20.2 lists DC characteristics. Table 20.3 lists the permissible output current values.

Usage Conditions:

- Do not release AV_{CC}, AV_{ref} and AV_{SS} when the A/D converter is not in use. Connect AV_{CC} and AV_{ref} to V_{CC} and AV_{SS} to V_{SS}.
- The current consumption value is measured under conditions of V_{IH} min = V_{CC} – 0.5 V and V_{IL} max = 0.5 V with no load on any output pin and the on-chip pull-up MOS off.
- Even when the A/D converter is not used or is stand-by, connect AV_{CC} to AV_{ref} the power voltage(V_{CC}).

Table 20.2 DC Characteristics (1)

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 20 MHz, Ta = –20 to +75°C*)

Normal Products: Ta = –40 to +85°C for wide-temperature range products.

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions
Input high-level voltage	$\overline{RES}$, NMI, MD2–MD0	V_{IH}	V_{CC} – 0.7	—	V_{CC} + 0.3	V	
	EXTAL		V_{CC} × 0.7	—	V_{CC} + 0.3	V	
	Port C		2.2	—	AV_{CC} + 0.3	V	
	Other input pins		2.2	—	V_{CC} + 0.3	V	
Input low-level voltage	$\overline{RES}$, NMI, MD2–MD0	V_{IL}	–0.3	—	0.5	V	
	Other input pins		–0.3	—	0.8	V	
Schmidt trigger input voltage	PA13–PA10, PA2, PA0, PB7–PB0	V_T^+	4.0	—	—	V	
		V_T^-	—	—	1.0	V	
		$V_T^+ – V_T^-$	0.4	—	—	V	
Input leak current	$\overline{RES}$	|Iin|	—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
	NMI, MD2–MD0		—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
	Port C		—	—	1.0	µA	Vin = 0.5 to AV_{CC} – 0.5 V
3-state leak current (while off)	Ports A and B, $\overline{CS3}$–$\overline{CS0}$, A21–A0, AD15–AD0	$\|I_{TSI}\|$	—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
Input pull-up MOS current	PA3	–Ip	20	—	300	µA	Vin = 0V
Output high-level voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			3.5	—	—	V	I_{OH} = –1 mA

Table 20.2 DC Characteristics (2)

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 20 MHz, Ta = –20 to +75°C*)

Normal Products: Ta = –40 to +85°C for wide-temperature range products.

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions
Output low level voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
			—	—	1.2	V	I_{OL} = 8 mA
Input capacitance	$\overline{RES}$	Cin	—	—	30	pF	Vin = 0 V, f = 1 MHz, Ta = 25°C
	NMI		—	—	30	pF	
	All other input pins		—	—	20	pF	
Current consumption	Ordinary operation	I_{CC}	—	60	90	mA	f = 12.5 MHz
			—	80	110	mA	f = 16.6 MHz
			—	100	130	mA	f = 20 MHz
	Sleep		—	40	70	mA	f = 12.5 MHz
			—	50	80	mA	f = 16.6 MHz
			—	60	90	mA	f = 20 MHz
	Standby		—	0.01	5*1	µA	Ta ≤ 50°C
			—	—	20.0*2	µA	50°C < Ta
Analog power supply current	During A/D conversion	AI_{CC}	—	1.0	2	mA	
	While A/D converter is waiting		—	0.01	5	µA	
Reference power supply current	During A/D conversion	AI_{ref}	—	0.5	1	mA	AV_{ref} = 5.0 V
	While A/D converter is waiting		—	0.01	5	µA	
RAM stand-by	voltage	V_{RAM}	2.0	—	—	V	

Notes: 1. 50 µA for the SH7032.
2. 300 µA for the SH7032.

Table 20.2 DC Characteristics (3)

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, φ = 16.6 MHz, Ta = –20 to +75°C*)

Normal Products: Ta = –40 to +85°C for wide-temperature range products.

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions
Input high-level voltage	$\overline{RES}$, NMI, MD2–MD0	V_{IH}	V_{CC} – 0.7	—	V_{CC} + 0.3	V	
	EXTAL		V_{CC} × 0.7	—	V_{CC} + 0.3	V	
	Port C		2.2	—	AV_{CC} + 0.3	V	
	Other input pins		2.2	—	V_{CC} + 0.3	V	
Input low-level voltage	$\overline{RES}$, NMI, MD2–MD0	V_{IL}	–0.3	—	0.5	V	
	Other input pins		–0.3	—	0.8	V	
Schmidt trigger input voltage	PA13–10, PA2, PA0, PB7–PB0	V_T^+	4.0	—	—	V	
		V_T^-	—	—	1	V	
		$V_T^+ - V_T^-$	0.4	—	—	V	
Input leak current	$\overline{RES}$	|Iin|	—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
	NMI, MD2–MD0		—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
	Port C		—	—	1.0	µA	Vin = 0.5 to AV_{CC} – 0.5 V
3-state leak current (while off)	Ports A and B, $\overline{CS3}$–$\overline{CS0}$, A21–A0, AD15–AD0	$\|I_{TSI}\|$	—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
Input pull-up MOS current	PA3	–Ip	20	—	300	µA	Vin = 0 V
Output high-level voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			3.5	—	—	V	I_{OH} = –1 mA
Output low level voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
			—	—	1.2	V	I_{OL} = 8 mA

Table 20.2 DC Characteristics (4)

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 16.6 MHz, Ta = –20 to +75°C*)

Normal Products: Ta = –40 to +85°C for wide-temperature range products.

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions
Input capacitance	$\overline{RES}$	Cin	—	—	30	pF	Vin = 0 V f = 1 MHz Ta = 25°C
	NMI		—	—	30	pF	
	All other input pins		—	—	20	pF	
Current consumption	Ordinary operation	I_{CC}	—	60	90	mA	f = 12.5 MHz
			—	80	110	mA	f = 16.6 MHz
	Sleep		—	40	70	mA	f = 12.5 MHz
			—	50	80	mA	f = 16.6 MHz
	Standby		—	0.01	5*1	µA	Ta ≤ 50°C
			—	—	20.0*2	µA	50°C < Ta
Analog power supply current	During A/D conversion	AI_{CC}	—	1.0	2.0	mA	
	While A/D converter is waiting		—	0.01	5	µA	
Reference power supply current	During A/D conversion	AI_{CC}	—	0.5	1	mA	AV_{ref} = 5.0 V
	While A/D converter is waiting		—	0.01	5	µA	
RAM stand-by	voltage	V_{RAM}	2.0	—	—	V	

Notes: 1. 50 µA for the SH7032.
2. 300 µA for the SH7032.

Table 20.2 DC Characteristics (5)

Conditions: V_{CC} = 3.0 V to 5.5 V, AV_{CC} = 3.0 to 5.5 V, AV_{CC} = V_{CC} ±10%, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 12.5 MHz, Ta = –20 to +75°C*)

Normal Products: Ta = –40 to +85°C for wide-temperature range products.

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions
Input high-level voltage	$\overline{RES}$, NMI, MD2–MD0	V_{IH}	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$	V	
	EXTAL		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
	Port C		$V_{CC} \times 0.7$	—	$AV_{CC} + 0.3$	V	
	Other input pins		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
Input low-level voltage	$\overline{RES}$, NMI, MD2–MD0	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	Other input pins		–0.3	—	$V_{CC} \times 0.2$	V	
Schmidt trigger input voltage	PA13–10, PA2, PA0, PB7–PB0	V_T^+	$V_{CC} \times 0.9$	—	—	V	
		V_T^-	—	—	$V_{CC} \times 0.2$	V	
		$V_T^+ - V_T^-$	$V_{CC} \times 0.07$	—	—	V	
Input leak current	$\overline{RES}$	|Iin|	—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
	NMI, MD2–MD0		—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
	Port C		—	—	1.0	µA	Vin = 0.5 to AV_{CC} – 0.5 V
3-state leak current (while off)	Ports A and B, $\overline{CS3}$–$\overline{CS0}$, A21–A0, AD15–AD0	$\|I_{TSI}\|$	—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
Input pull-up MOS current	PA3	–Ip	20	—	300	µA	Vin = 0V
Output high-level voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA
Output low level voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
			—	—	1.2	V	I_{OL} = 8 mA

Table 20.2 DC Characteristics (6)

Conditions: V_{CC} = 3.0 V to 5.5 V, AV_{CC} = 3.0 to 5.5 V, AV_{CC} = V_{CC} ±10%, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 12.5 MHz, Ta = –20 to +75°C*)

Normal Products: Ta = –40 to +85°C for wide-temperature range products.

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions
Input capacitance	$\overline{RES}$	Cin	—	—	30	pF	Vin = 0 V
	NMI		—	—	30	pF	f = 1 MHz
	All other input pins		—	—	20	pF	Ta = 25°C
Current consumption	Ordinary operation	I_{CC}	—	60	90	mA	f = 12.5 MHz
	Sleep		—	40	70	mA	f = 12.5 MHz
	Standby		—	0.01	5*1	µA	Ta ≤ 50°C
			—	—	20.0*2	µA	50°C < Ta
Analog power supply current	During A/D conversion	AI_{CC}	—	0.5	1.5	mA	AV_{CC} = 3.0 V
			—	1.0	2.0	mA	AV_{CC} = 5.0 V
	While A/D converter is waiting		—	0.01	5.0	µA	
Reference power supply current	During A/D conversion	AI_{ref}	—	0.4	0.8	mA	AV_{ref} = 3.0 V
			—	0.5	1	mA	AV_{ref} = 5.0 V
	While A/D converter is waiting		—	0.01	5.0	µA	
RAM stand-by	voltage	V_{RAM}	2.0	—	—	V	

Notes: 1. 50 µA for the SH7032.
2. 300 µA for the SH7032.
3. I_{CC} depends on V_{CC} and f as follows.
I_{CC} max. = 1.0 (mA) + 1.29 (mA/MHz · V) × V_{CC} × f [ordinary operation]
I_{CC} max. = 1.0 (mA) + 1.00 (mA/MHz · V) × V_{CC} × f [sleep]

Table 20.3 Permitted Output Current Values

Case A: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 to 5.5 V, AV_{CC} = V_{CC} ±10%, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*)

Case B: V_{CC} = 5.0 V ±10%, AV_{CC}= 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*)

Normal Products: Ta = –40 to +85°C for wide-temperature range products.

		Case A			Case B						
		12.5 MHz			16.6 MHz			20 MHz			
Item	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
Output low-level permissible current (per pin)	I_{OL}	—	—	10	—	—	10	—	—	10	mA
Output low-level permissible current (total)	ΣI_{OL}	—	—	80	—	—	80	—	—	80	mA
Output high-level permissible current (per pin)	$-I_{OH}$	—	—	2.0	—	—	2.0	—	—	2.0	mA
Output high-level permissible current (total)	$-\Sigma I_{OH}$	—	—	25	—	—	25	—	—	25	mA

Caution: To ensure LSI reliability, do not exceed the value for output current given in table 20.3.

20.3 AC Characteristics

The following AC timing chart represents the AC characteristics, not signal functions. For signal functions, see the explanation in the text.

20.3.1 Clock Timing

Table 20.4 Clock Timing

Case A: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 to 5.5 V, AV_{CC} = V_{CC} ±10%, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 20 MHz, Ta = –20 to +75°C*)

Case B: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 20 MHz, Ta = –20 to +75°C*)

Normal Products: Ta = –40 to +85°C for wide-temperature range products.

		Case A		Case B					
		12.5 MHz		16.6 MHz		20 MHz			
Item	Symbol	Min	Max	Min	Max	Min	Max	Unit	Figures
EXTAL input high level pulse width	t_{EXH}	20	—	10	—	10	—	ns	20.1
EXTAL input low level pulse width	t_{EXL}	20	—	10	—	10	—	ns	
EXTAL input rise time	t_{EXr}	—	10	—	5	—	5	ns	
EXTAL input fall time	t_{EXf}	—	10	—	5	—	5	ns	
Clock cycle time	t_{cyc}	80	500	60	500	50	500	ns	20.1, 20.2
Clock high pulse width	t_{CH}	30	—	20	—	20	—	ns	20.2
Clock low pulse width	t_{CL}	30	—	20	—	20	—	ns	
Clock rise time	t_{Cr}	—	10	—	5	—	5	ns	
Clock fall time	t_{Cf}	—	10	—	5	—	5	ns	
Reset oscillation settling time	t_{OSC1}	10	—	10	—	10	—	ms	20.3
Software standby oscillation settling time	t_{OSC2}	10	—	10	—	10	—	ms	

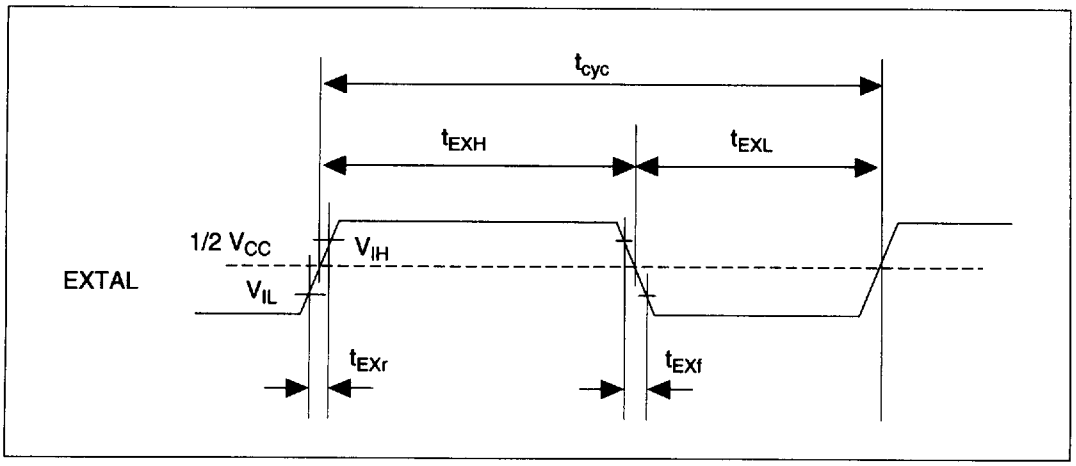


Figure 20.1 EXTAL Input Timing

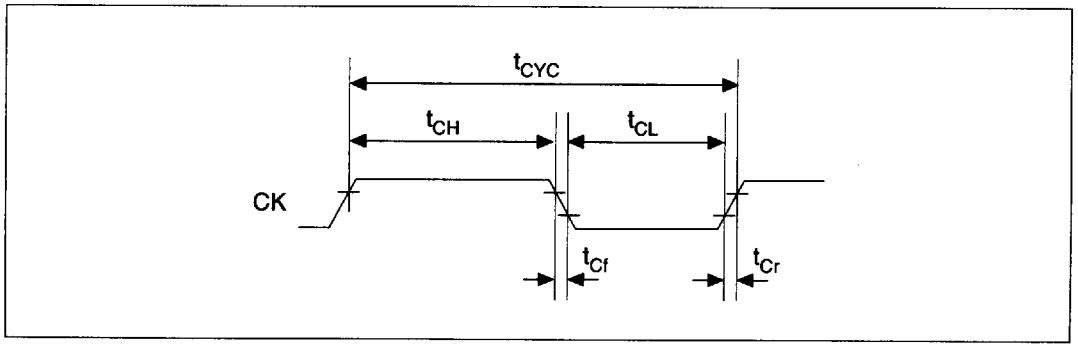


Figure 20.2 System Clock Timing

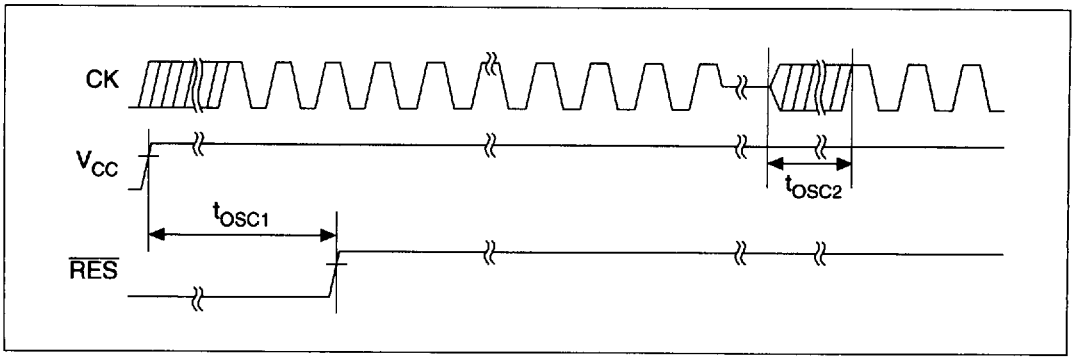


Figure 20.3 Oscillation Settling Time

20.3.2 Control Signal Timing

Table 20.5 Control Signal Timing

Case A: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 to 5.5 V, AV_{CC} = V_{CC} ±10%, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*)

Case B: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*)

Normal Products: Ta = –40 to +85°C for wide-temperature range products.

		Case A		Case B					
		12.5 MHz		16.6 MHz		20 MHz			
Item	Symbol	Min	Max	Min	Max	Min	Max	Unit	Figure
$\overline{RES}$ setup time	t_{RESS}	320	—	240	—	200	—	ns	20.4
$\overline{RES}$ pulse width	t_{RESW}	20	—	20	—	20	—	t_{cyc}	
NMI reset setup time	t_{NMIRS}	320	—	240	—	200	—	ns	
NMI reset hold time	t_{NMIRH}	320	—	240	—	200	—	ns	
NMI setup time	t_{NMIS}	160	—	120	—	100	—	ns	20.5
NMI hold time	t_{NMIH}	80	—	60	—	50	—	ns	
$\overline{IRQ0}$–$\overline{IRQ7}$ setup time (edge detection time)	t_{IRQES}	160	—	120	—	100	—	ns	
$\overline{IRQ0}$–$\overline{IRQ7}$ setup time (level detection time)	t_{IRQLS}	160	—	120	—	100	—	ns	
$\overline{IRQ0}$–$\overline{IRQ7}$ hold time	t_{IRQEH}	80	—	60	—	50	—	ns	
$\overline{IRQOUT}$ output delay time)	t_{IRQOD}	—	80	—	60	—	50	ns	20.6
Bus request setup time	t_{BRQS}	80	—	60	—	50	—	ns	20.7
Bus acknowledge delay time 1	t_{BACD1}	—	80	—	60	—	50	ns	
Bus acknowledge delay time 2	t_{BACD2}	—	80	—	60	—	50	ns	
Bus 3-state delay time	t_{BZD}	—	80	—	60	—	50	ns	

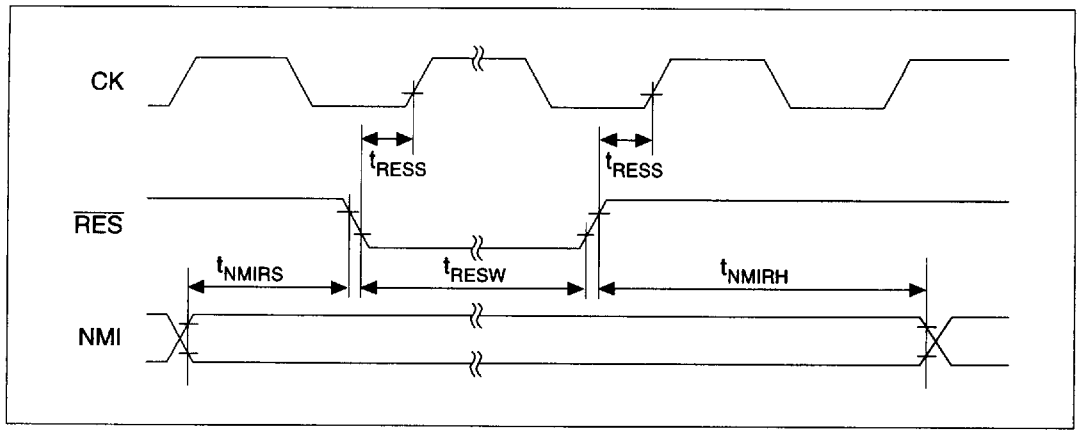


Figure 20.4 Reset Input Timing

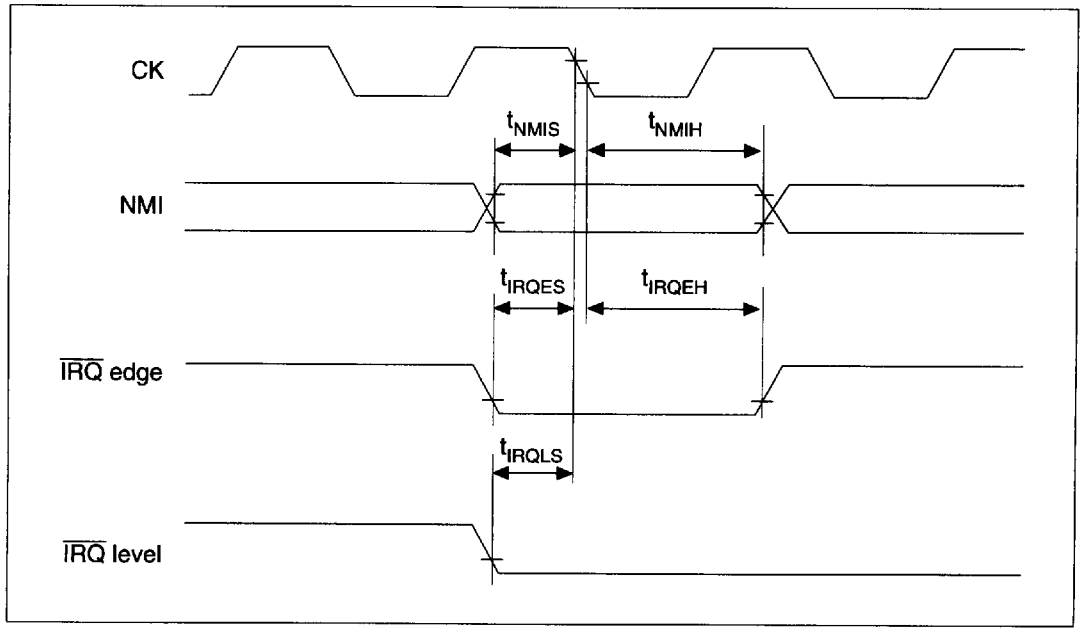


Figure 20.5 Interrupt Signal Input Timing

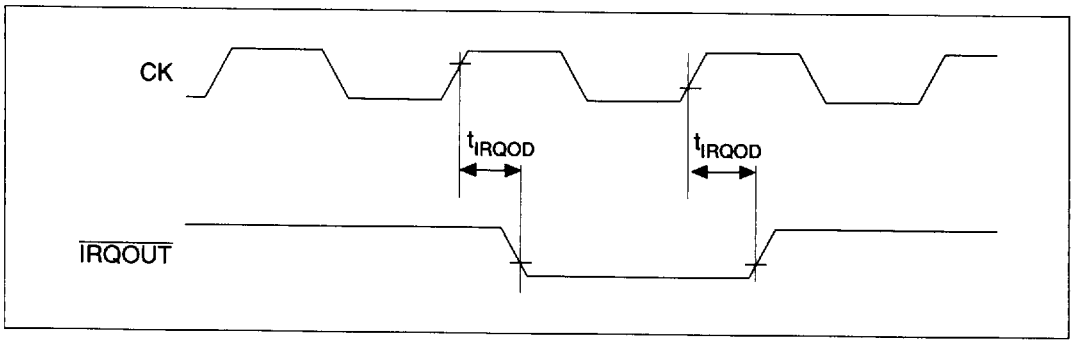


Figure 20.6 Interrupt Signal Output Timing

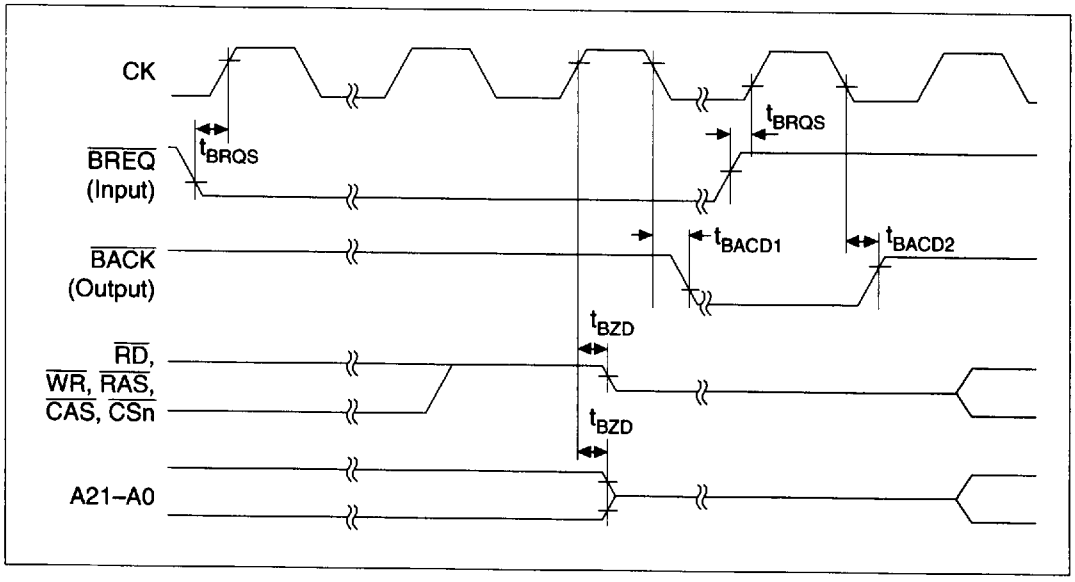


Figure 20.7 Bus Release Timing

20.3.3 Bus Timing

Table 20.6 Bus Timing (1)

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 20 MHz, Ta = –20 to +75°C*

Normal Products: Ta = –40 to +85°C for wide-temperature range products.

Item		Symbol	Min	Max	Unit	Figures
Address delay time		t_{AD}	—	20*1	ns	20.8, 20.9, 20.11–20.14, 20.19, 20.20
$\overline{CS}$ delay time 1		t_{CSD1}	—	25	ns	20.8, 20.9, 20.20
$\overline{CS}$ delay time 2		t_{CSD2}	—	25	ns	
$\overline{CS}$ delay time 3		t_{CSD3}	—	20	ns	20.19
$\overline{CS}$ delay time 4		t_{CSD4}	—	20	ns	
Access time 1 from read strobe	35% duty*2	t_{RDAC1}	$t_{cyc} \times 0.65 - 20$	—	ns	20.8,
	50% duty		$t_{cyc} \times 0.5 - 20$	—	ns	
Access time 2 from read strobe	35% duty*2	t_{RDAC2}	$t_{cyc} \times (n+1.65) - 20$*3	—	ns	20.9, 20.10
	50% duty		$t_{cyc} \times (n+1.5) - 20$*3	—	ns	
Access time 3 from read strobe	35% duty*2	t_{RDAC3}	$t_{cyc} \times (n+0.65) - 20$*3	—	ns	20.19
	50% duty		$t_{cyc} \times (n+0.5) - 20$*3	—	ns	
Read strobe delay time		t_{RSD}	—	20	ns	20.8, 20.9, 20.11–20.15, 20.19, 20.24–20.28
Read data setup time		t_{RDS}	15	—	ns	20.8, 20.9, 20.11–20.14,
Read data hold time		t_{RDH}	0	—	ns	20.19
Write strobe delay time 1		t_{WSD1}	—	20	ns	20.9, 20.13, 20.14, 20.19, 20.20
Write strobe delay time 2		t_{WSD2}	—	20	ns	20.9, 20.13, 20.14, 20.19
Write strobe delay time 3		t_{WSD3}	—	20	ns	20.11, 20.12
Write strobe delay time 4		t_{WSD4}	—	20	ns	20.11, 20.12, 20.20
Write data delay time 1		t_{WDD1}	—	35	ns	20.9, 20.13, 20.14, 19
Write data delay time 2		t_{WDD2}	—	20	ns	20.11, 20.12
Write data hold time		t_{WDH}	0	—	ns	20.9, 20.11–20.14

Table 20.6 Bus Timing (1) (cont)

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%,AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, φ = 20 MHz, Ta = –20 to +75°C*

Normal Products: Ta = –40 to +85°C for wide-temperature range products.

Item	Symbol	Min	Max	Unit	Figures
Parity output delay time 1	t_{WPDD1}	—	40	ns	20.9, 20.13, 20.14
Parity output delay time 2	t_{WPDD2}	—	20	ns	20.11, 20.12
Parity output hold time	t_{WPDH}	0	—	ns	20.9, 20.11–20.14
Wait setup time	t_{WTS}	14	—	ns	20.10, 20.15, 20.19
Wait hold time	t_{WTH}	10	—	ns	
Read data access time 1	t_{ACC1}	t_{cyc} – 30*4	—	ns	20.8, 20.11, 20.12
Read data access time 2	t_{ACC2}	$t_{cyc} \times (n+2)$ – 30*3	—	ns	20.9, 20.10, 20.13, 20.14
$\overline{RAS}$ delay time 1	t_{RASD1}	—	20	ns	20.11–20.14, 20.16–20.18
$\overline{RAS}$ delay time 2	t_{RASD2}	—	30	ns	
$\overline{CAS}$ delay time 1	t_{CASD1}	—	20	ns	20.11
$\overline{CAS}$ delay time 2	t_{CASD2}	—	20	ns	20.13, 20.14, 20.16–20.18
$\overline{CAS}$ delay time 3	t_{CASD3}	—	20	ns	
Column address setup time	t_{ASC}	0	—	ns	20.11, 20.12
Read data access time from $\overline{CAS}$ 1 — 35% duty*2	t_{CAC1}	$t_{cyc} \times 0.65$ – 19	—	ns	
Read data access time from $\overline{CAS}$ 1 — 50% duty	t_{CAC1}	$t_{cyc} \times 0.5$ – 19	—	ns	
Read data access time from $\overline{CAS}$ 2	t_{CAC2}	$t_{cyc} \times (n+1)$ – 25*3	—	ns	20.13, 20.14, 20.15
Read data access time from $\overline{CAS}$ 1	t_{RAC1}	$t_{cyc} \times 1.5$ – 20	—	ns	20.11, 20.12
Read data access time from $\overline{RAS}$ 2	t_{RAC2}	$t_{cyc} \times (n+2.5)$ – 20*3	—	ns	20.13, 20.14, 20.15
High-speed page mode $\overline{CAS}$ precharge time	t_{CP}	$t_{cyc} \times 0.25$	—	ns	20.12

Table 20.6 Bus Timing (1) (cont)

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, φ = 20 MHz, Ta = –20 to +75°C*

Normal Products: Ta = –40 to +85°C for wide-temperature range products.

Item		Symbol	Min	Max	Unit	Figures
$\overline{AH}$ delay time 1		t_{AHD1}	—	20	ns	20.19
$\overline{AH}$ delay time 2		t_{AHD2}	—	20	ns	
Multiplexed address delay time		t_{MAD}	—	30	ns	
Multiplexed address hold time		t_{MAH}	0	—	ns	
DACK0, DACK1 delay time 1		t_{DACD1}	—	23	ns	20.8, 20.9, 20.11–20.14, 20.19, 20.20
DACK0, DACK1 delay time 2		t_{DACD2}	—	23	ns	
DACK0, DACK1 delay time 3		t_{DACD3}	—	20	ns	20.9, 20.13, 20.14, 20.19
DACK0, DACK1 delay time 4		t_{DACD4}	—	20	ns	20.11, 20.12
DACK0, DACK1 delay time 5		t_{DACD5}	—	20	ns	
Read delay time	35% duty*2	t_{RDD}	—	$t_{cyc} \times 0.35 + 12$	ns	20.8, 20.9, 20.11-20.15, 20.19, 20.24-20.28
	50% duty		—	$t_{cyc} \times 0.5 + 15$	ns	
Data setup time for $\overline{CAS}$		t_{DS}	0*5	—	ns	20.11, 20.13
$\overline{CAS}$ setup time for $\overline{RAS}$		t_{CSR}	10	—	ns	20.16, 20.17, 20.18
Row address hold time		t_{RAH}	10	—	ns	20.11, 20.13
Write command hold time		t_{WCH}	15	—	ns	
Write command setup time	35% duty*2	t_{WCS}	0	—	ns	20.11
	50% duty	t_{WCS}	0	—	ns	
Access time from $\overline{CAS}$ precharge		t_{ACP}	t_{cyc} –20	—	ns	20.12

Notes: 1. HBS and LBS signals are 25 ns.
2. When frequency is 10 MHz or more.
3. n is the number of wait cycles.
4. Access time from addresses A0 to A21 is tcyc-25.
5. –5ns for parity output of DRAM long-pitch access.

Table 20.7 Bus Timing (2)

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 16.6 MHz, Ta = –20 to +75°C*

Normal Products: Ta = –40 to +85°C for wide-temperature range products.

Item		Symbol	Min	Max	Unit	Figures
Address delay time		t_{AD}	—	25*1	ns	20.8, 20.9, 20.11–20.14, 20.19, 20.20
$\overline{CS}$ delay time 1		t_{CSD1}	—	30	ns	20.8, 20.9, 20.20
$\overline{CS}$ delay time 2		t_{CSD2}	—	25	ns	
$\overline{CS}$ delay time 3		t_{CSD3}	—	25	ns	20.19
$\overline{CS}$ delay time 4		t_{CSD4}	—	25	ns	
Access time 1 from read strobe	35% duty*2	t_{RDAC1}	$t_{cyc} \times 0.65 - 20$	—	ns	20.8, 20.9,
	50% duty		$t_{cyc} \times 0.5 - 20$	—	ns	
Access time 2 from read strobe	35% duty*2	t_{RDAC2}	$t_{cyc} \times (n + 1.65) - 20$*3	—	ns	20.9, 20.10
	50% duty		$t_{cyc} \times (n + 1.5) - 20$*3	—	ns	
Access time 3 from read strobe	35% duty*1	t_{RDAC3}	$t_{cyc} \times (n + 0.65) - 20$*3	—	ns	20.19
	50% duty		$t_{cyc} \times (n + 0.5) - 20$*3	—	ns	
Read strobe delay time		t_{RSD}	—	25	ns	20.8, 20.9, 20.19
Read data setup time		t_{RDS}	15	—	ns	20.8, 20.9, 20.11–20.14,
Read data hold time		t_{RDH}	0	—	ns	20.19
Write strobe delay time 1		t_{WSD1}	—	25	ns	20.9, 20.13, 20.14, 20.19, 20.20
Write strobe delay time 2		t_{WSD2}	—	25	ns	20.9, 20.13, 20.14, 20.19
Write strobe delay time 3		t_{WSD3}	—	25	ns	20.11, 20.12
Write strobe delay time 4		t_{WSD4}	—	25	ns	20.11, 20.12, 20.20
Write data delay time 1		t_{WDD1}	—	45	ns	20.9, 20.13, 20.14, 20.19
Write data delay time 2		t_{WDD2}	—	25	ns	20.11, 20.12
Write data hold time		t_{WDH}	0	—	ns	20.9, 20.11–20.14
Parity output delay time 1		t_{WPDD1}	—	45	ns	20.9, 20.13, 20.14
Parity output delay time 2		t_{WPDD2}	—	25	ns	20.11, 20.12
Parity output hold time		t_{WPDH}	0	—	ns	20.9, 20.11–20.14

Table 20.7 Bus Timing (2) (cont)

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 16.6 MHz, Ta = –20 to +75°C*

Normal Products: Ta = –40 to +85°C for wide-temperature range products.

Item		Symbol	Min	Max	Unit	Figures
Wait setup time		t_{WTS}	19	—	ns	20.10, 20.15, 20.19
Wait hold time		t_{WTH}	10	—	ns	
Read data access time 1		t_{ACC1}	t_{cyc} – 30*4	—	ns	20.8, 20.11, 20.12
Read data access time 2		t_{ACC2}	$t_{cyc} \times (n+2) - 30$*3	—	ns	20.9, 20.10, 20.13, 20.14
$\overline{RAS}$ delay time 1		t_{RASD1}	—	25	ns	20.11–20.14, 20.16–20.18
$\overline{RAS}$ delay time 2		t_{RASD2}	—	35	ns	
$\overline{CAS}$ delay time 1		t_{CASD1}	—	25	ns	20.11
$\overline{CAS}$ delay time 2		t_{CASD2}	—	25	ns	20.13, 20.14, 20.16–20.18
$\overline{CAS}$ delay time 3		t_{CASD3}	—	25	ns	
Column address setup time		t_{ASC}	0	—	ns	20.11, 20.12
Read data access time from CAS 1	35% duty*2	t_{CAC1}	$t_{cyc} \times 0.65 - 19$	—	ns	
	50% duty		$t_{cyc} \times 0.5 - 19$	—	ns	
Read data access time from $\overline{CAS}$ 2		t_{CAC2}	$t_{cyc} \times (n + 1) - 25$*3	—	ns	20.13, 20.14, 20.15
Read data access time from $\overline{RAS}$ 1		t_{RAC1}	$t_{cyc} \times 1.5 - 20$	—	ns	20.11, 20.12
Read data access time from $\overline{RAS}$ 2		t_{RAC2}	$t_{cyc} \times (n + 2.5) - 20$*3	—	ns	20.13, 20.14, 20.15
High-speed page mode $\overline{CAS}$ precharge time		t_{CP}	$t_{cyc} \times 0.25$	—	ns	20.12
$\overline{AH}$ delay time 1		t_{AHD1}	—	25	ns	20.19
$\overline{AH}$ delay time 2		t_{AHD2}	—	25	ns	
Multiplexed address delay time		t_{MAD}	—	30	ns	
Multiplexed address hold time		t_{MAH}	0	—	ns	

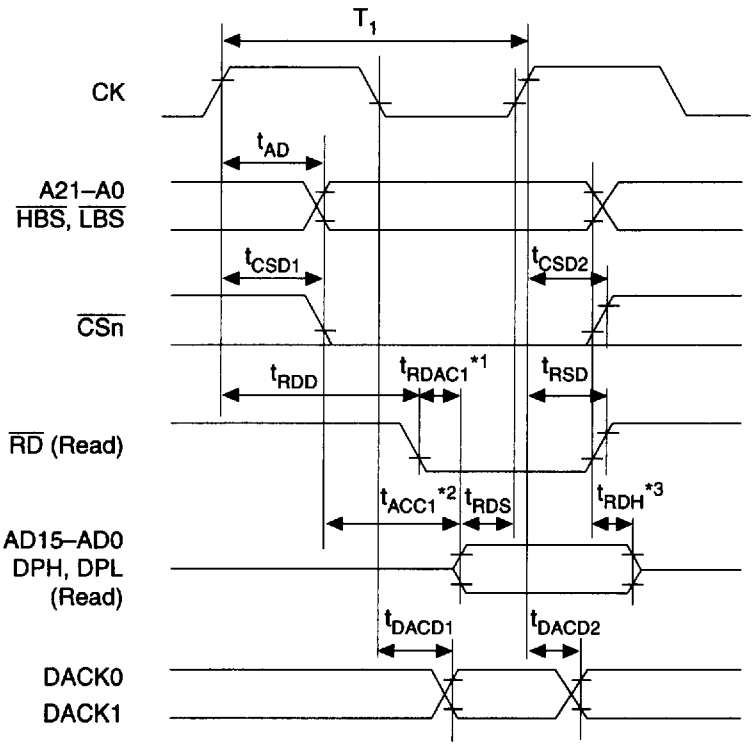
Table 20.7 Bus Timing (2) (cont)

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, φ = 16.6 MHz, Ta = –20 to +75°C*

Normal Products: Ta = –40 to +85°C for wide-temperature range products.

Item		Symbol	Min	Max	Unit	Figures
DACK0, DACK1 delay time 1		t_{DACD1}	—	25	ns	20.8, 20.9, 20.11–20.14, 20.19, 20.20
DACK0, DACK1 delay time 2		t_{DACD2}	—	25	ns	
DACK0, DACK1 delay time 3		t_{DACD3}	—	25	ns	20.9, 20.13, 20.14, 20.19
DACK0, DACK1 delay time 4		t_{DACD4}	—	25	ns	20.11, 20.12
DACK0, DACK1 delay time 5		t_{DACD5}	—	25	ns	
Read delay time	35% duty*2	t_{RDD}	—	$t_{cyc} \times 0.35 + 12$	ns	20.8, 20.9, 20.11-20.15, 20.19, 20.24-20.28
	50% duty		—	$t_{cyc} \times 0.5 + 15$	ns	
Data setup time for $\overline{CAS}$		t_{DS}	0*5	—	ns	20.11, 20.13
$\overline{CAS}$ setup time for $\overline{RAS}$		t_{CSR}	10	—	ns	20.16, 20.17, 20.18
Row address hold time		t_{RAH}	10	—	ns	20.11, 20.13
Write command hold time		t_{WCH}	15	—	ns	
Write command setup time	35% duty*2	t_{WCS}	0	—	ns	20.11
	50% duty		0	—	ns	
Access time from $\overline{CAS}$ precharge		t_{ACP}	t_{cyc} –20	—	ns	20.12

Notes
1. HBS and LBS signals are 30 ns.
2. When frequency is 10 MHz or more
3. n is the number of wait cycles.
4. Access time from addresses A0 to A21 is tcyc-25.
5. –5ns for parity output of DRAM long-pitch access

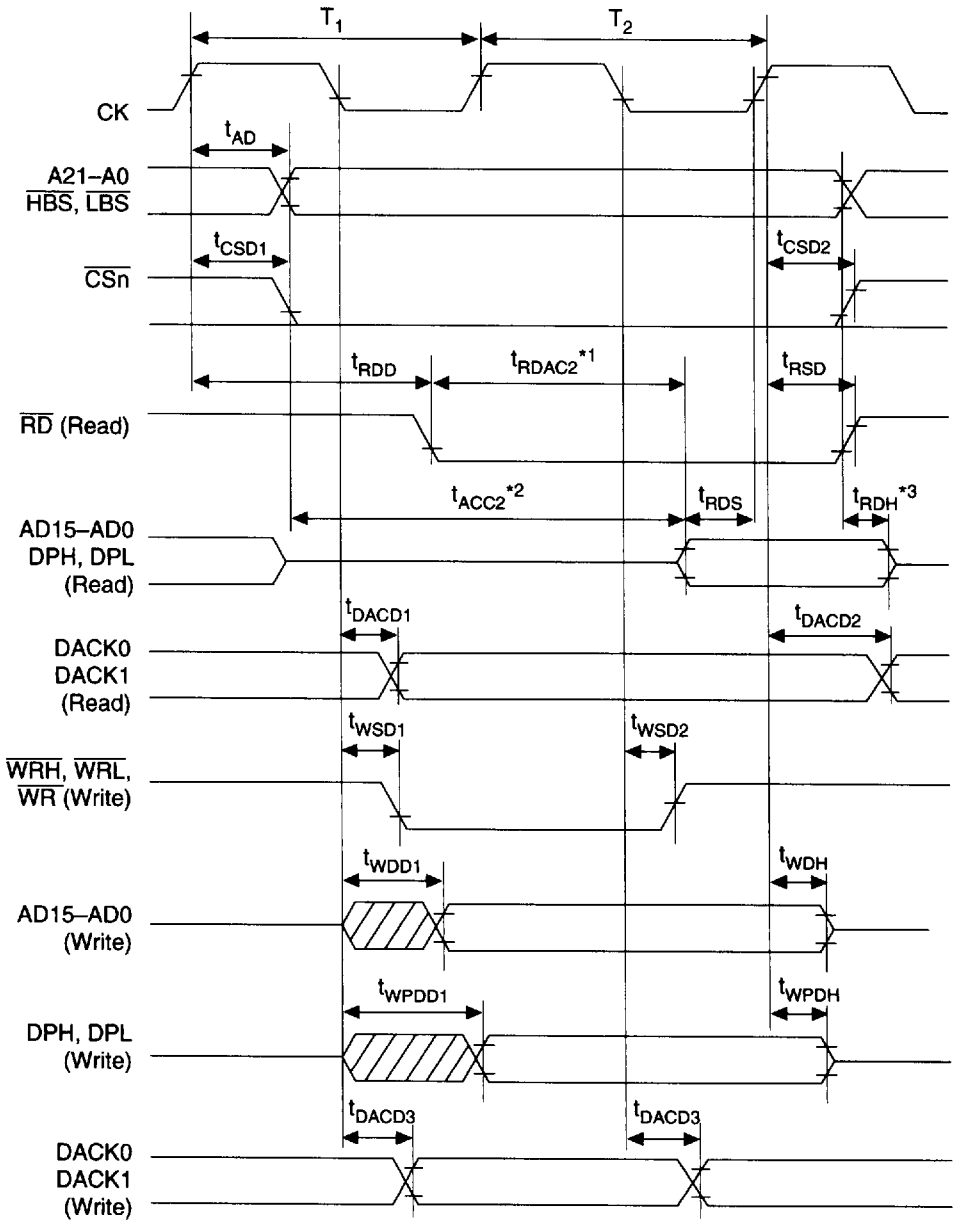


Notes: 1. For t_{RDAC1}, use $t_{cyc} \times 0.65 - 20$ (for 35% duty) or $t_{cyc} \times 0.5 - 20$ (for 50% duty) instead of $t_{cyc} - t_{RDD} - t_{RDS}$.

2. For t_{ACC1}, use $t_{cyc} - 30$ instead of $t_{cyc} - t_{AD}$ (or t_{CSD1}) $- t_{RDS}$.

3. t_{RDH} is measured from A21–A0, $\overline{CSn}$, or $\overline{RD}$, whichever is negated first.

Figure 20.8 Basic Bus Cycle: One-State Access

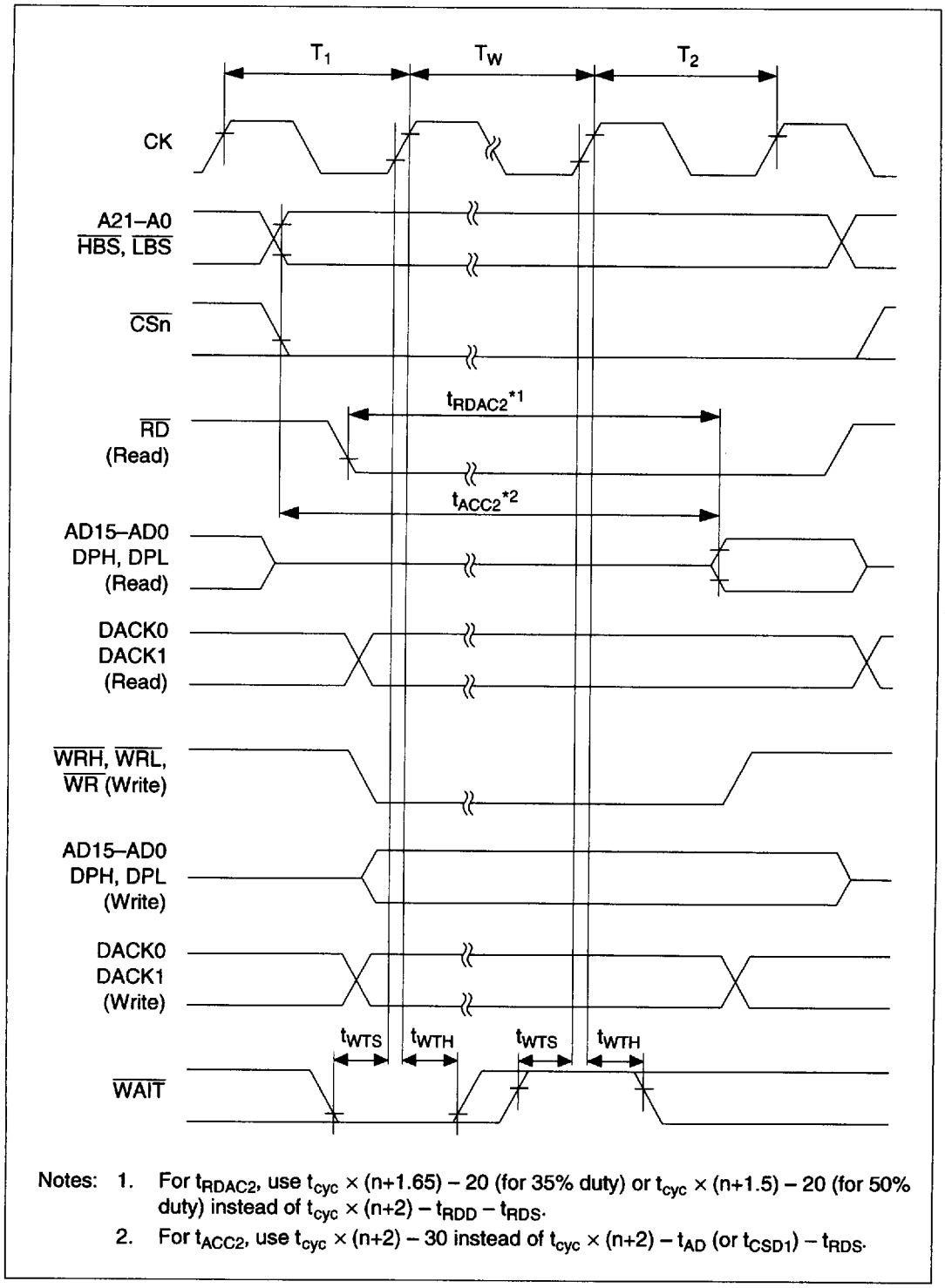


Notes: 1. For t_{RDAC2}, use $t_{cyc} \times (n + 1.65) - 20$ (for 35% duty) or $t_{cyc} \times (n + 1.5) - 20$ (for 50% duty) instead of $t_{cyc} \times (n + 2) - t_{RDD} - t_{RDS}$.

2. For t_{ACC2}, use $t_{cyc} \times (n + 2) - 30$ instead of $t_{cyc} \times (n + 2) - t_{AD}$ (or t_{CSD1}) $- t_{RDS}$.

3. t_{RDH} is measured from A21–A0, $\overline{CSn}$, or $\overline{RD}$, whichever is negated first.

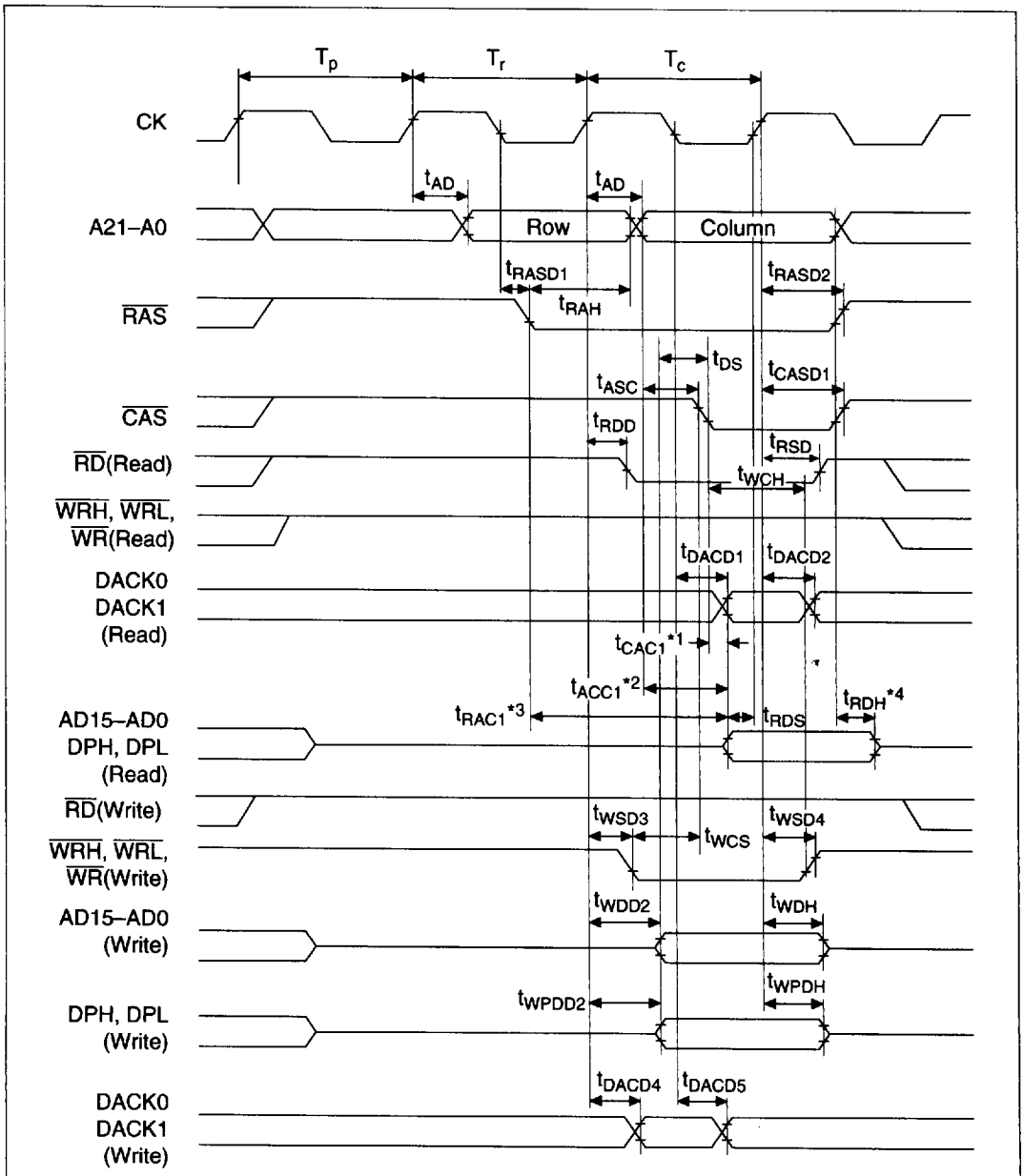
Figure 20.9 Basic Bus Cycle: Two-State Access



Notes: 1. For t_{RDAC2}, use $t_{cyc} \times (n+1.65) - 20$ (for 35% duty) or $t_{cyc} \times (n+1.5) - 20$ (for 50% duty) instead of $t_{cyc} \times (n+2) - t_{RDD} - t_{RDS}$.

2. For t_{ACC2}, use $t_{cyc} \times (n+2) - 30$ instead of $t_{cyc} \times (n+2) - t_{AD}$ (or t_{CSD1}) $- t_{RDS}$.

Figure 20.10 Basic Bus Cycle: Two States + Wait State



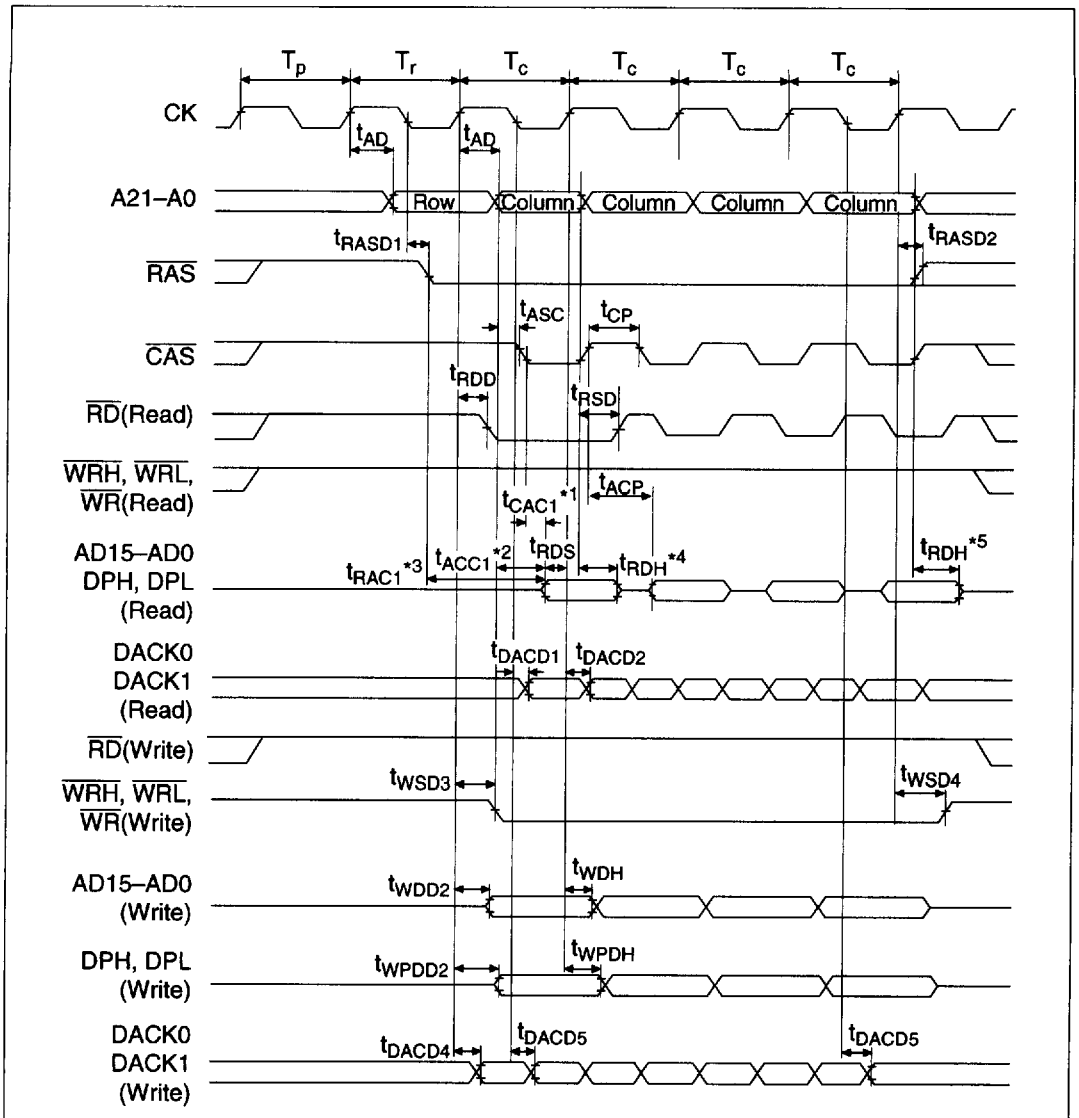
Notes: 1. For t_{CAC1}, use $t_{cyc} \times 0.65 - 19$ (for 35% duty) or $t_{cyc} \times 0.5 - 19$ (for 50% duty) instead of $t_{cyc} - t_{AD} - t_{ASC} - t_{RDS}$.

2. For t_{ACC1}, use $t_{cyc} - 30$ instead of $t_{cyc} - t_{AD} - t_{RDS}$.

3. For t_{RAC1}, use $t_{cyc} \times 1.5 - 20$ instead of $t_{cyc} \times 1.5 - t_{RASD1} - t_{RDS}$.

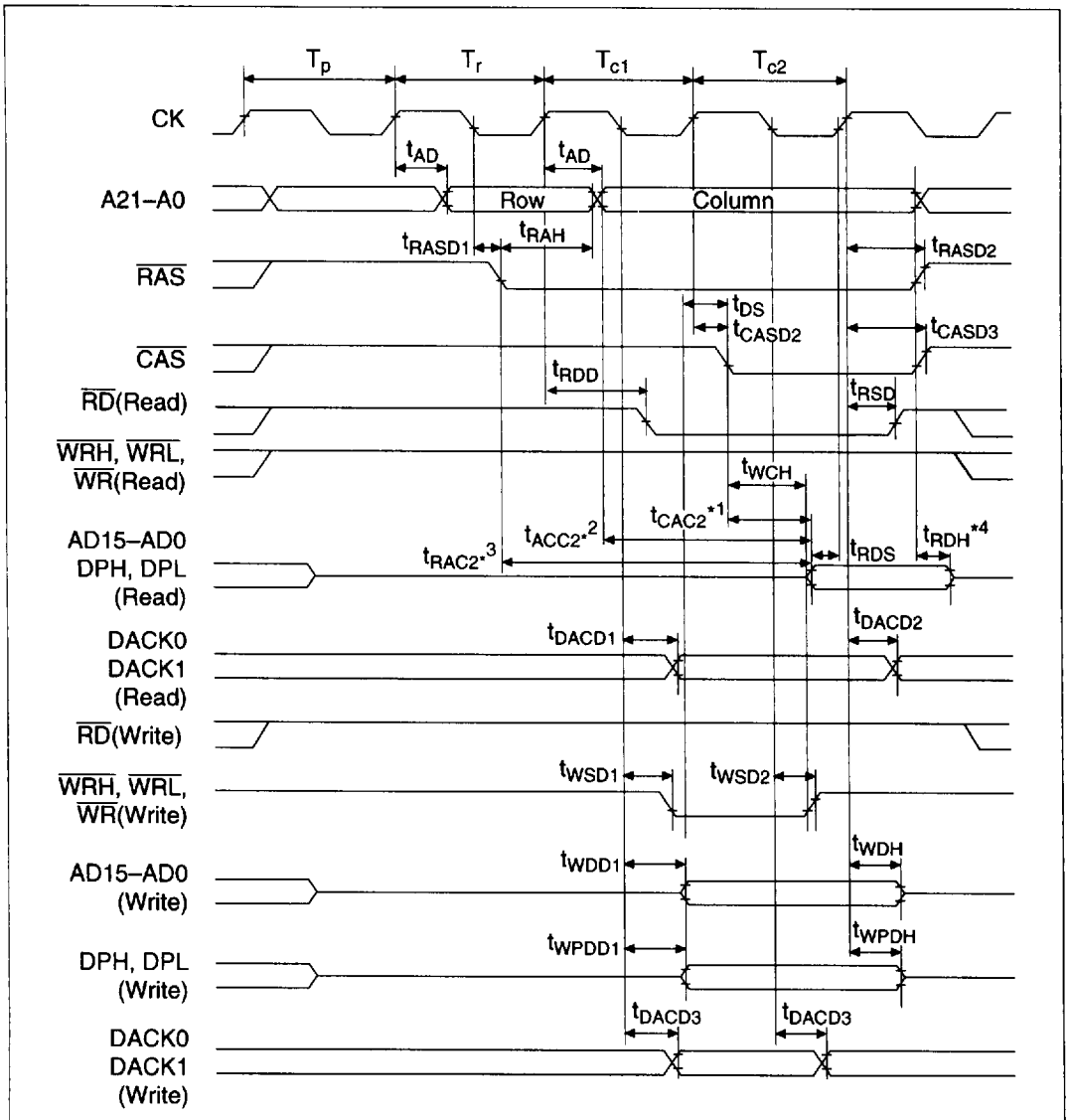
4. t_{RDH} is measured from A21–A0, $\overline{RAS}$, or $\overline{CAS}$, whichever is negated first.

Figure 20.11 DRAM Bus Cycle (Short Pitch, Normal Mode)



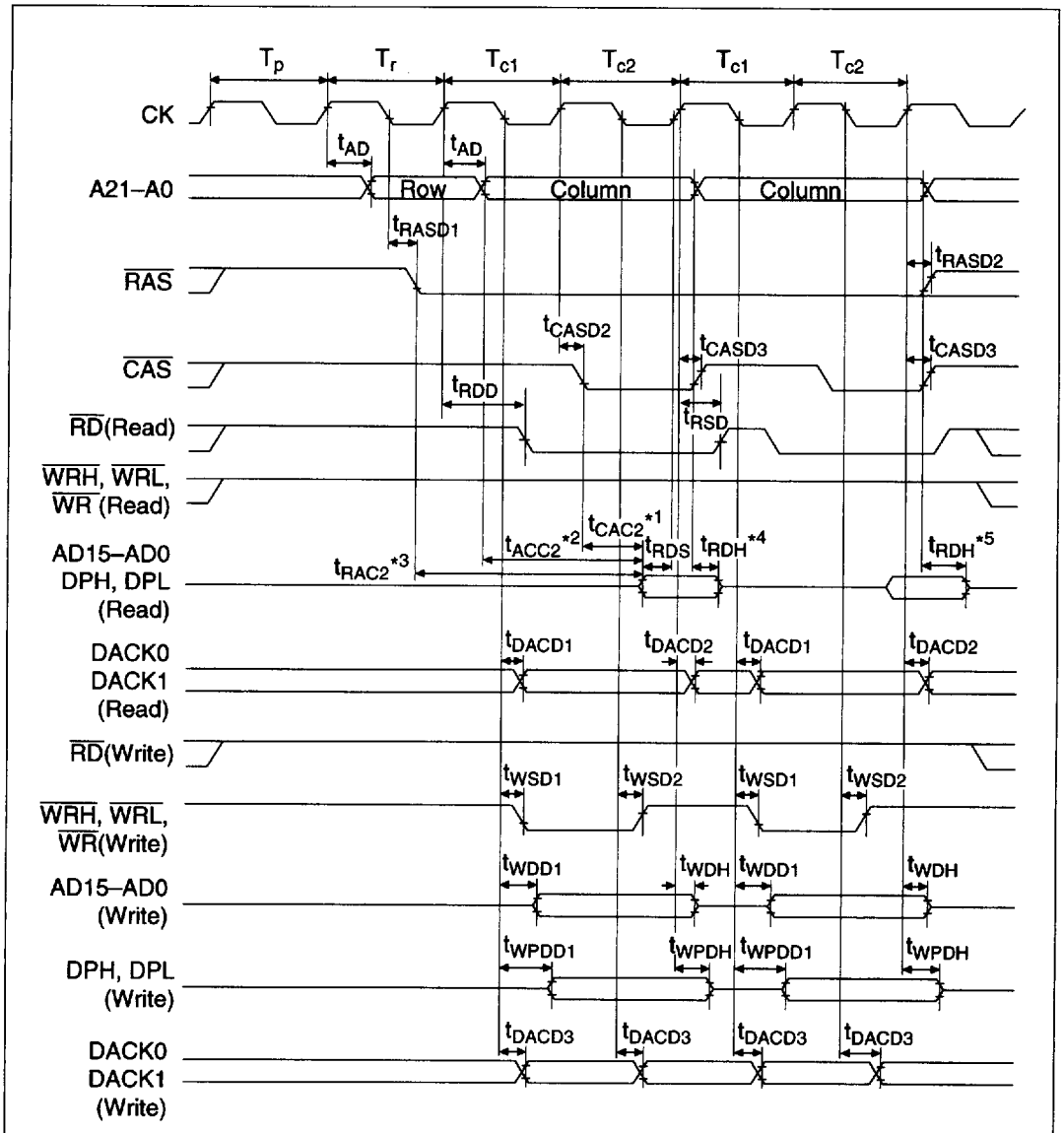
Notes:
1. For t_{CAC1}, use $t_{cyc} \times 0.65 - 19$ (for 35% duty) or $t_{cyc} \times 0.5 - 19$ (for 50% duty) instead of $t_{cyc} - t_{AD} - t_{ASC} - t_{RDS}$.
2. For t_{ACC1}, use $t_{cyc} - 30$ instead of $t_{cyc} - t_{AD} - t_{RDS}$.
3. For t_{RAC1}, use $t_{cyc} \times 1.5 - 20$ instead of $t_{cyc} \times 1.5 - t_{RASD1} - t_{RDS}$.
4. t_{RDH} is measured from A21–A0 or $\overline{CAS}$, whichever is negated first.
5. t_{RDH} is measured from A21–A0, $\overline{RAS}$, or $\overline{CAS}$, whichever is negated first.

Figure 20.12 DRAM Bus Cycle (Short Pitch, High-Speed Page Mode)



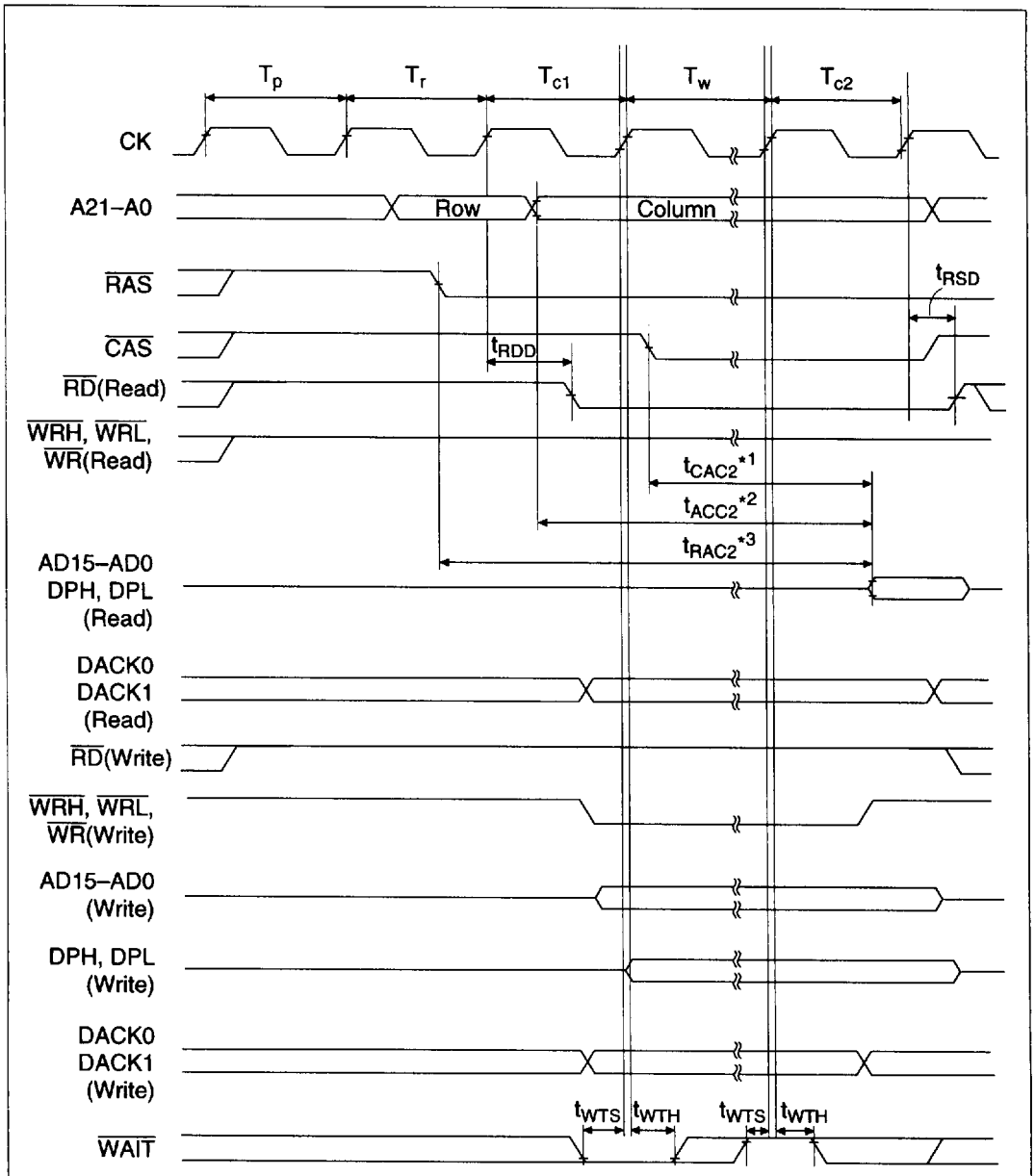
Notes: 1. For t_{CAC2}, use $t_{cyc} \times (n + 1) - 25$ instead of $t_{cyc} \times (n + 1) - t_{CASD2} - t_{RDS}$.
2. For t_{ACC2}, use $t_{cyc} \times (n + 2) - 30$ instead of $t_{cyc} \times (n + 2) - t_{AD} - t_{RDS}$.
3. For t_{RAC2}, use $t_{cyc} \times (n + 2.5) - 20$ instead of $t_{cyc} \times (n + 2.5) - t_{RASD1} - t_{RDS}$.
4. t_{RDH} is measured from A21–A0, $\overline{CAS}$, or $\overline{RAS}$, whichever is negated first.

Figure 20.13 DRAM Bus Cycle: (Long Pitch, Normal Mode)



Notes:
1. For t_{CAC2}, use $t_{cyc} \times (n + 1) - 25$ instead of $t_{cyc} \times (n + 1) - t_{CASD2} - t_{RDS}$.
2. For t_{ACC2}, use $t_{cyc} \times (n + 2) - 30$ instead of $t_{cyc} \times (n + 2) - t_{AD} - t_{RDS}$.
3. For t_{RAC2}, use $t_{cyc} \times (n + 2.5) - 20$ instead of $t_{cyc} \times (n + 2.5) - t_{RASD1} - t_{RDS}$.
4. t_{RDH} is measured from A21–A0 or $\overline{CAS}$, whichever is negated first.
5. t_{RDH} is measured from A21–A0, $\overline{RAS}$, or $\overline{CAS}$ whichever is negated first.

Figure 20.14 DRAM Bus Cycle: (Long Pitch, High-Speed Page Mode)



Notes: 1. For t_{CAC2}, use $t_{cyc} \times (n + 1) - 25$ instead of $t_{cyc} \times (n + 1) - t_{CASD2} - t_{RDS}$.
2. For t_{ACC2}, use $t_{cyc} \times (n + 2) - 30$ instead of $t_{cyc} \times (n + 2) - t_{AD} - t_{RDS}$.
3. For t_{RAC2}, use $t_{cyc} \times (n + 2.5) - 20$ instead of $t_{cyc} \times (n + 2.5) - t_{RASD1} - t_{RDS}$.

Figure 20.15 DRAM Bus Cycle: (Long Pitch, High-Speed Page Mode + Wait State)

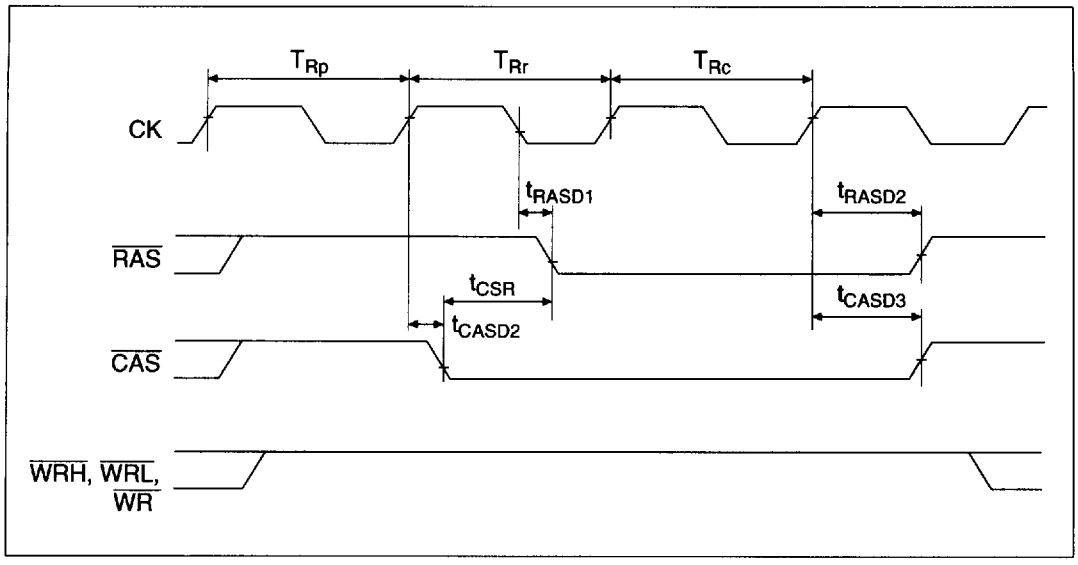


Figure 20.16 CAS-before-RAS Refresh (Short Pitch)

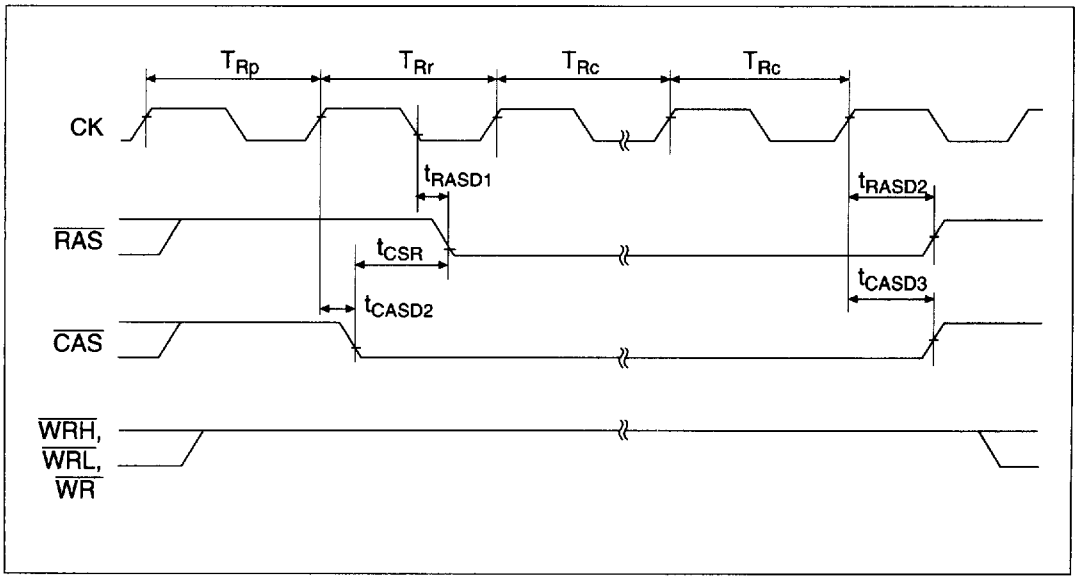


Figure 20.17 CAS-before-RAS Refresh (Long Pitch)

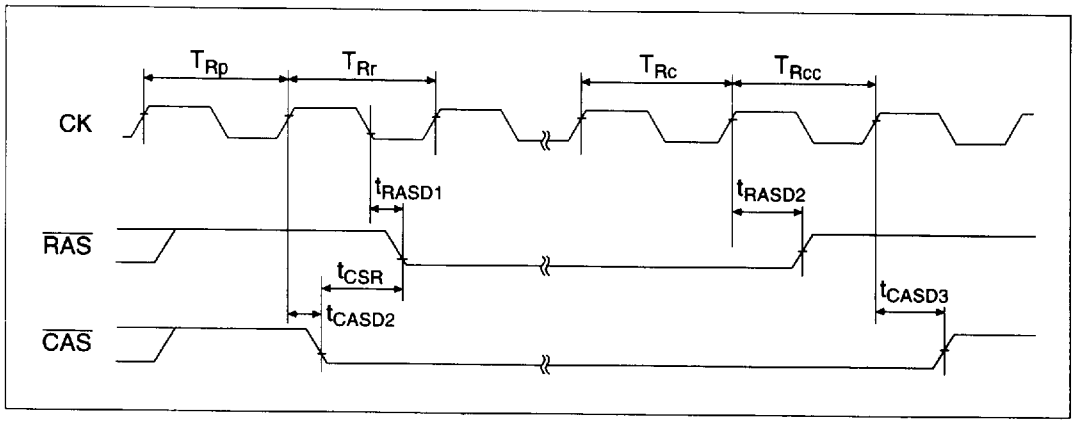


Figure 20.18 Self Refresh

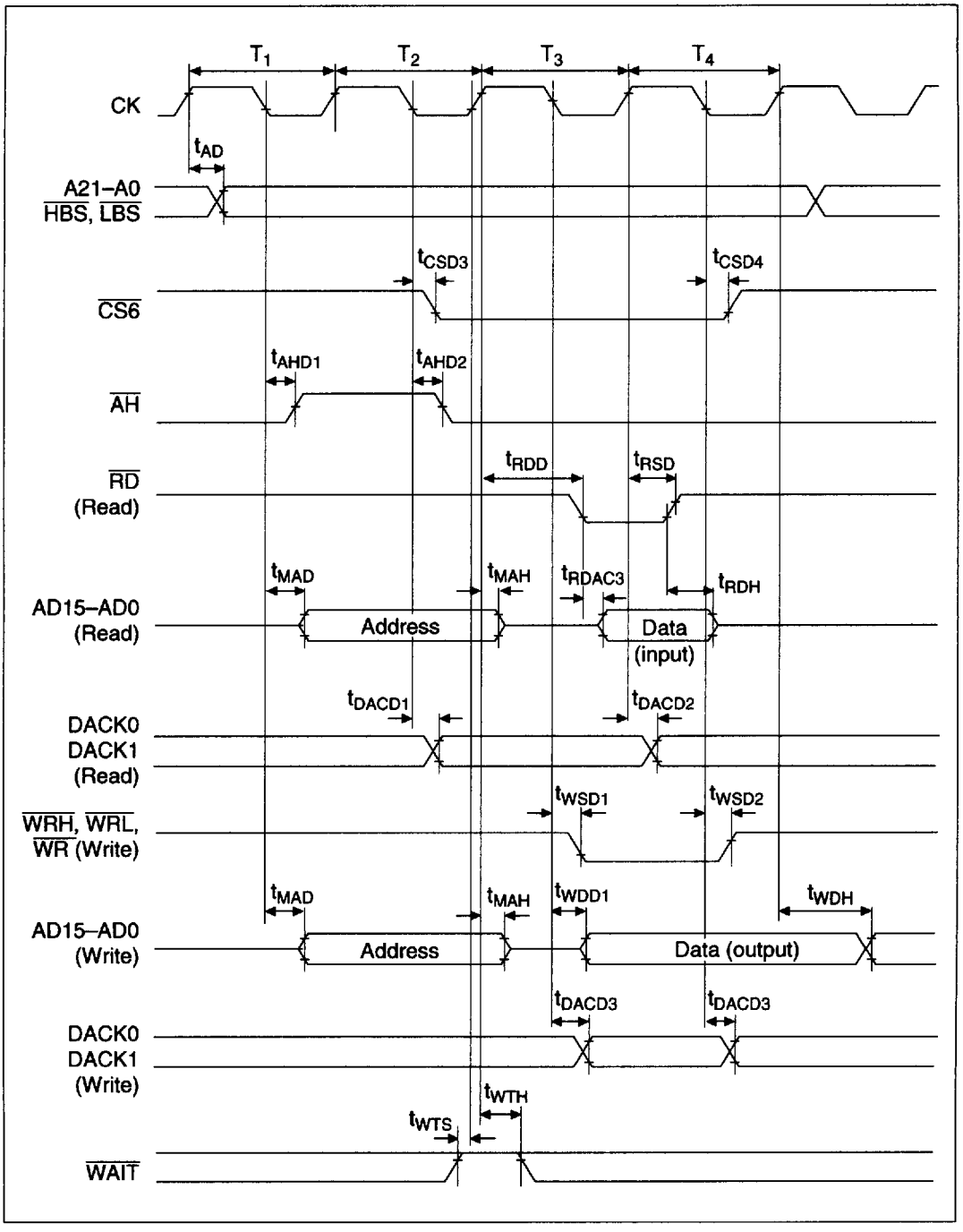


Figure 20.19 Address/Data Multiplex I/O Bus Cycle

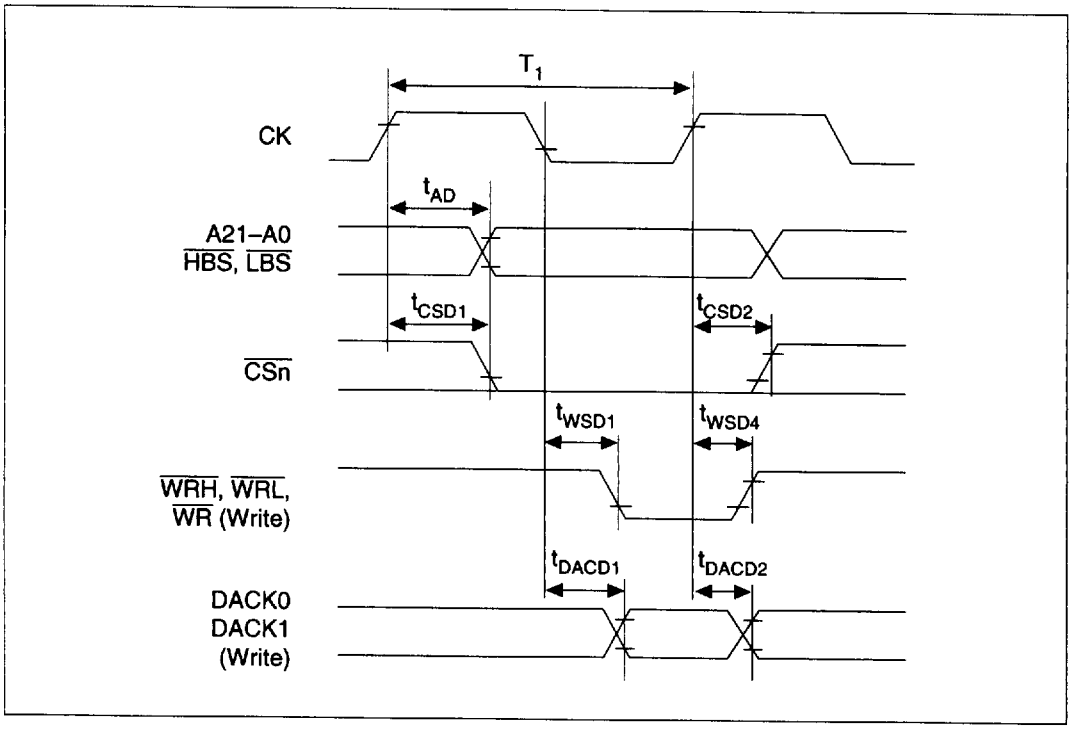


Figure 20.20 DMA Single Transfer/1 State Access Write

Table 20.8 Bus Timing (3)

Conditions: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 to 5.5 V, AV_{CC} = V_{CC} ±10%, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 12.5 MHz, Ta = –20 to +75°C*

Normal Products: Ta = –40 to +85°C for wide-temperature range products.

Item		Symbol	Min	Max	Unit	Figures
Address delay time		t_{AD}	—	40	ns	20.21, 20.22, 20.24–20.27, 20.32, 20.33
$\overline{CS}$ delay time 1		t_{CSD1}	—	40	ns	20.21, 20.22, 20.33
$\overline{CS}$ delay time 2		t_{CSD2}	—	40	ns	
$\overline{CS}$ delay time 3		t_{CSD3}	—	40	ns	20.32
$\overline{CS}$ delay time 4		t_{CSD4}	—	40	ns	
Access time 1 from read strobe	35% duty*1	t_{RDAC1}	$t_{cyc} \times 0.65 - 35$	—	ns	20.21,
	50% duty		$t_{cyc} \times 0.5 - 35$	—	ns	
Access time 2 from read strobe	35% duty*1	t_{RDAC2}	$t_{cyc} \times (n+1.65) - 35$*2	—	ns	20.22, 20.23
	50% duty		$t_{cyc} \times (n+1.5) - 35$*2	—	ns	
Access time 3 from read strobe	35% duty*1	t_{RDAC3}	$t_{cyc} \times (n+0.65) - 35$*2	—	ns	20.32
	50% duty		$t_{cyc} \times (n+0.5) - 35$*2	—	ns	
Read strobe delay time		t_{RSD}	—	40	ns	20.21, 20.22, 20.32
Read data set-up time		t_{RDS}	25	—	ns	20.21, 20.22,
Read data hold time		t_{RDH}	0	—	ns	20.24-20.27, 20.32
Write strobe delay time 1		t_{WSD1}	—	40	ns	20.22, 20.26, 20.27, 20.32, 20.33
Write strobe delay time 2		t_{WSD2}	—	30	ns	20.22, 20.26, 20.27, 20.32
Write strobe delay time 3		t_{WSD3}	—	40	ns	20.24, 20.25
Write strobe delay time 4		t_{WSD4}	—	40	ns	20.24, 20.25, 20.33
Write data delay time 1		t_{WDD1}	—	70	ns	20.22, 20.26, 20.27, 20.32
Write data delay time 2		t_{WDD2}	—	40	ns	20.24, 20.26
Write data hold time		t_{WDH}	–10	—	ns	20.22, 20.24–20.27, 20.32
Parity output delay time 1		t_{WPDD1}	—	80	ns	20.22, 20.24, 20.27
Parity output delay time 2		t_{WPDD2}	—	40	ns	20.24, 20.25
Parity output hold time		t_{WPDH}	–10	—	ns	20.22, 20.23–20.27

Table 20.8 Bus Timing (3) (cont)

Conditions: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 to 5.5 V, AV_{CC} = V_{CC} ±10%, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 12.5 MHz, Ta = –20 to +75°C*

Normal Products: Ta = –40 to +85°C for wide-temperature range products.

Item		Symbol	Min	Max	Unit	Figures
Wait setup time		t_{WTS}	40	—	ns	20.23, 20.28, 20.32
Wait hold time		t_{WTH}	10	—	ns	
Read data access time 1		t_{ACC1}	t_{cyc} – 44	—	ns	20.21, 20.24, 20.25
Read data access time 2		t_{ACC2}	$t_{cyc} \times (n+2) - 44$*2	—	ns	20.22, 20.23, 20.26, 20.28
$\overline{RAS}$ delay time 1		t_{RASD1}	—	40	ns	20.24–20.27, 20.29–20.31
$\overline{RAS}$ delay time 2		t_{RASD2}	—	40	ns	
$\overline{CAS}$ delay time 1		t_{CASD1}	—	40	ns	20.24
$\overline{CAS}$ delay time 2		t_{CASD2}	—	40	ns	20.26, 20.27, 20.29–20.31
$\overline{CAS}$ delay time 3		t_{CASD3}	—	40	ns	
Column address setup time		t_{ASC}	0	—	ns	20.24, 20.25
Read data access time from $\overline{CAS}$ 1	35% duty*1	t_{CAC1}	$t_{cyc} \times 0.65 - 35$	—	ns	
	50% duty		$t_{cyc} \times 0.5 - 35$	—	ns	
Read data access time from $\overline{CAS}$ 2		t_{CAC2}	$t_{cyc} \times (n+1) - 35$*2	—	ns	20.26, 20.27, 20.28
Read data access time from $\overline{RAS}$ 1		t_{RAC1}	$t_{cyc} \times 1.5 - 35$	—	ns	20.24, 20.25
Read data access time from $\overline{RAS}$ 2		t_{RAC2}	$t_{cyc} \times (n+2.5) - 35$*2	—	ns	20.26, 20.27, 20.28
High-speed page mode $\overline{CAS}$ precharge time		t_{CP}	$t_{cyc} \times 0.25$	—	ns	20.25
$\overline{AH}$ delay time 1		t_{AHD1}	—	40	ns	20.32
$\overline{AH}$ delay time 2		t_{AHD2}	—	40	ns	
Multiplexed address delay time		t_{MAD}	—	40	ns	
Multiplexed address hold time		t_{MAH}	–10	—	ns	

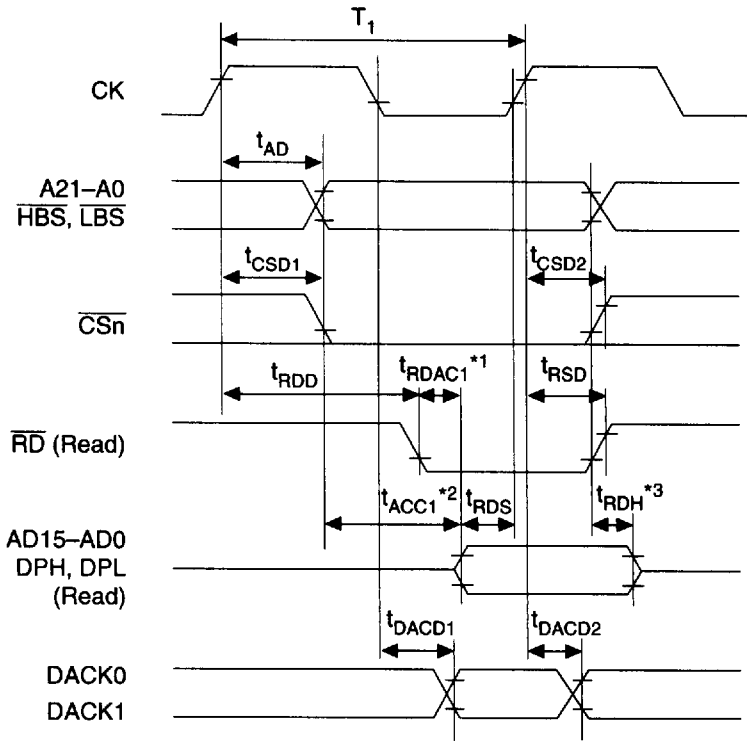
Table 20.8 Bus Timing (3) (cont)

Conditions: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 to 5.5 V, V_{CC} = AV_{CC} ±10%, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 12.5 MHz, Ta = –20 to +75°C*

Normal Products: Ta = –40 to +85°C for wide-temperature range products

Item		Symbol	Min	Max	Unit	Figures
DACK0, DACK1 delay time 1		t_{DACD1}	—	40	ns	20.21, 20.22, 20.24–20.27, 20.32, 20.33
DACK0, DACK1 delay time 2		t_{DACD2}	—	40	ns	
DACK0, DACK1 delay time 3		t_{DACD3}	—	40	ns	20.22, 20.26, 20.27, 20.32
DACK0, DACK1 delay time 4		t_{DACD4}	—	40	ns	20.24, 20.25
DACK0, DACK1 delay time 5		t_{DACD5}	—	40	ns	
Read delay time	35% duty*1	t_{RDD}	—	$t_{cyc} \times 0.35 + 35$	ns	20.21, 20.22, 20.24-20.28, 20.32
	50% duty		—	$t_{cyc} \times 0.5 + 35$	ns	
Data setup time for $\overline{CAS}$		t_{DS}	0*3	—	ns	20.24, 20.26
$\overline{CAS}$ setup time for $\overline{RAS}$		t_{CSR}	10	—	ns	20.29–20.31
Row address hold time		t_{RAH}	10	—	ns	20.24, 20.26
Write command hold time		t_{WCH}	15	—	ns	
Write command setup time	35% duty*1	t_{WCS}	0	—	ns	20.24
	50% duty	t_{WCS}	0	—	ns	
Access time from $\overline{CAS}$ precharge		t_{ACP}	tcyc –20	—	ns	20.25

Notes: 1. When frequency is 10 MHz or more.
2. n is the number of wait cycles.
3. –5 ns for parity output of DRAM long-pitch access

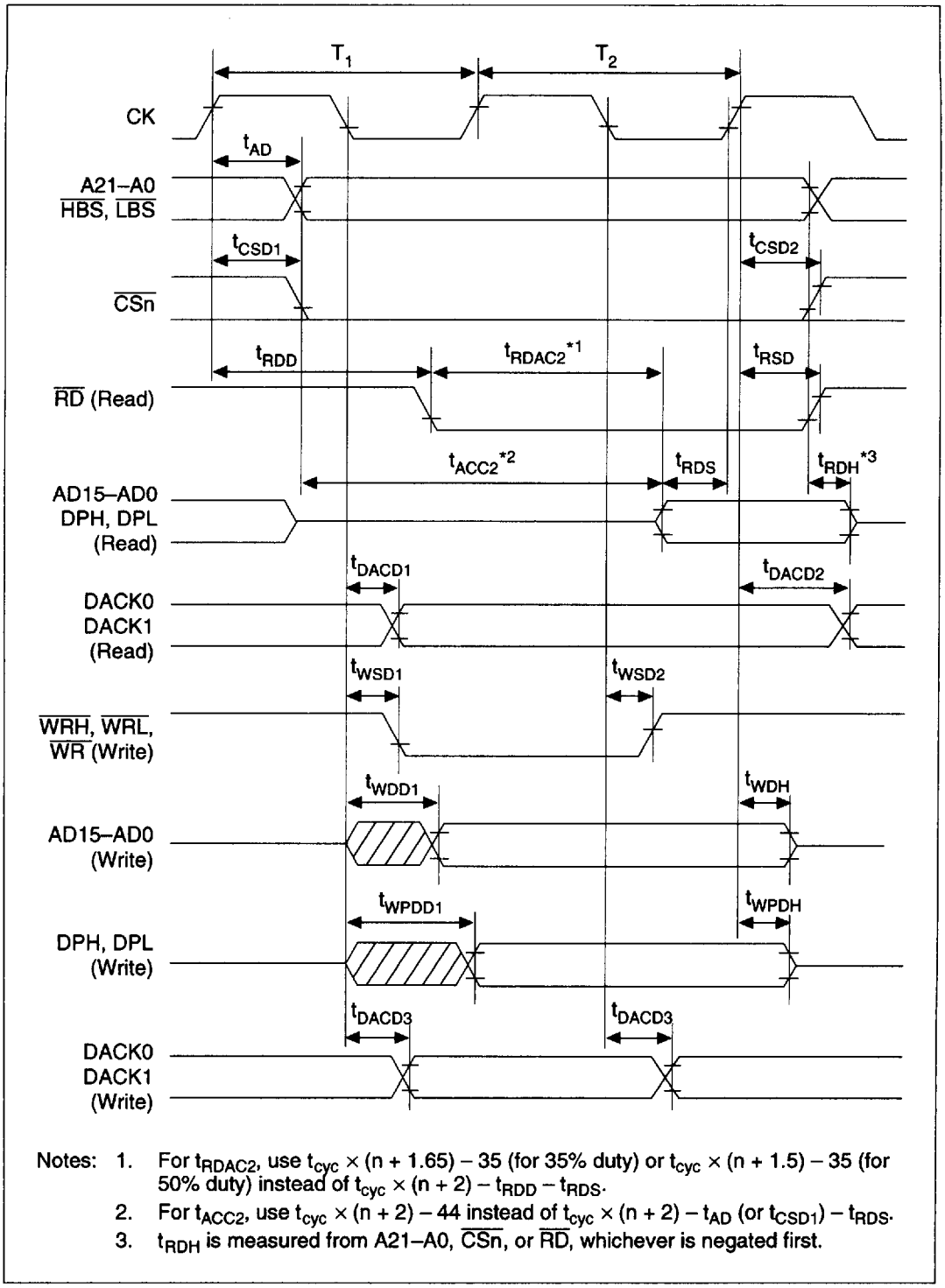


Notes: 1. For t_{RDAC1}, use $t_{cyc} \times 0.65 - 35$ (for 35% duty) or $t_{cyc} \times 0.5 - 35$ (for 50% duty) instead of $t_{cyc} - t_{RDD} - t_{RDS}$.

2. For t_{ACC1}, use $t_{cyc} - 44$ instead of $t_{cyc} - t_{AD}$ (or t_{CSD1}) $- t_{RDS}$.

3. t_{RDH} is measured from A21–A0, $\overline{CSn}$, or $\overline{RD}$, whichever is negated first.

Figure 20.21 Basic Bus Cycle: One-State Access

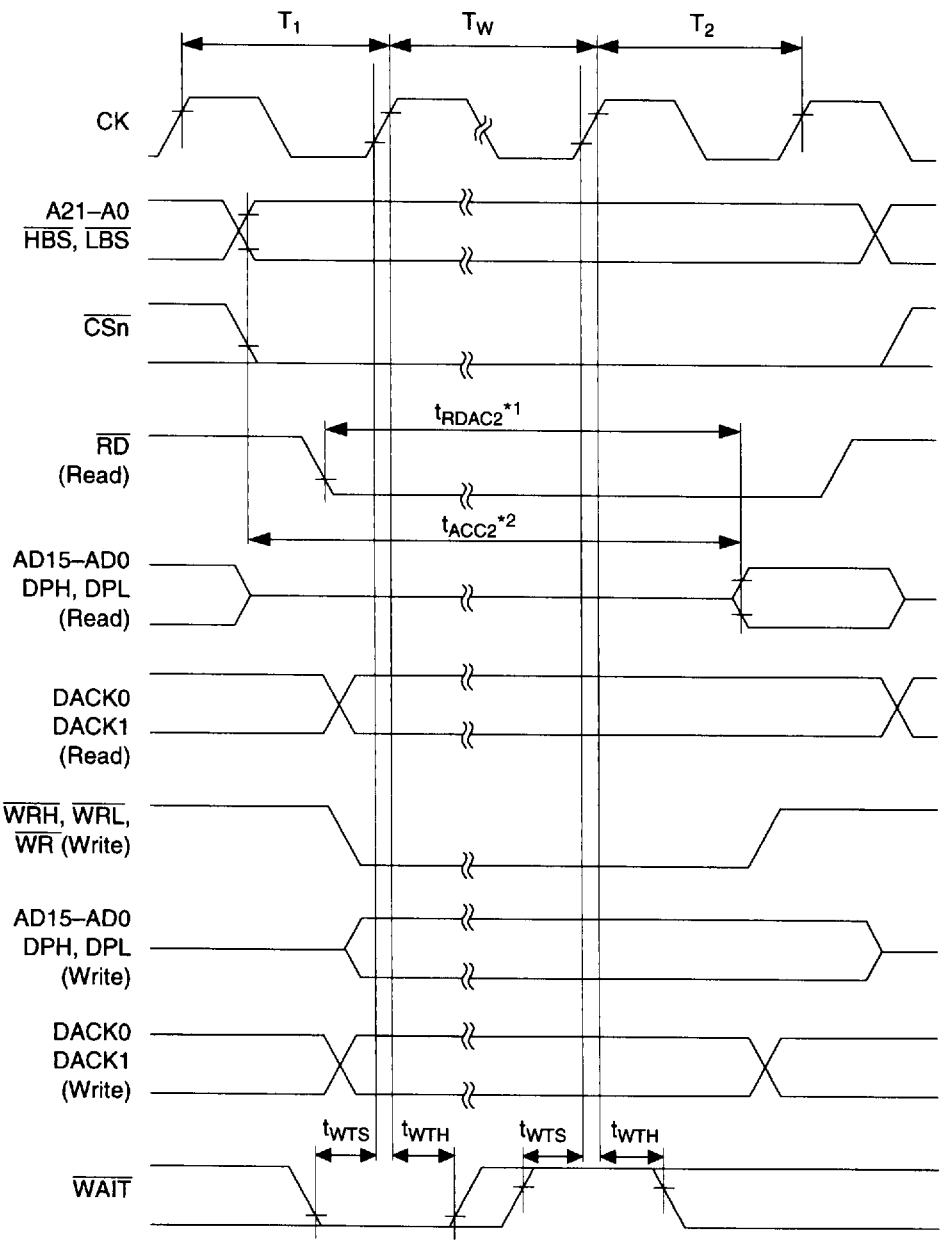


Notes: 1. For t_{RDAC2}, use $t_{cyc} \times (n + 1.65) - 35$ (for 35% duty) or $t_{cyc} \times (n + 1.5) - 35$ (for 50% duty) instead of $t_{cyc} \times (n + 2) - t_{RDD} - t_{RDS}$.

2. For t_{ACC2}, use $t_{cyc} \times (n + 2) - 44$ instead of $t_{cyc} \times (n + 2) - t_{AD}$ (or t_{CSD1}) $- t_{RDS}$.

3. t_{RDH} is measured from A21–A0, $\overline{CSn}$, or $\overline{RD}$, whichever is negated first.

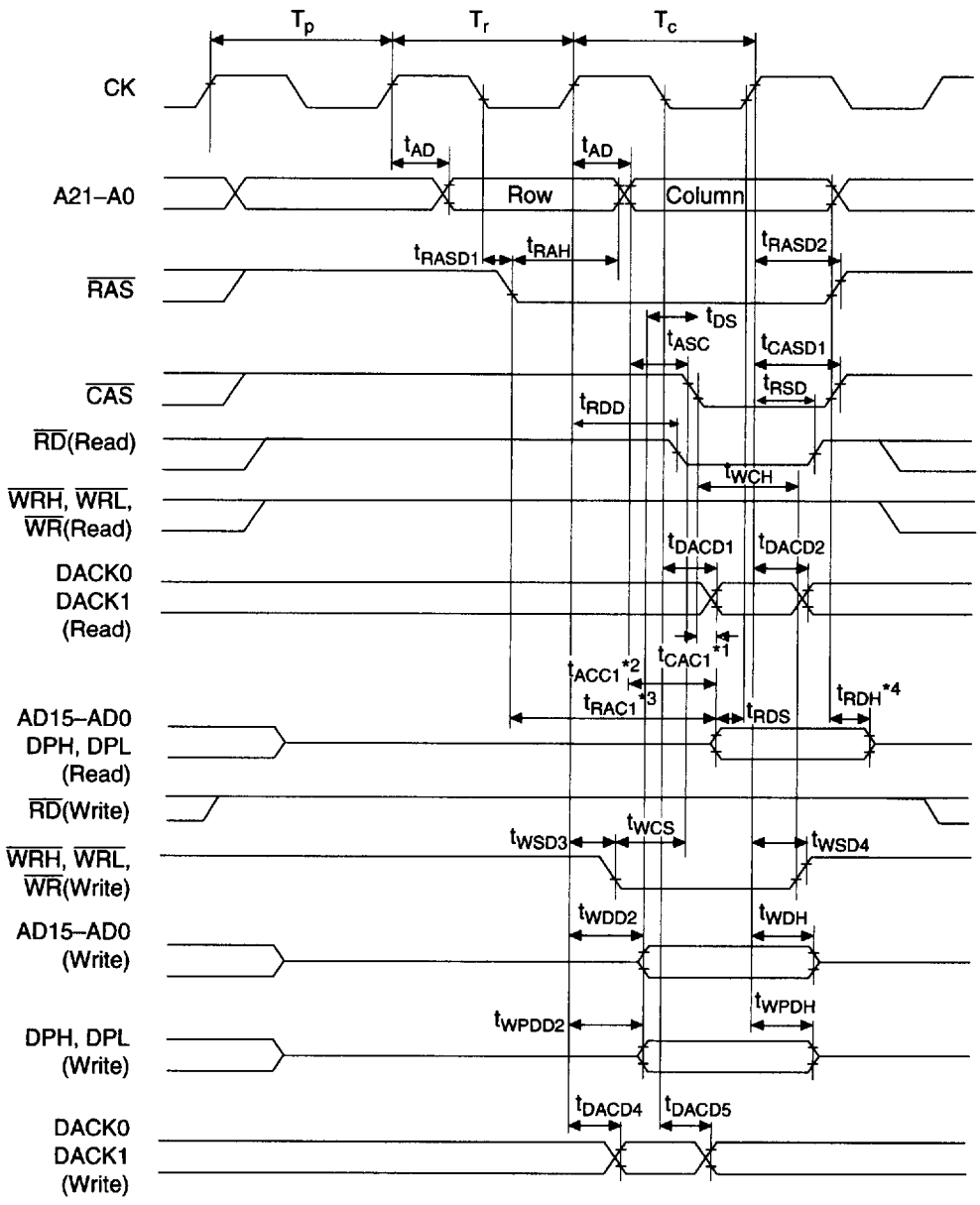
Figure 20.22 Basic Bus Cycle: Two-State Access



Notes: 1. For t_{RDAC2}, use $t_{cyc} \times (n + 1.65) - 35$ (for 35% duty) or $t_{cyc} \times (n + 1.5) - 35$ (for 50% duty) instead of $t_{cyc} \times (n + 2) - t_{RDD} - t_{RDS}$.

2. For t_{ACC2}, use $t_{cyc} \times (n + 2) - 44$ instead of $t_{cyc} \times (n + 2) - t_{AD}$ (or t_{CSD1}) $- t_{RDS}$.

Figure 20.23 Basic Bus Cycle: Two States + Wait State



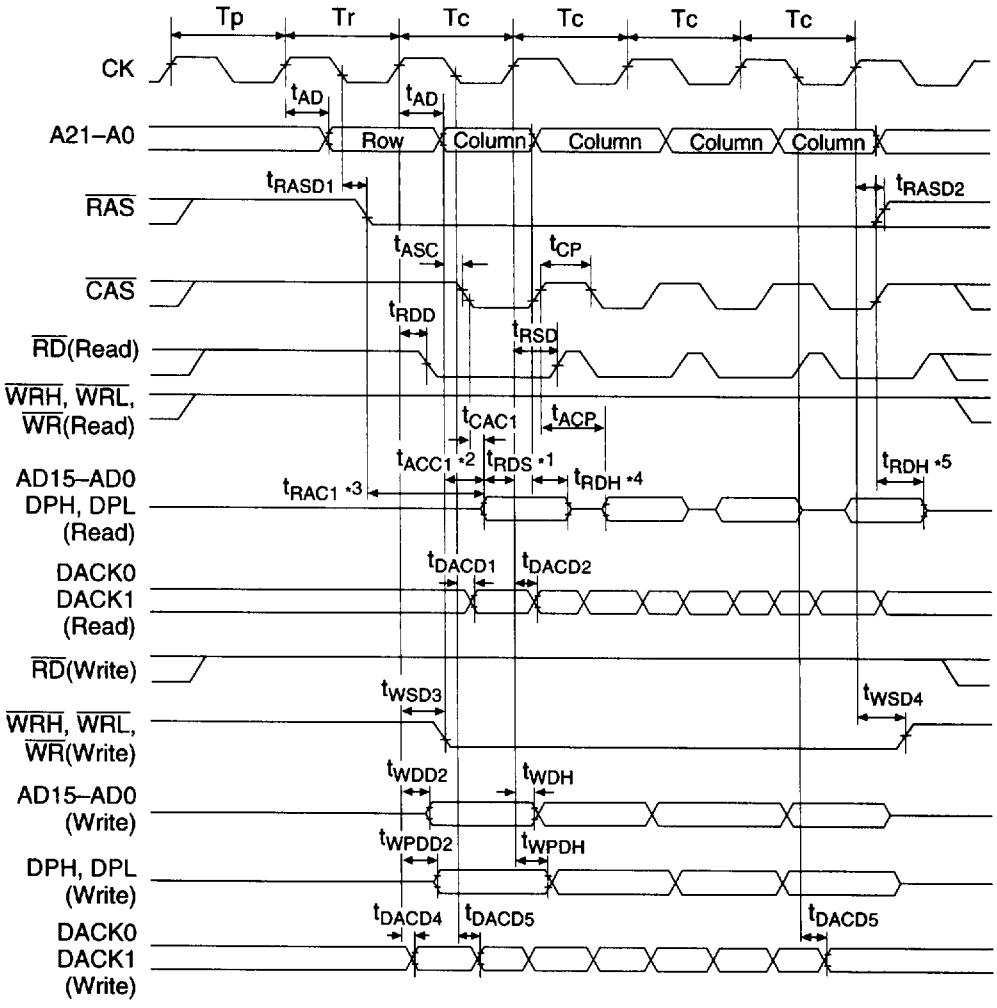
Notes: 1. For t_{CAC1}, use $t_{cyc} \times 0.65 - 35$ (for 35% duty) or tcyc $\times$ 0.5 – 35 (for 50% duty) instead of $t_{cyc} - t_{AD} - t_{ASC} - t_{RDS}$.

2. For t_{ACC1}, use $t_{cyc} - 44$ instead of $t_{cyc} - t_{AD} - t_{RDS}$.

3. For t_{RAC1}, use $t_{cyc} \times 1.5 - 35$ instead of $t_{cyc} \times 1.5 - t_{RASD1} - t_{RDS}$.

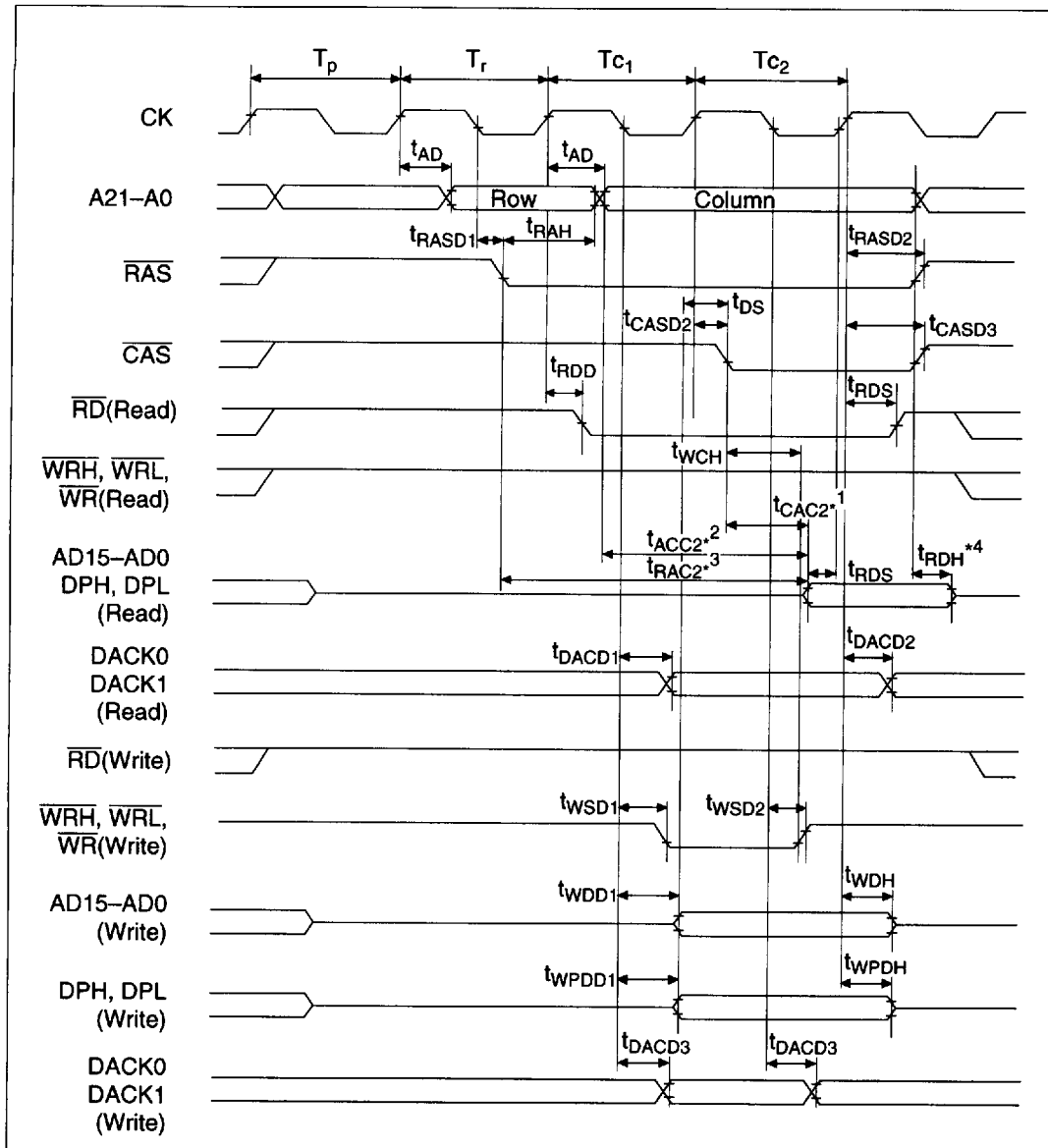
4. t_{RDH} is measured from A21–A0, $\overline{RAS}$, or $\overline{CAS}$, whichever is negated first.

Figure 20.24 DRAM Bus Cycle (Short Pitch, Normal Mode)



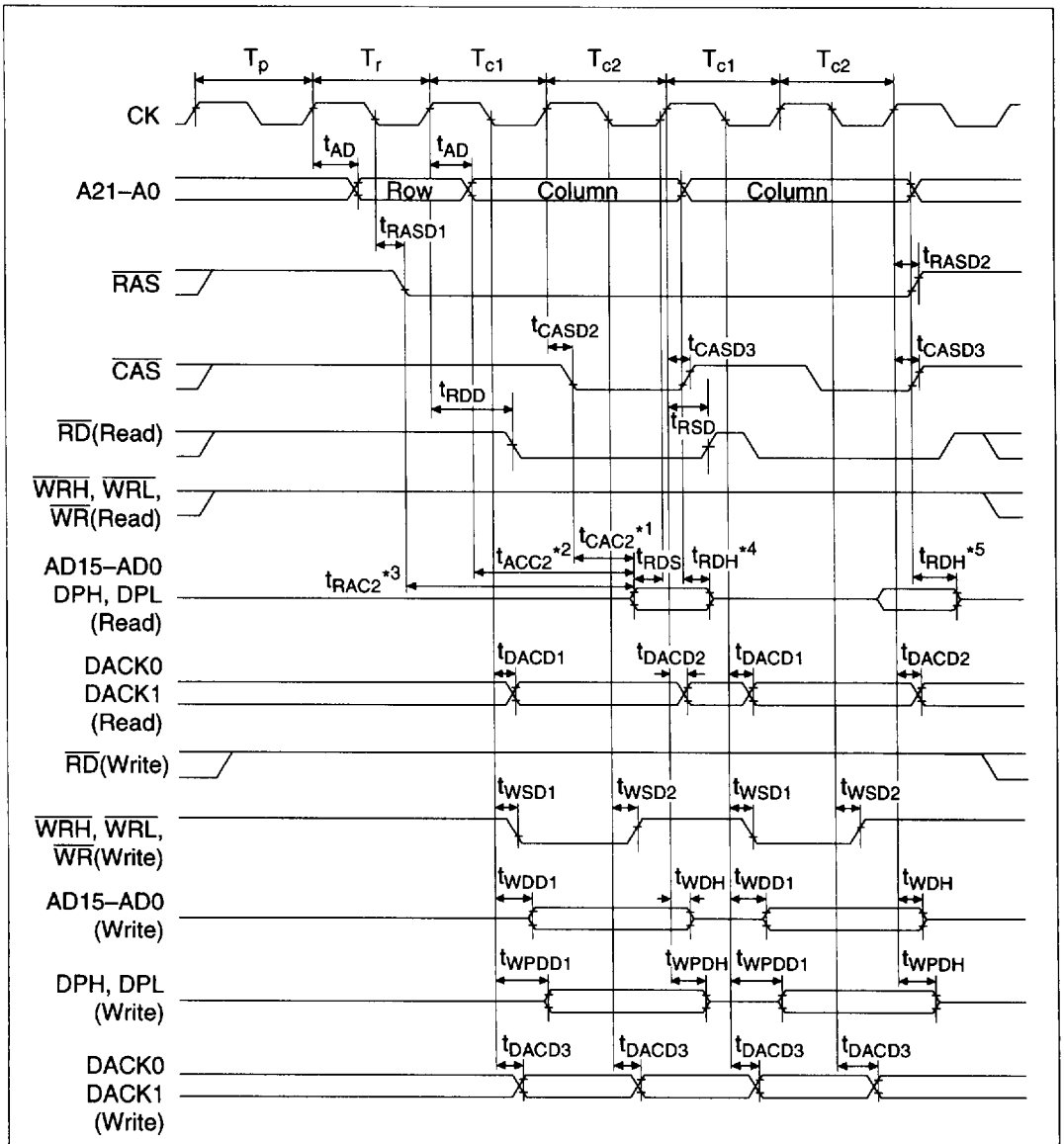
Notes:
1. For t_{CAC1}, use $t_{cyc} \times 0.65 - 35$ (for 35% duty) or $t_{cyc} \times 0.5 - 35$ (for 50% duty) instead of $t_{cyc} - t_{AD} - t_{ASC} - t_{RDS}$.
2. For t_{ACC1}, use $t_{cyc} - 44$ instead of $t_{cyc} - t_{AD} - t_{RDS}$.
3. For t_{RAC1}, use $t_{cyc} \times 1.5 - 35$ instead of $t_{cyc} \times 1.5 - t_{RASD1} - t_{RDS}$.
4. t_{RDH} is measured from A21–A0 or $\overline{CAS}$, whichever is negated first.
5. t_{RDH} is measured from A21–A0, $\overline{RAS}$, or $\overline{CAS}$, whichever is negated first.

Figure 20.25 DRAM Bus Cycle (Short Pitch, High-Speed Page Mode)



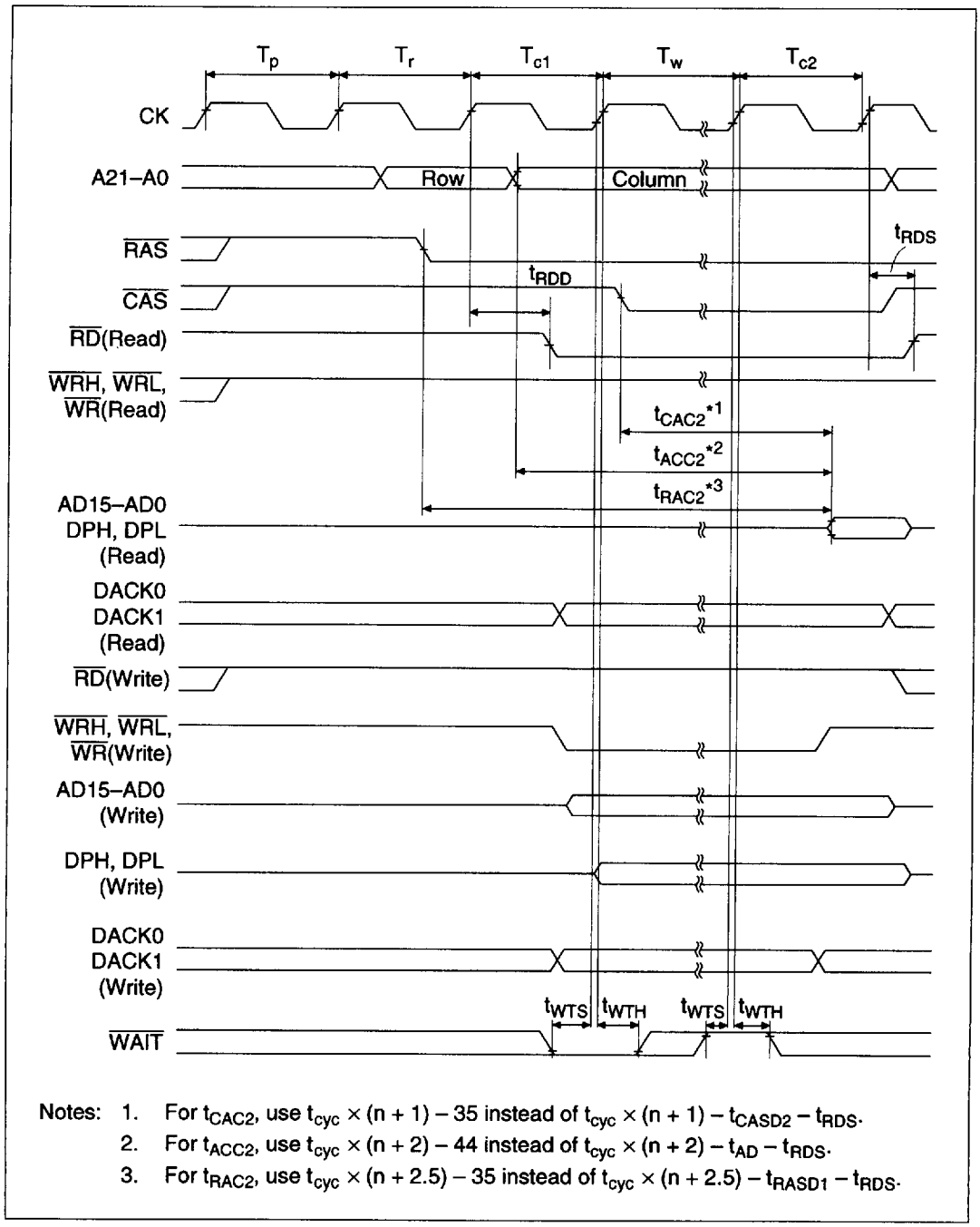
Notes: 1. For t_{CAC2}, use $t_{cyc} \times (n + 1) - 35$ instead of $t_{cyc} \times (n + 1) - t_{CASD2} - t_{RDS}$.
2. For t_{ACC2}, use $t_{cyc} \times (n + 2) - 44$ instead of $t_{cyc} \times (n + 2) - t_{AD} - t_{RDS}$.
3. For t_{RAC2}, use $t_{cyc} \times (n + 2.5) - 35$ instead of $t_{cyc} \times (n + 2.5) - t_{RASD1} - t_{RDS}$.
4. t_{RDH} is measured from A21–A0, $\overline{CAS}$, or $\overline{RAS}$, whichever is negated first.

Figure 20.26 DRAM Bus Cycle: (Long Pitch, Normal Mode)



Notes:
1. For t_{CAC2}, use $t_{cyc} \times (n + 1) - 35$ instead of $t_{cyc} \times (n + 1) - t_{CASD2} - t_{RDS}$.
2. For t_{ACC2}, use $t_{cyc} \times (n + 2) - 44$ instead of $t_{cyc} \times (n + 2) - t_{AD} - t_{RDS}$.
3. For t_{RAC2}, use $t_{cyc} \times (n + 2.5) - 35$ instead of $t_{cyc} \times (n + 2.5) - t_{RASD1} - t_{RDS}$.
4. t_{RDH} is measured from A21–A0 or $\overline{CAS}$, whichever is negated first.
5. t_{RDH} is measured from A21–A0, $\overline{RAS}$, or $\overline{CAS}$ whichever is negated first.

Figure 20.27 DRAM Bus Cycle: (Long Pitch, High-Speed Page Mode)



Notes: 1. For t_{CAC2}, use $t_{cyc} \times (n + 1) - 35$ instead of $t_{cyc} \times (n + 1) - t_{CASD2} - t_{RDS}$.
2. For t_{ACC2}, use $t_{cyc} \times (n + 2) - 44$ instead of $t_{cyc} \times (n + 2) - t_{AD} - t_{RDS}$.
3. For t_{RAC2}, use $t_{cyc} \times (n + 2.5) - 35$ instead of $t_{cyc} \times (n + 2.5) - t_{RASD1} - t_{RDS}$.

Figure 20.28 DRAM Bus Cycle: (Long Pitch, High-Speed Page Mode + Wait State)

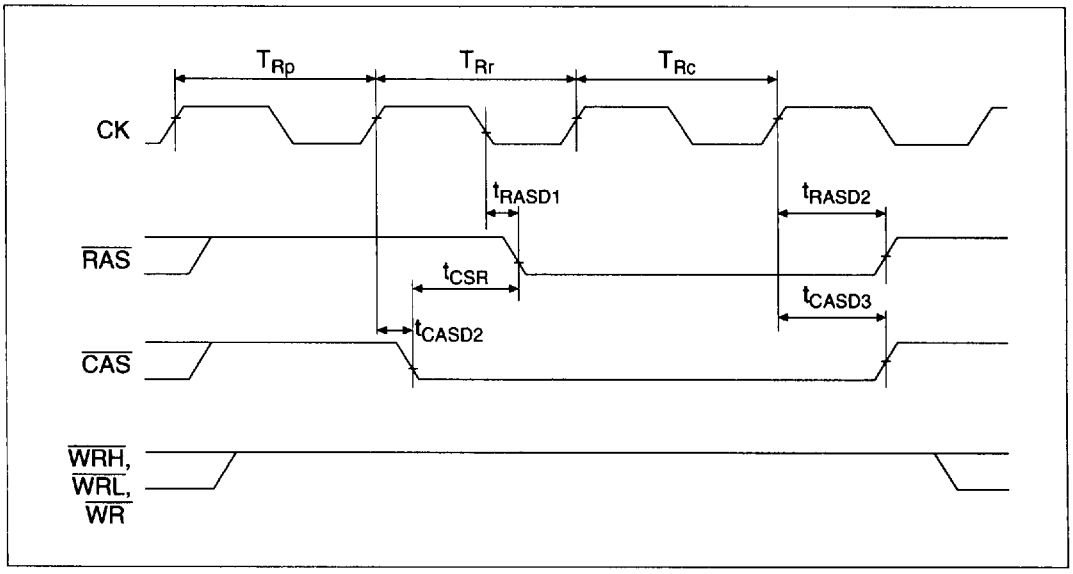


Figure 20.29 CAS-before-RAS Refresh (Short Pitch)

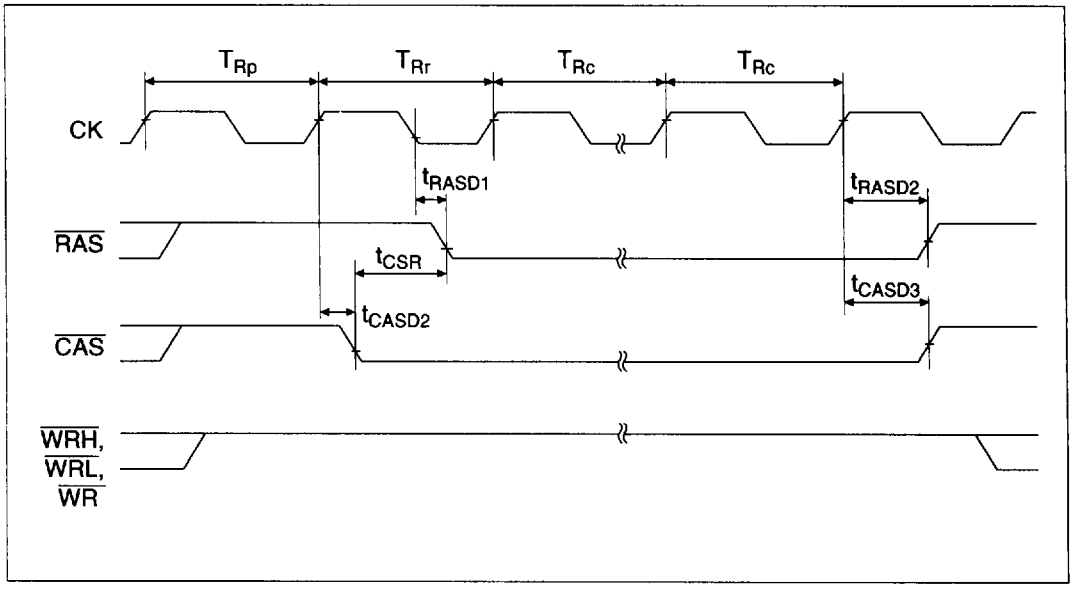


Figure 20.30 CAS-before-RAS Refresh (Long Pitch)

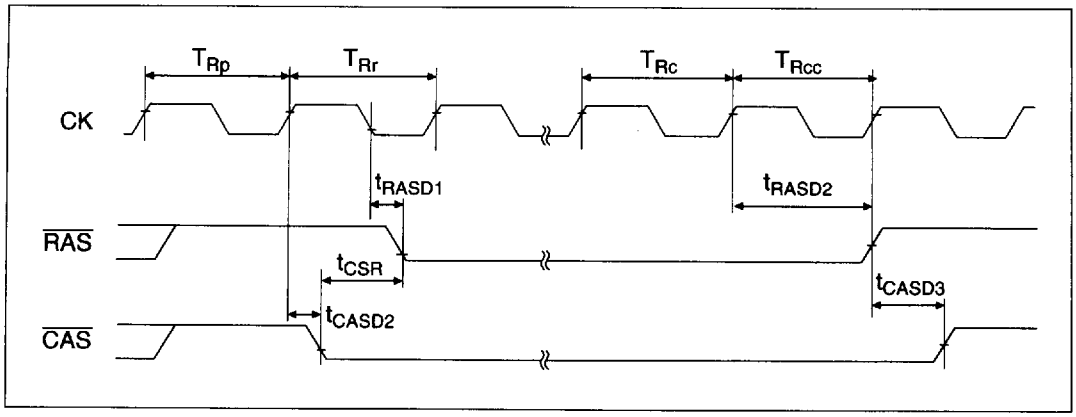


Figure 20.31 Self Refresh

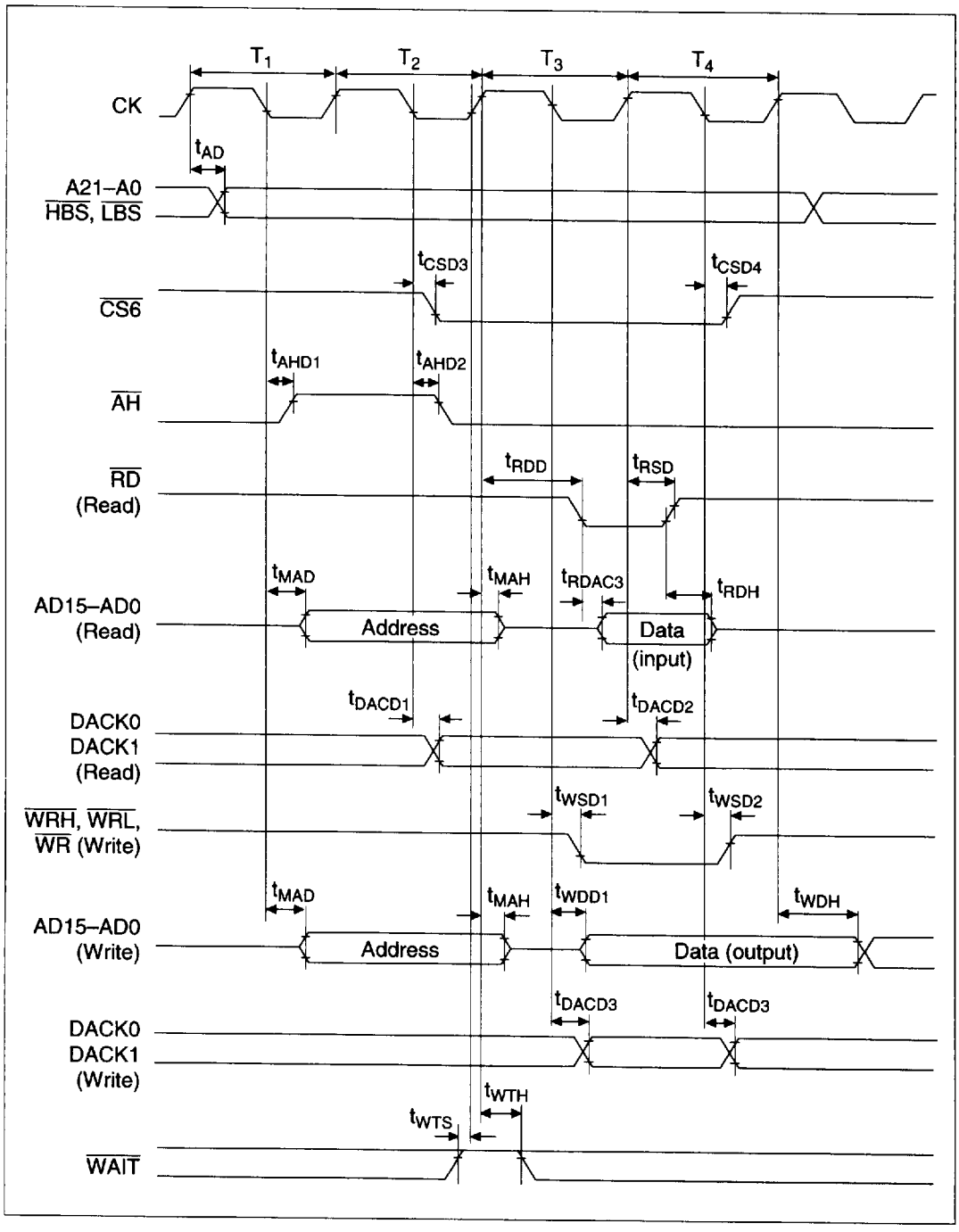


Figure 20.32 Address/Data Multiplex I/O Bus Cycle

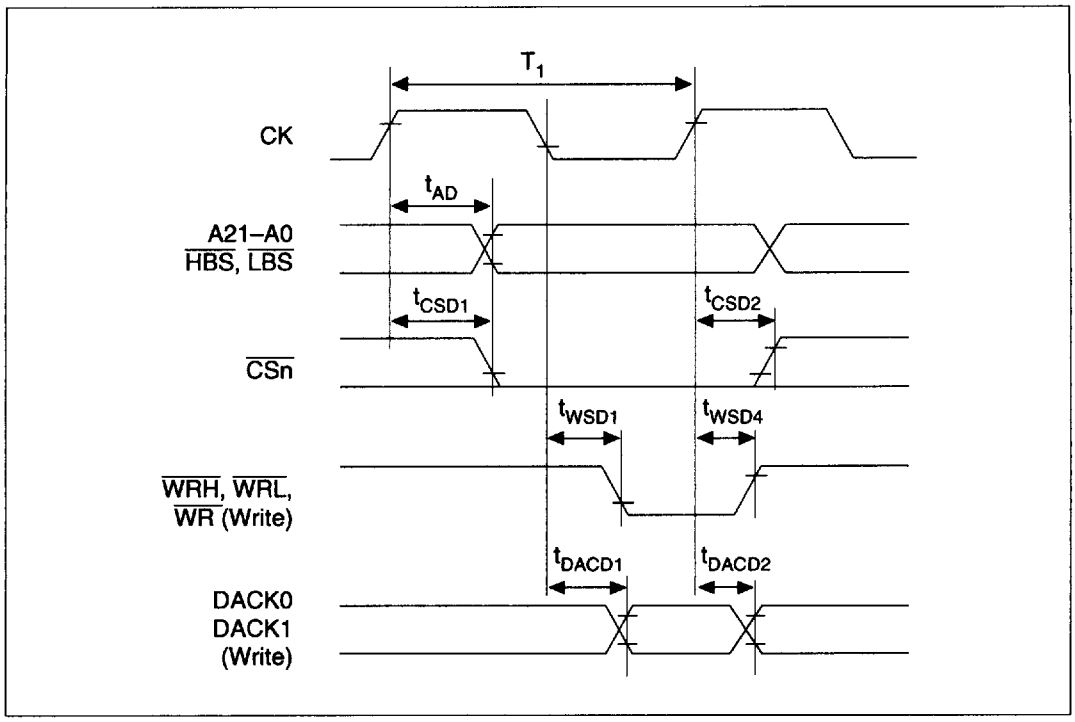


Figure 20.33 DMA Single Transfer/Single State Access Write

20.3.4 DMAC Timing

Table 20.9 DMAC Timing

Case A: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 to 5.5 V, AV_{CC} = V_{CC} ±10%, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*

Case B: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*

Normal Products: Ta = –40 to +85°C for wide-temperature range products.

		Case A		Case B					
		12.5 MHz		16.6 MHz		20 MHz			
Item	Symbol	Min	Max	Min	Max	Min	Max	Unit	Figure
$\overline{DREQ0}$, $\overline{DREQ1}$ setup time	t_{DRQS}	80	—	40	—	27	—	ns	20.34
$\overline{DREQ0}$, $\overline{DREQ1}$ hold time	t_{DRQH}	30	—	30	—	30	—	ns	
$\overline{DREQ0}$, $\overline{DREQ1}$ low level width	t_{DRQW}	1.5	—	1.5	—	1.5	—	t_{cyc}	20.35

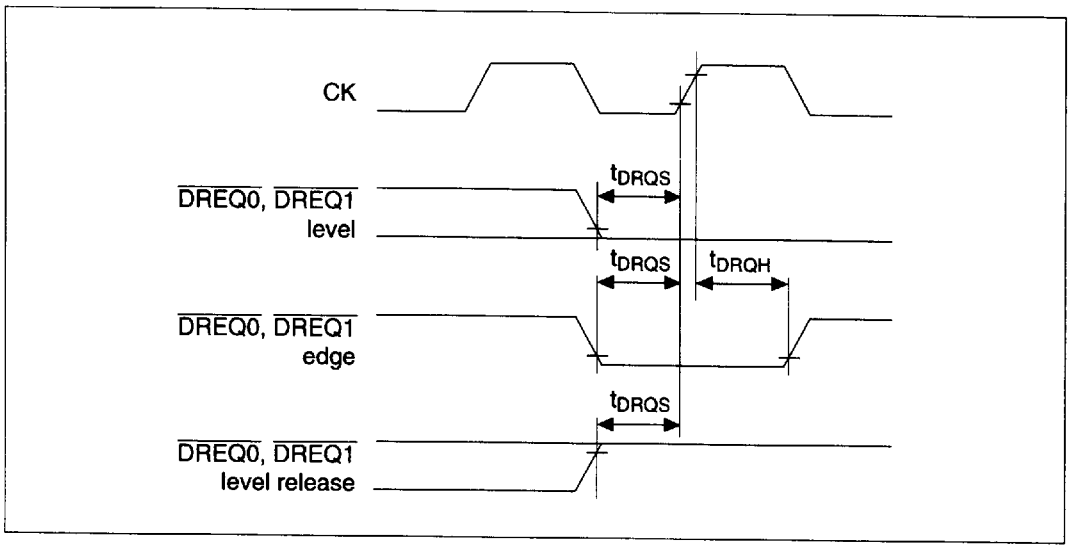


Figure 20.34 $\overline{\text{DREQ0}}$, $\overline{\text{DREQ1}}$ Input Timing (1)

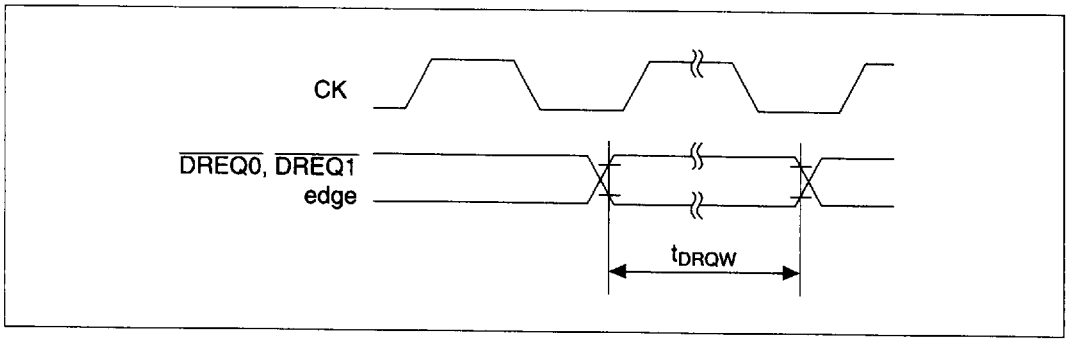


Figure 20.35 $\overline{\text{DREQ0}}$, $\overline{\text{DREQ1}}$ Input Timing (2)

20.3.5 16-bit Integrated Timer Pulse Unit Timing

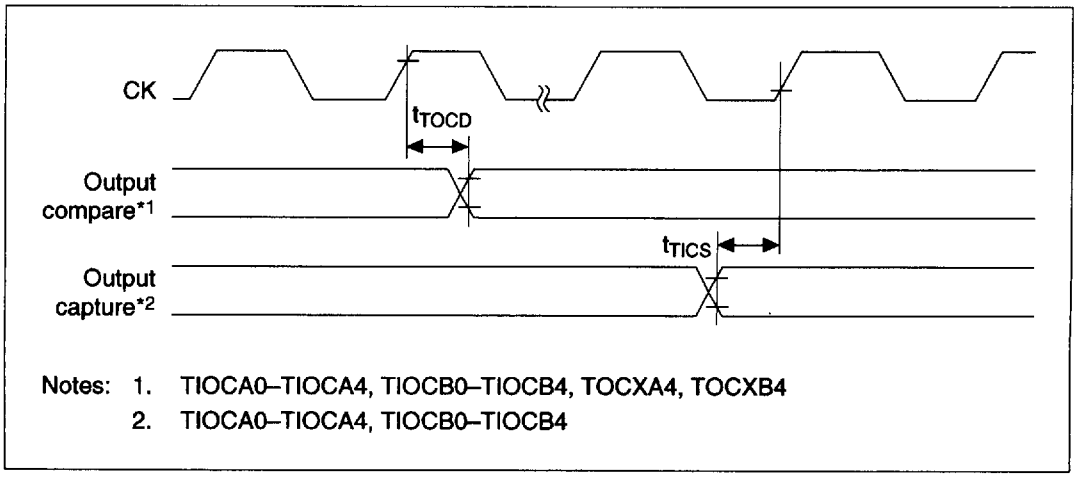
Table 20.10 16-bit Integrated Timer Pulse Unit Timing

Case A: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 to 5.5 V, AV_{CC} = V_{CC} ±10%, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*

Case B: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*

Normal Products: Ta = –40 to +85°C for wide-temperature range products.

		Case A		Case B					
		12.5 MHz		16.6 MHz		20 MHz			
Item	Symbol	Min	Max	Min	Max	Min	Max	Unit	Figure
Output compare delay time	t_{TOCD}	—	100	—	100	—	100	ns	20.36
Input capture setup time	t_{TICS}	50	—	45	—	35	—	ns	
Timer clock input setup time	t_{TCKS}	50	—	50	—	50	—	ns	20.37
Timer clock pulse width (single edge)	$t_{TCKWH/L}$	1.5	—	1.5	—	1.5	—	t_{cyc}	
Timer clock pulse width (both edges)	$t_{TCKWL/L}$	2.5	—	2.5	—	2.5	—	t_{cyc}	



Notes: 1. TIOCA0–TIOCA4, TIOCB0–TIOCB4, TOCXA4, TOCXB4
2. TIOCA0–TIOCA4, TIOCB0–TIOCB4

Figure 20.36 ITU Input/Output Timing

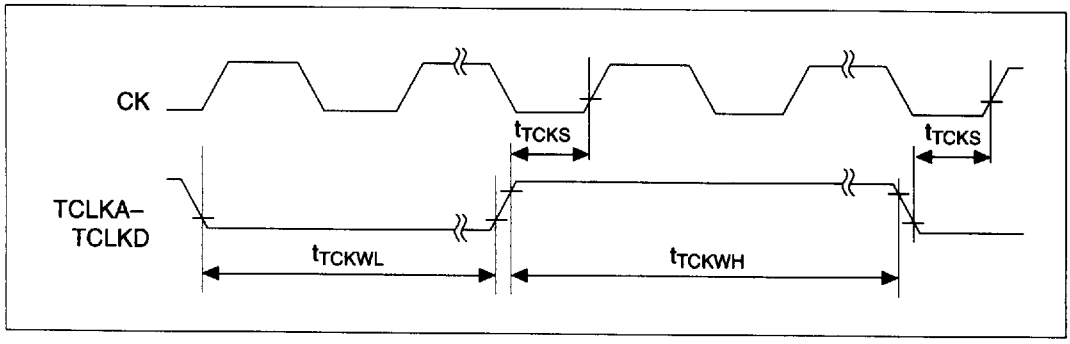


Figure 20.37 ITU Clock Input Timing

20.3.6 Programmable Timing Pattern Controller and I/O Port Timing

Table 20.11 Programmable Timing Pattern Controller and I/O Port Timing

Case A: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 to 5.5 V, AV_{CC} = V_{CC} ±10%, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 12.5 MHz, Ta = –20 to +75°C*

Case B: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 16.6 MHz, Ta = –20 to +75°C*

Case C: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 20 MHz, Ta = –20 to +75°C*

Normal Products: Ta = –40 to +85°C for wide-temperature range products.

		Cases A, B and C			
Item	**Symbol**	**Min**	**Max**	**Unit**	**Figure**
Port output delay time	t_{PWD}	—	100	ns	20.38
Port input hold time	t_{PRH}	50	—	ns	
Port input setup time	t_{PRS}	50	—	ns	

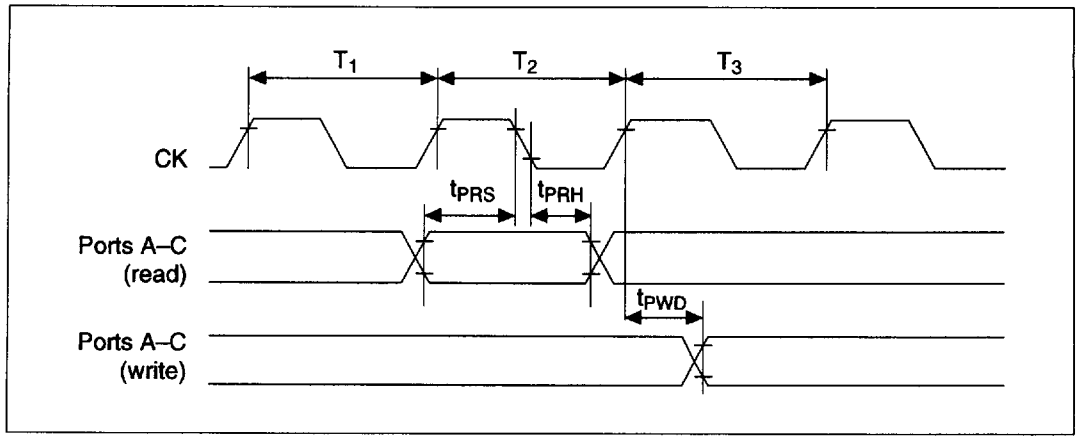


Figure 20.38 Programmable Timing Pattern Controller Output Timing

20.3.7 Watchdog Timer Timing

Table 20.12 Watchdog Timer Timing

Case A: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 to 5.5 V, AV_{CC} = V_{CC} ±10%, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 12.5 MHz, Ta = –20 to +75°C*

Case B: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 16.6 MHz, Ta = –20 to +75°C*

Case C: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 20 MHz, Ta = –20 to +75°C*

Normal Products: Ta = –40 to +85°C for wide-temperature range products.

		Cases A, B and C			
Item	**Symbol**	**Min**	**Max**	**Unit**	**Figure**
$\overline{\text{WDTOVF}}$ delay time	t_{WOVD}	—	100	ns	20.39

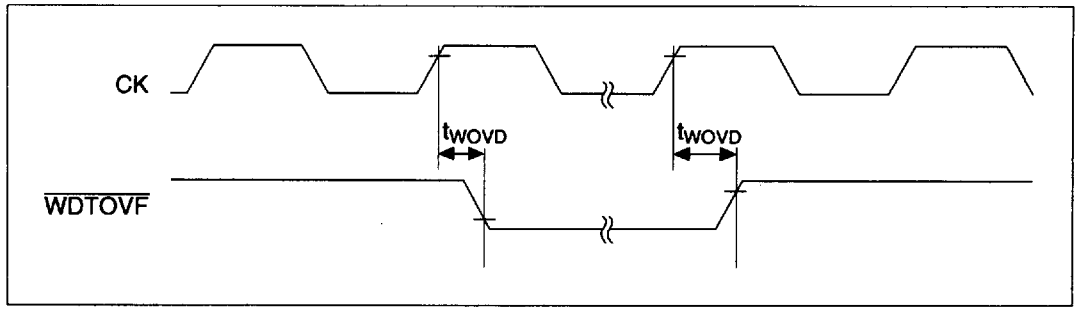


Figure 20.39 Watchdog Timer Output Timing

20.3.8 Serial Communications Interface Timing

Table 20.13 Serial Communications Interface Timing

Case A: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 to 5.5 V, AV_{CC} = V_{CC} ±10%, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 12.5 MHz, Ta = –20 to +75°C*

Case B: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 16.6 MHz, Ta = –20 to +75°C*

Case C: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, f = 20 MHz, Ta = –20 to +75°C*

Normal Products: Ta = –40 to +85°C for wide-temperature range products.

		Cases A, B and C			
Item	**Symbol**	**Min**	**Max**	**Unit**	**Figure**
Input clock cycle	t_{Scyc}	4	—	t_{cyc}	20.40
Input clock cycle (clocked synchronization)	t_{Scyc}	6	—	t_{cyc}	
Input clock pulse width	t_{Sckw}	0.4	0.6	t_{Scyc}	
Input clock rise time	t_{Sckr}	—	1.5	t_{cyc}	
Input clock fall time	t_{Sckf}	—	1.5	t_{cyc}	
Transmission data delay time (clocked synchronization)	t_{TXD}	—	100	ns	20.41
Receive data setup time (clocked synchronization)	t_{RXS}	100	—	ns	
Receive data hold time (clocked synchronization)	t_{RXH}	100	—	ns	

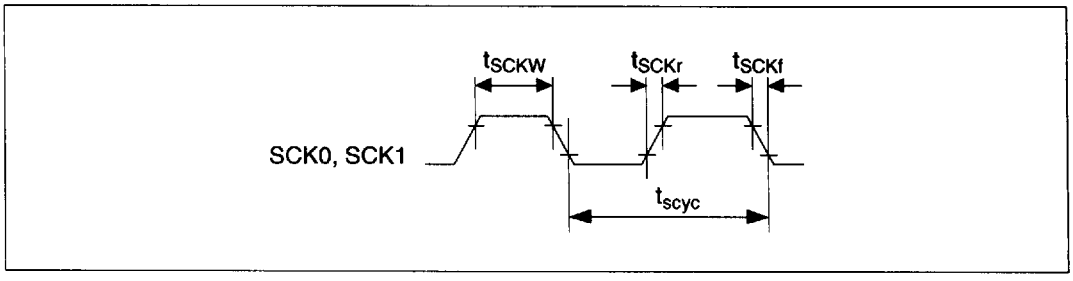


Figure 20.40 Input Clock Timing

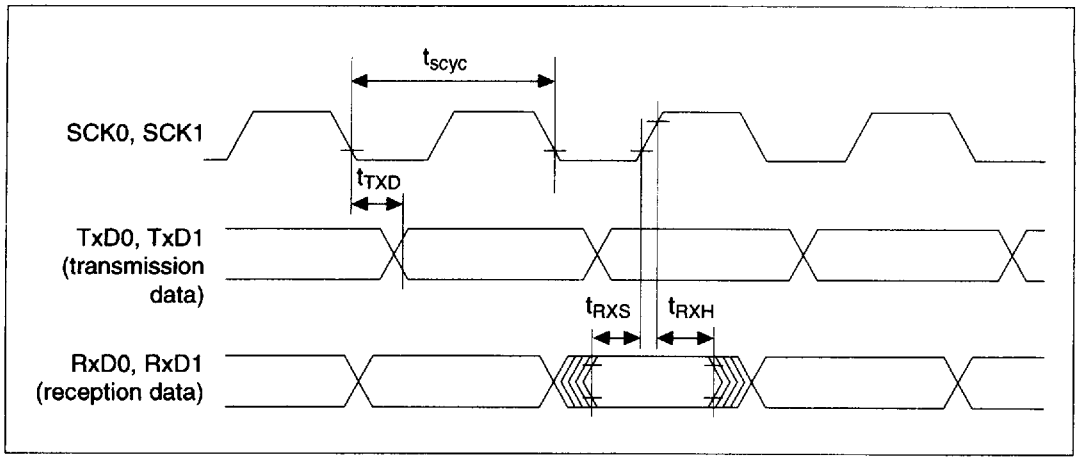


Figure 20.41 SCI I/O Timing (Clocked Synchronization Mode)

20.3.9 A/D Converter Timing

Table 20.14 A/D Converter Timing

Case A: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 to 5.5 V, AV_{CC} = V_{CC} ±10%, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 12.5 MHz, Ta = –20 to +75°C*

Case B: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 16.6 MHz, Ta = –20 to +75°C*

Case C: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 20 MHz, Ta = –20 to +75°C*

Normal Products: Ta = –40 to +85°C for wide-temperature range products.

		Cases A, B and C			
Item	**Symbol**	**Min**	**Max**	**Unit**	**Figure**
External trigger input start delay time	t_{TRGS}	50	—	ns	20.42
A/D converter time (266 cycles)	t_{CONV}	—	266	t_{cyc}	20.43
A/D converter time (134 cycles)	t_{CONV}	—	134	t_{cyc}	
$\overline{\text{ADTRG}}$ pulse width	t_{TRGW}	2.0	—	t_{cyc}	20.42

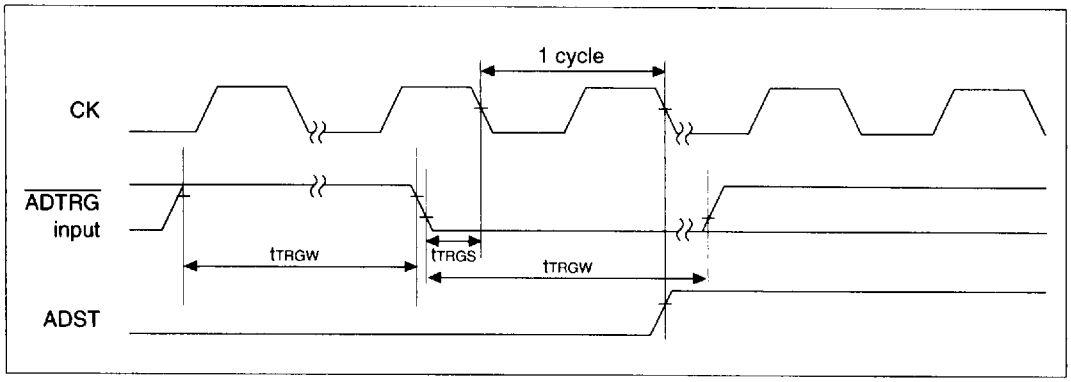


Figure 20.42 External Trigger Input Timing

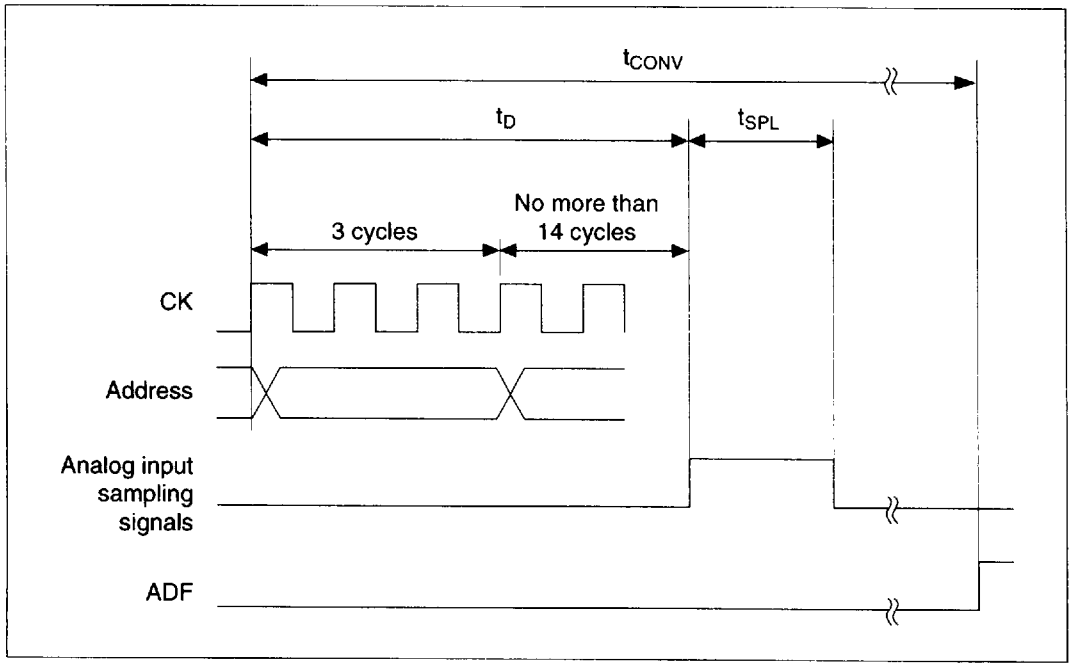
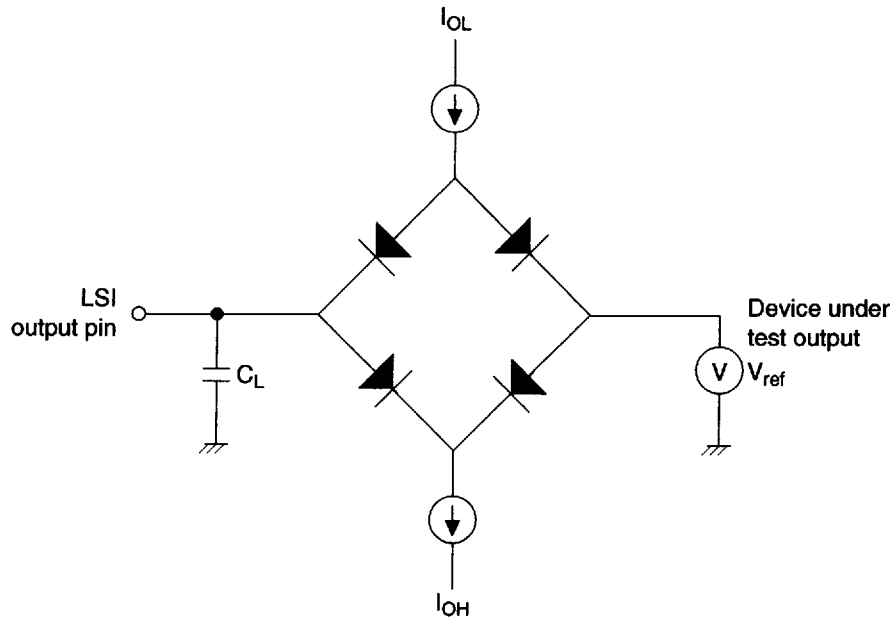


Figure 20.43 Analog Conversion Timing

20.3.10 AC Characteristics Measurement Conditions



C_L is set as follows for each pin.
30pF: CK, $\overline{\text{CASH}}$, $\overline{\text{CASL}}$, $\overline{\text{CS0}}$–$\overline{\text{CS7}}$, $\overline{\text{BREQ}}$, $\overline{\text{BACK}}$, $\overline{\text{AH}}$, $\overline{\text{LRQOUT}}$, $\overline{\text{RAS}}$, DACK0, DACK1
50pF: A21–A0, AD15–AD0, DPH, DPL, $\overline{\text{RD}}$, $\overline{\text{WRH}}$, $\overline{\text{WRL}}$, $\overline{\text{HBS}}$, $\overline{\text{LBS}}$, $\overline{\text{WR}}$
70pF: All port outputs and peripheral module output pins other than the above.
I_{OL} and I_{OH} values are as shown in section 20.2, DC Characteristics, and table 20.3, Permitted Output Current Values.

Figure 20.44 Output Load Circuit

20.4 A/D Converter Characteristics

Table 20.15 A/D Converter Characteristics (1)

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*

Normal Products: Ta = –40 to +85°C for wide-temperature range products.

	12.5 MHz			16.6 MHz			20 MHz			
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	10	10	10	10	10	10	bit
Conversion time	—	—	11.2	—	—	8.4	—	—	6.7	µS
Analog input capacitance	—	—	20	—	—	20	—	—	20	pF
Permissible signal-source impedance	—	—	3	—	—	3	—	—	3	kΩ
Nonlinearity error	—	—	±3	—	—	±3	—	—	±3	LSB
Offset error	—	—	±3	—	—	±3	—	—	±3	LSB
Full-scale error	—	—	±3	—	—	±3	—	—	±3	LSB
Quantization error	—	—	±0.5	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±4	—	—	±4	—	—	±4	LSB

Table 20.15 A/D Converter Characteristics (2)

Conditions: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 to 5.5 V, AV_{CC} = V_{CC} ±10%, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*

Normal Products: Ta = –40 to +85°C for wide-temperature range products.

	12.5 MHz			
Item	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	bit
Conversion time	—	—	11.2	µS
Analog input capacitance	—	—	20	pF
Permissible signal-source impedance	—	—	3	kΩ
Nonlinearity error	—	—	±4.0	LSB
Offset error	—	—	±4.0	LSB
Full-scale error	—	—	±4.0	LSB
Quantization error	—	—	±0.5	LSB
Absolute accuracy	—	—	±6.0	LSB

20.5 Usage Note

The ZTAT version and the mask ROM version satisfy the electrical properties given in this document. However, effective values of the electrical properties, the operating margin, and the noise margin may differ with the manufacturing processes, on-chip ROM, and layout patterns. When conducting a system evaluation test using the ZTAT version, conduct a similar evaluation test of the mask ROM version before it replaces the ZTAT version.