HA16686MP

Read Pulse Generator

Description

The HA16686MP generates a digital read data signal from the read signal output by a hard disk drive. It is a one-chip version of the HA16676MP read data generator and the HA16663 read pulse generator.

Preamplified signals from the magnetic head are passed through an AGC, then through a filter and differentiator to generate the output signal. A gate signal for the read data is also generated.

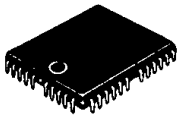
Features

- Transfer rates up to 10 Mbps
- AGC input amplifier ensures stable reproduction independent of media or head type.
- AGC can be disabled when writing
- AGC output can be fixed for servo feedback, and differential amplifier for peak hold detection
- Digital read data output is TTL compatible
- Compact surface-mount package
- Use with the HA16652P/MP, HA16688MP, HA16689MP HDD R/W circuit for compact HDD controller board designs

Ordering Information

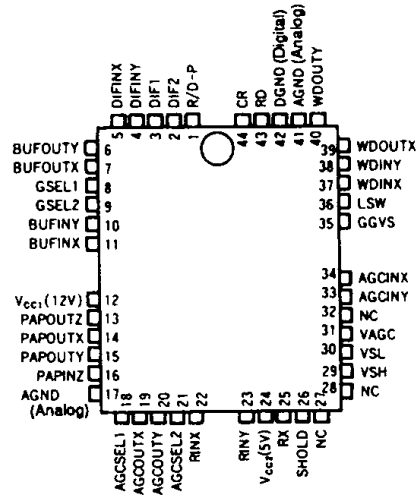
Type No.	Package
HA16686MP	MP-44

HA16686MP



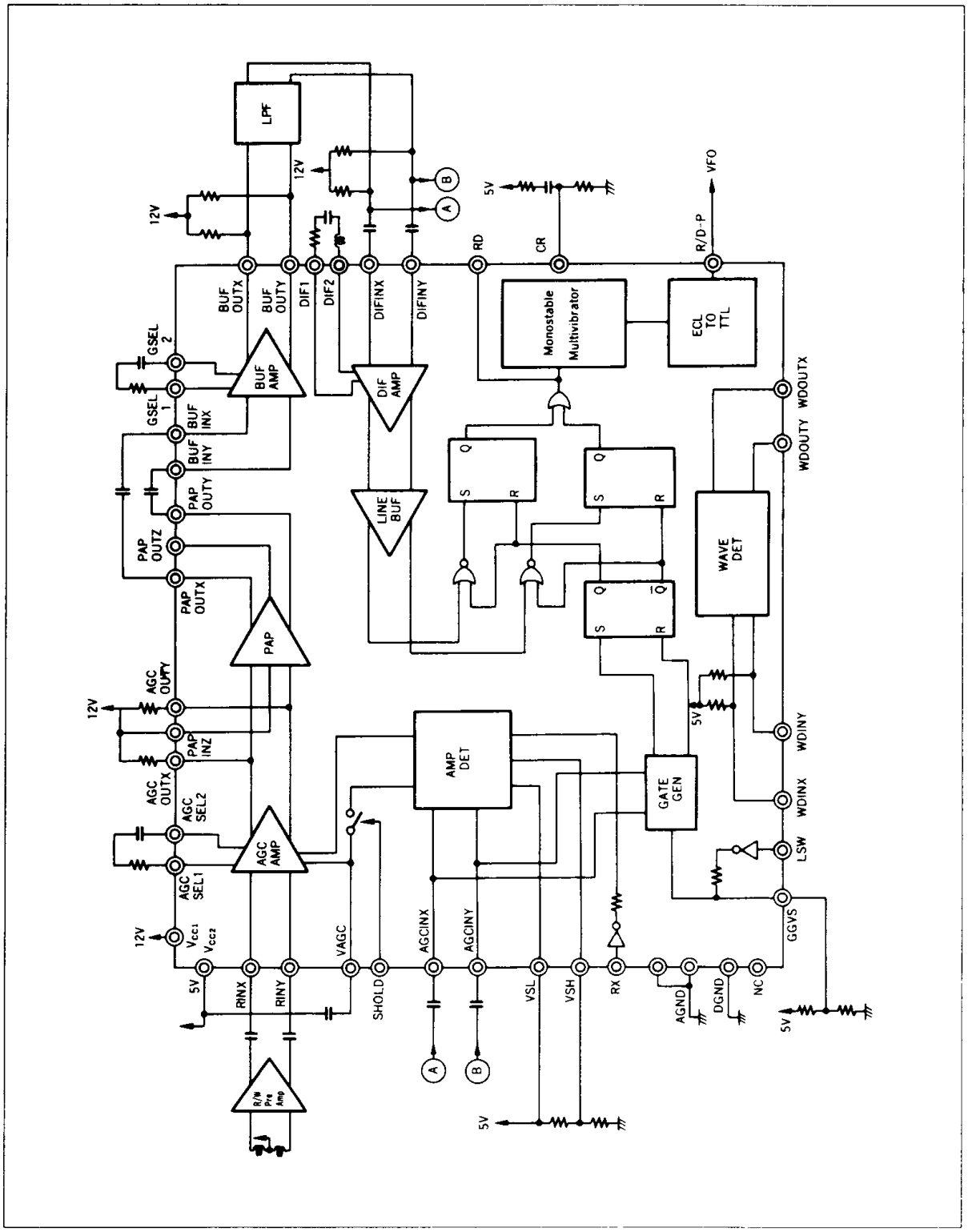
(MP-44)

Pin Assignment



Top View

Block Diagram



Pin Descriptions

Type	Pin No.	Name	Function
Power supply	12	V_{CC1}	+12 V power supply (analog)
	24	V_{CC2}	+5 V power supply (digital)
	17, 41	AGND	Analog GND
	42	DGND	Digital GND
Inputs	22	RINX	Differential inputs for read signal from disk drive
	23	RINY	
	10	BUFINY	Differential inputs for buffer amplifier to lowpass filter
	11	BUFINX	
	5	DIFINX	Differential inputs for differentiating amplifier
	4	DIFINY	
	34	AGCINX	Differential inputs for AGC output amplitude detector
	33	AGCINY	
	30	VSL	AGC amplitude detector low-level slice voltage—corresponds to discharge current threshold
	29	VSH	AGC amplitude detector high-level slice voltage—corresponds to charge current threshold
	25	RX	AGC loop on/off select RX = High: AGC loop off (minimum AGC loop gain) RX = Low: AGC loop on
	26	SHOLD	Constant AGC gain select (low input fixes gain)
	35	GGVS	Gate generator voltage slice level
	36	LSW	GGVS level select (V_{GGVS} lowered by 0.2 V when input is high)
	37	WDINX	Differential inputs for peak hold bandwidth amplifier (internally biased)
	38	WDINY	
Outputs	19	AGCOUTX	Differential outputs from AGC (open collector)
	20	AGCOUTY	
	14	PAPOUTX	Differential outputs from AGC output buffer (emitter follower)
	13	PAPOUTZ	
	15	PAPOUTY	
	7	BUFOUTX	Differential outputs from the LPF buffer amplifier
	6	BUFOUTY	
	31	VAGC	Discharge current from AGC amplitude detector
	16	PAPINZ	
	39	WDOUTX	Differential outputs from peak hold bandwidth amplifier (open emitter)
	40	WDOUTY	
	43	RD	Read data (ECL)
	1	R/D-P	Read data pulse (TTL): Pulsewidth is determined by external CR network
External Components	18	AGCSEL1	CR network for selecting the gain and lowpass cutoff frequency for the AGC
	21	AGCSEL2	
	8	GSEL1	CR network for selecting the gain and lowpass cutoff frequency of the LPF buffer amplifier
	9	GSEL2	
	3	DIF1	LCR network for selecting sensitivity and gain of the differentiating amplifier
	2	DIF2	
	44	CR	CR network for selecting the pulsewidth of the read data pulse

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit	Pins
Power supply voltage	V_{CC1}	15	V	
	V_{CC2}	7	V	
Input voltage	V_{I1}	V_{CC1}	V	PAPINZ
	V_{I2}	5.5	V	SHOLD
	V_{I3}	V_{CC2}	V	RX, VSL, VSH, GGVS, LSW
Output voltage	V_{O1}	V_{CC1}	V	VAGC
Output current	I_{O1}	−10	mA	PAPOUTX, PAPOUTY, PAPOUTZ
	I_{O2}	−2	mA	RD
	I_{O3}	4	mA	R/D-P
	I_{O4}	−440	µA	R/D-P
	I_{O5}	−5	mA	WDOUTX, WDOUTY
	I_{O6}	−30	mA	CR
Differential input voltage	V_{ID1}	500	mV_{p-p}	RINX, RINY
	V_{ID2}	3	V_{p-p}	BUFINX, BUFINY
	V_{ID3}	3	V_{p-p}	DIFINX, DIFINY
	V_{ID4}	3	V_{p-p}	AGCINX, AGCINY
	V_{ID5}	2	V_{p-p}	WDINX, WDINY
Operating temperature	T_{opr}	0 to 70	°C	
Storage temperature	T_{stg}	−55 to 125	°C	
Operating junction temperature	T_{jopr}	150	°C	
Power dissipation	P_T	940	mW	

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Notes:

1. Applies to RX, VSL, VSH, GGVS, and LSW.
2. Applies to PAPOUTX, PAPOUTY, and PAPOUTZ.

Electrical Characteristics

DC Characteristics (Ta = 25°C)

Functional Block	Parameter	Symbol	Min	Typ	Max	Unit	Pins	Test Conditions
Power supplies	Operating power supply voltage 1	V_{CC1}	10.8	12.0	13.2	V	V_{CC1}	
	Operating power supply voltage 2	V_{CC2}	4.5	5.0	5.5	V	V_{CC2}	
	Current consumption 1	I_{CC1}	—	25	33	mA	V_{CC1}	V_{CC1} = 13.2 V, V_{CC2} = 5.5 V
	Current consumption 2	I_{CC2}	—	58	76	mA	V_{CC2}	V_{CC1} = 13.2 V, V_{CC2} = 5.5 V
AGC	Differential input resistance	R_{IA}	—	3	—	kΩ	RINX	
	Input bias voltage	V_{BA}	3.0	3.5	4.0	V	RINY	V_{CC1} = 12 V, V_{CC2} =5 V
	Differential input offset voltage	V_{OFA}	−130	0	130	mV	AGCOUTX AGCOUTY	
	In-phase output voltage	V_{OCA}	10.6	11.1	11.5	V		V_{CC1} = 12 V
	Output sink current	I_{OSA}	1.6	3	4.6	mA		V_{CC2} = 5 V, RL = 300 Ω
LPF buffer	Differential input resistance	R_{IB}	—	10	—	kΩ	BUFINX	
	Input bias voltage	V_{BB}	4.35	4.85	5.2	V	BUFINY	V_{CC1} = 12 V, V_{CC2} = 5 V
	Differential output offset voltage	V_{OFB}	−230	0	230	mV	BUFOUTX BUFOUTY	
	In-phase output voltage	V_{OCB}	9.8	10.5	11.2	V		V_{CC1} = 12 V
	Output sink current	I_{OSB}	1.8	3.5	5.5	mA		V_{CC2} = 5 V, RL = 430 Ω
Differentiating amplifier	Differential input resistance	R_{ID}	—	10	—	kΩ	DIFINX	
	Input bias voltage	V_{BD}	3.4	3.6	3.8	V	DIFINY	V_{CC1} = 12 V, V_{CC2} = 5 V
	Output sink current	I_{OSD}	0.45	0.75	1.4	mA	DIF 1 DIF 2	
AGC controller	Differential input resistance	R_{IC}	—	10	—	kΩ	AGCINX	V_{CC1} = 12 V, V_{CC2} = 5 V
	Input bias voltage	V_{BC}	4.8	4.95	5.2	V	AGCINTY	
	Input bias current	I_{BS}	—	3	12	μA	VSL VSH	
	AGC voltage	V_{AGC}	6.3	7	7.6	V	VAGC	V_{CC1} = 12 V, V_{CC2} = 5 V, RX = 2.0 V
	Input current when SHOLD = low	I_{IAGC}	—	2.5	5.0	μA		V_{CC1} = 12 V, V_{CC2} = 5 V V_{AGC} = 7 V
	Input high voltage	V_{IH}	2.0	—	—	V	RX	
	Input low voltage	V_{IL}	—	—	0.8	V		
	Input high current	I_{IH}	—	100	300	μA		V_{CC1} = 12 V, V_{CC2} = 5 V, V_{IH} =2.4 V
	Input low current	I_{IL}	−1.0	−0.2	—	mA		V_{CC1} = 12 V, V_{CC2} = 5 V, V_{IL} =0.4 V
	Input high voltage	V_{IH}	2.0	—	—	V	SHOLD	V_{CC1} = 12 V, V_{CC2} = 5 V
	Input low voltage	V_{IL}	—	—	0.8	V		
	Input high current	I_{IH}	—	3	10	μA		V_{CC1} = 12 V, V_{CC2} = 5V, V_{IH} = 2.4V
	Input low current	I_{IL}	—	0	5	μA		V_{CC1} = 12 V, V_{CC2} = 5 V, V_{IL} = 0.4V
Gate generator	Input high voltage	V_{IH}	2.0	—	—	V	LSW	V_{CC1} = 12 V, V_{CC2} = 5 V
	Input low voltage	V_{IL}	—	—	0.8	V		
	Input high current	I_{IH}	—	100	300	μA		V_{CC1} = 12 V, V_{CC2} = 5 V, V_{IH} = 2.4 V
	Input low current	I_{IL}	−1.0	−0.2	—	mA		V_{CC1} = 12 V, V_{CC2} = 5 V, V_{IL} = 0.4 V
	Input voltage 1	V_{G1}	—	1.5	—	V	GGVS	V_{CC1} = 12 V, V_{CC2} = 5 V, L_{SW} = 0.4 V
	Input voltage 2	V_{G2}	—	1.3	—	V		V_{CC1} = 12 V, V_{CC2} = 5 V, L_{SW} = 2.0V
	Output high voltage	V_{OH}	3.9	4.2	4.5	V	RD	V_{CC1} = 12 V, V_{CC2} = 5 V
Peak hold amplifier	Differential input resistance	R_{IW}	—	10	—	kΩ	WDINX WDINY	
	Input bias voltage	V_{BW}	4.8	4.95	5.2	V		V_{CC1} = 12 V, V_{CC2} = 5 V
	In-phase output voltage	V_{OCW}	9.5	10.2	10.9	V	WDOUTX WDOUTY	

DC Characteristics (cont)

Functional Block	Parameter	Symbol	Min	Typ	Max	Unit	Pins	Test Conditions
Monostable multivibrator	Output high voltage	V_{OH}	3.26	3.53	3.8	V	CR	V_{CC1} = 12 V, V_{CC2} = 5 V
	Output low voltage	V_{OL}	1.7	2	2.48	V		
	Output high voltage	V_{OH}	2.5	3.4	—	V	R/D – P	V_{CC2} = 4.5 V, I_{OH} = – 400 µA
	Output low voltage	V_{OL}	—	0.3	0.5	V		V_{CC2} = 4.5 V, I_{OL} = 2 mA
AGC output buffer	Input bias current	I_{BP}	—	7.5	45	µA	PAPINZ	V_{CC1} = 12 V, V_{CC2} = 5 V

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Pins	Test Conditions
Differential voltage gain	A_{VW}	—	6	—	dB	WDOUTX WDOUTY	f = 1 MHz
Bandwidth	BW_W	—	30	—	dB	WDOUTX WDOUTY	f = 1 MHz
Output rise time	t_r	—	7	—	ns	R/D – P	V_{CC} = 5 V, R_{T1} = 30 Ω
Output fall time	t_f	—	5	—	ns		R_{T2} = 2.2 kΩ
Output delay time	t_{pdHL}	—	20	—	ns		C_T = 150 pF
Output pulsewidth	t_W	—	50	—	ns		