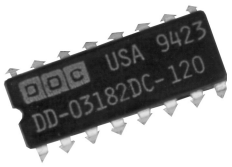


ARINC 429 LINE DRIVER

DESCRIPTION

The DD-03182 device is a line driver chip that transmits data on the serial data bus in accordance with the "ARINC Specification 429 Mark 33 Digital Information Transfer System" (ARINC 429). This device can be used with DDC's DD-03296 discrete-to-digital device, in conjunction with the DD-03282 transceiver chip or the DD-00429 microprocessor interface.

The line driver receives TTL information on the $Data_A$/$Data_B$ input pins and transmits it out on the A_{OUT}/B_{OUT} output pins. The output voltage level is programmable via the V_{REF} input pin. The output pins are also protected against short circuits from aircraft power. The slew rate of the DD-03182 can be programmed for either High (100 kbit) or Low (12.5 kbit) speed via two external timing capacitors connected to the C_A/C_B input pins.

APPLICATIONS

The DD-03182 can be used for many different applications ranging from flight critical to nonessential. Surface mount, DIP and PLCC package configurations are available. Military temperature range is also available if required.

FEATURES

- ***Plastic 14-Pin SOIC Package Available with or without Fuse***
- ***Pin-For-Pin Alternative for Most Harris/Holt/Raytheon Applications***
- ***Programmable Output Voltage Level***
- ***Short-Circuit Protection on Outputs***
- ***Programmable Slew and Data Rates***

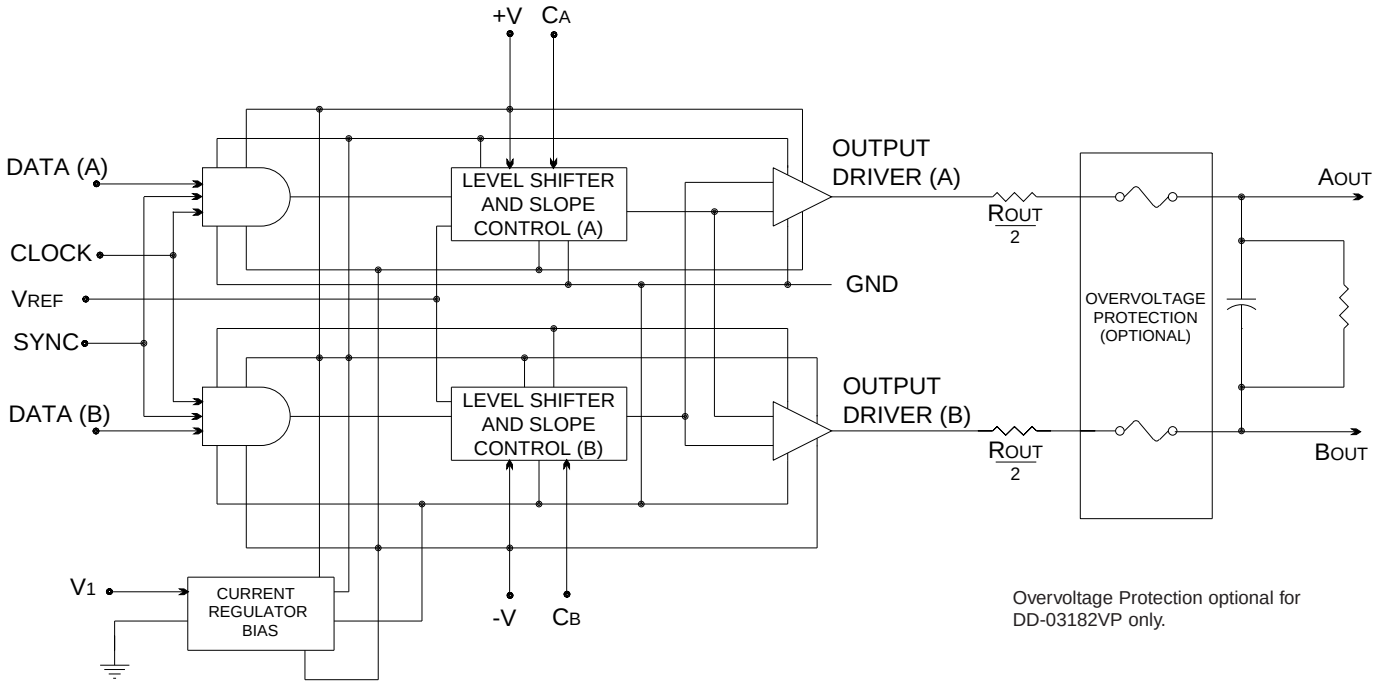


FIGURE 1. DD-03182 BLOCK DIAGRAM

TABLE 1. DD-03182 SPECIFICATIONS				
PARAMETER	**UNITS**	**MIN**	**TYP**	**MAX**
ABSOLUTE MAXIMUM RATINGS				
VOLTAGE BETWEEN PINS				
+V and -V	V			40
V_1 and GND	V			7
V_{REF} and GND	V			6
Output Short-circuit Protection		See Note 1		
Output Overvoltage Protection		See Note 2		
Power Dissipation		See TABLE 2		
POWER SUPPLY REQUIREMENTS				
+V	VDC	11.4	15	16.5
-V	VDC	-11.4	-15	-16.5
V_1	VDC	4.75	5	5.25
V_{REF} (for ARINC 429)	VDC	4.75	5	5.25
V_{REF} (for other applications)	VDC	0		
THERMAL				
Operating Ambient Temperature				
Ceramic	°C	-55		+125
Plastic	°C	-40		+85
Storage Temperature	°C	-65		+150
Lead Temperature (localized 10 sec duration)	°C			+300
Thermal Resistance: Junction to Case θ_{jc}				
DD-03182DC	°C/W		15	
Junction to Ambient θ_{ja} (see Note 3)				
DD-03182DC	°C/W		75	
DD-03182PP	°C/W		95	
DD-03182GP	°C/W		115	
DD-03182VP	°C/W		130	
Max. Junction Temperature	°C			175
SIZE				
DD-03182VP	in.	0.344 x 0.158 x 0.069		
	(mm.)	(8.737 x 4.013 x 1.753)		
DD-03182DC	in.	0.785 x 0.291 x 0.160		
	(mm.)	(19.939 x 7.391 x 4.064)		
DD-03182GP	in.	0.413 x 0.300 x 0.082		
	(mm.)	(10.490 x 7.620 x2.080)		
DD-03182PP	in.	0.454 x 0.454 x 0.155		
	(mm.)	(11.53 x 11.53 x 3.94)		
WEIGHT				
DD-03182VP	oz. (g.)	0.01 (0.28)		
DD-03182DC	oz. (g.)	0.08 (2.26)		
DD-03182GP	oz. (g.)	0.02 (0.57)		
DD-03182PP	oz. (g.)	0.04 (1.13)		

Notes:
1. Both outputs can be shorted to ground or to each other, at +25°C ambient temperature.
2. Both outputs are fused between 0.5 Amp DC and 1.0 Amp DC to prevent an overvoltage fault from coupling onto the system power bus.
3. Thermal resistance when mounted on a 4" x 4" FR4 PC board in a horizontal position, still air.

GENERAL

The ARINC 429 standard is widely used in the civil aerospace market (commercial aircraft). ARINC 429 operates at either 12 to 14.5 or 100 kbits on a simplex bus. A simplex bus is one on which there is only one transmitter but multiple receivers (up to a maximum of 20 in the case of 429). If receipt of a message by a given sink R(n) is required by the source T, a separate bus with R(n) as the source and T as the sink is required. To those designers who focus on military systems, a simplex bus may seem cumbersome, but it can be readily certified for civil aircraft.

Communications on 429 buses use 32-bit words with odd parity. The waveform is a bipolar return to zero with each bit lasting either 70 or 83µs ±2.5 percent, or 10µs, ±2.5 percent, depending on whether the bus is low- or high-speed. A low-speed bus is used for general purpose, low critical applications. A high-speed bus is used for transmitting large quantities of data or flight critical information.

ARINC 429 imposes relatively modest and readily achievable performance demands on the hardware. FIGURE 2 is a general schematic of a 429 bus. The transmitter output impedance should be in the range of 75 to 85 Ω, equally divided between the two leads. The output voltage, V_o, is 10 V and is generated by imposing equal but opposite polarity voltages on the two leads. The null voltage is 0.5 V. For the receiver, the input resistance shall be greater than 12,000 Ω and the input differential capacitance and the capacitance to ground shall, in both cases, be less than 50 pF. The 12,000 Ω minimum input resistance ensures that up to 20 receivers can be on the bus without overloading it and minimizes receiver interaction under fault conditions. To preclude continued receiver operation in a lead-to-ground fault condition, 429 has established the range of acceptable receiver voltage levels to be +6.5 to +13.0 V and -6.5 to -13.0 V and null levels from +2.5 to -2.5 V. Any signals falling outside of these levels will be ignored. Also note that a lead-to-ground fault will produce a differential voltage swing up 5.5 V. FIGURE 4 shows the waveforms required by 429 and permissible levels for transmitter and receiver voltages.

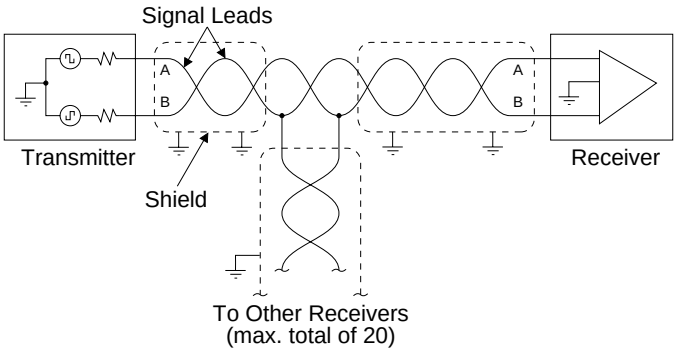


FIGURE 2. GENERALIZED 429 BUS

TABLE 2. DD-03182 POWER DISSIPATION FOR CONTINUOUS ARINC 429 TRANSMISSION							
DATA RATE (KBPS)	LOAD (Note 2)		+V @ 15 V (mA) (Note 3)	-V @ -15 V (mA) (Note 3)	V_{REF} and V_1 @ 5 V (mA)	LOAD POWER (mW) (Note 1)	CHIP POWER (mW) (Note 1)
	R (Ω)	C (pF)					
0 TO 100	No load	0	2.5	-5.0	4.4	0	120
12.5	2000	1000	4.6	-7.1	4.4	19	158
12.5	2000	10,000	6.5	-8.9	4.4	19	206
12.5	2000	30,000	11.3	-13.8	4.4	19	336
12.5	800	1000	7.8	-10.3	4.4	42	219
12.5	800	10,000	8.9	-11.4	4.4	42	249
12.5	800	30,000	13.5	-16	4.4	42	371
12.5	400	1000	12.5	-15.1	4.4	71	317
12.5	400	10,000	13	-15.5	4.4	71	329
12.5	400	30,000	16.2	-18.7	4.4	71	414
100	2000	1000	5.8	-8.3	4.4	19	189
100	2000	3,000	9.3	-11.7	4.4	19	281
100	2000	10,000	22.2	-24.7	4.4	19	627
100	800	1000	8.4	-11	4.4	42	237
100	800	3,000	11.4	-14	4.4	42	317
100	800	10,000	23.1	-25.7	4.4	42	629
100	400	1000	12.8	-15.3	4.4	71	324
100	400	3,000	14.3	-16.8	4.4	71	364
100	400	10,000	24.4	-26.9	4.4	71	633

Notes: 1. Supply current data is at 100% duty cycle. Load and chip power is calculated as 89% duty cycle (32 bits,/36 bits).
2. Data is not presented for 30,000 pF at 100 kbps. This is considered an unrealistic load for high-speed operation.
3. For 12 volt power supplies, multiply tabulated values of chip power by 0.8.

TABLE 3. DD-03182 DC ELECTRICAL CHARACTERISTICS					
CONDITIONS: Ambient Temperature is in accordance with the temperature range of device type ordered; +V = +15 VDC ±10%; -V = -15 VDC ±10%; $V_1 = V_{REF}$ = +5 VDC ±5%*.					
PARAMETER (SYMBOL)	**UNITS**	**MIN**	**TYP**	**MAX**	**TEST CONDITIONS**
Quiescent +V Supply Current (IQ+V)	mA		2.5		No load 429 mode. DATA = CLOCK = SYNC = L
Quiescent -V Supply Current (IQ-V)	mA		5		No load 429 mode. DATA = CLOCK = SYNC = L
Quiescent V1 Supply Current (IQV1)	mA		4.4		No load 429 mode. DATA = CLOCK = SYNC = L
Quiescent VREF supply current (IQVREF)	µA		10		No load 429 mode. DATA = CLOCK = SYNC = L
Logic 1 input V (VIH)	V	2.0			No load
Logic 1 input I (IIH)	µA			10	No load
Logic 0 input V (VIL)	V			0.6	No load
Logic 0 input I (IIL)	µA			-20	No load (Pin 15 I_{IL} = -2 mA max.)
Output voltage high: +1 (VOH)	V	V_{REF} -250 mV	V_{REF}	V_{REF} +250 mV	No load 429 Mode
Output voltage null: 0 (VNULL)	mV	-250		+250	No load 429 Mode
Output voltage low: -1 (VOL)	V	$-V_{REF}$ -250 mV	$-V_{REF}$	$-V_{REF}$ +250 mV	No load 429 Mode
Timing capacitor charge current: CA [+1] CB [-1] (ICT+) CA [-1] CB [+1] (ICT-)	 µA µA		 +200 -200		No load 429 Mode. SYNC = CLOCK = H C_A and C_B held at 0
+V Short-circuit supply current (ISC [+V])	mA			+150	Output short to GND.
-V Short-circuit supply current (ISC [-V])	mA			-150	Output short to GND.
Output resistance each output (ROUT/2) is at +25°C only.	ohms	30	37.5	45	
Input capacitance (CIN)	pF			15	

*Note: The device will operate with +V and -V supplies at ±12 VDC ±5% in accordance with the temperature range of the device type ordered.

The DD-03182 line driver is designed to take data from a box and place it on the data bus. The serial data is presented on DATA(A) and DATA(B) inputs in a dual rail format. The driver is enabled by the SYNC and CLOCK inputs. The output voltage level is programmed by the V_{REF} input and is normally tied to +5 VDC along with V_1 to produce output levels of +5V, 0V, and -5 V on each output for 10 V differential outputs (see FIGURE 3).

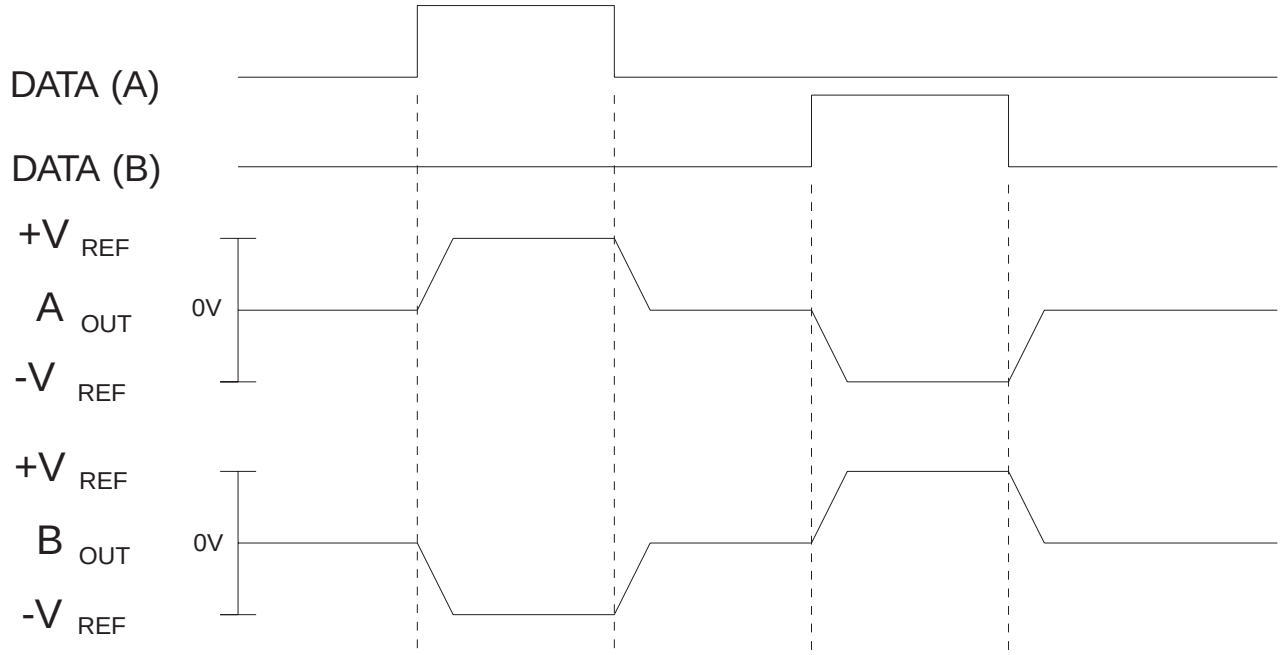
The outputs are fused for fail-safe protection against shorts to aircraft power. The output slew rate is controlled by external timing capacitors on C_A and C_B. Typical Values are 75 pF for 100 kHz data and 500 pF for 12.5 kHz data.

The cable used in 429 buses is a twisted, shielded pair of 20- to 26-gauge conductors. The shield is grounded at both ends of the cable run and at all production breaks. Although there is no specification placed on the cable impedance, it generally falls in the range of 60 to 80 Ω.

TABLE 4. DD-03182 TRUTH TABLE

SYNC (Note 1)	CLOCK (Note 1)	DATA (A) (Note 1)	DATA (B) (Note 1)	A_{OUT} (Note 2)	B_{OUT} (Note 2)	COMMENTS
L	X	X	X	0	0	Null
X	L	X	X	0	0	Null
H	H	L	L	0	0	Null
H	H	H	H	0	0	Null
H	H	H	L	+1	-1	Logic 1
H	H	L	H	-1	+1	Logic 0

Notes:
1. X = Don't care.
2. The A_{OUT}/B_{OUT} notation is as follows:
   +1 = V_{REF} volts
   0 = 0



Note: The output slew rates are controlled by timing capacitors CA and CB. They are charged to ±200µA (nominal).
Slew rate (SR) is calculated by SR = 200/C (V/µs), where C is in pF.

FIGURE 3. ARINC 429 WAVEFORM

SLEW RATE VS. TIMING CAPACITOR VALUES

The output slew rates are controlled by timing capacitors C_A and C_B, and are charged by ±200 µA (nominal). Slew rate (SR) is calculated by:

SR = 200/C (V/µsec), where C is in pF (equation 1).

HIGH-SPEED SLEW RATE

C_A and C_B = 75 pF for 100 kbps
From equation 1: 200/75 = 2.67 V/µsec
10% - 90% = 0.5 V to 4.5 V
Δ = 4.0 V

For 100 kbps bit rate, the slew rate specification is 1.5 µsec ±0.5 µsec. Slew rate range (1.0 to 2.0 µsec).

200/SR = Capacitor, in pF
200/2.67 = 75 pF

(2.67 V/µsec)(1.5) = 4.0 V

SR = 4/(Rise Time)

4 µsec = 4V/1 µsec Capacitor = 200/4 = 50 pF

2 µsec = 4V/2 µsec Capacitor = 200/2 = 100 pF

LOW-SPEED SLEW RATE

C_A and C_B = 500 pF for 12.5 kbps
From equation 1: 200/500 = 0.4 V/µsec

For 12.5 kbps bit rate, the slew rate specification is 10 µsec ±5.0 µsec. Slew rate range (5 to 15 µsec).

200/SR = Capacitor in pF
200/0.4 = 500 pF

(0.4 V/µsec)(10) = 4.0 V

SR = 4/(Rise Time)

0.8 µsec = 4V/5 µsec Capacitor = 200/0.8 = 250 pF

0.267 µsec = 4V/15 µsec Capacitor = 200/0.267 = 750 pF

DD-03182 PIN FUNCTIONS

Refer to FIGURES 7, 8 and 9 and TABLE 5 for specific package pin configurations.

V_{REF} (Input) – the voltage on V_{REF} sets the output voltage levels on A_{OUT} and B_{OUT}. The output logic level swings between $+V_{REF}$ volts, 0 volts and $-V_{REF}$ volts.

N/C – No Connection

SYNC (Input) – Logic 0 outputs will be forced to NULL or MARK state. Logic 1 enables data transmission.

CLOCK (Input) – Logic 0 outputs will be forced to NULL or MARK state. Logic 1 enables data transmission.

DATA(A)/DATA(B) (Inputs) – These signals contain the serial data to be transmitted on the ARINC 429 data bus.

C_A/C_B (Analog) – External timing capacitors are tied from these points to ground to establish the output signal slew rate. Typically, C_A=C_B=75 pF for 100 kHz data and C_A=C_B=500 pF for 12.5 kHz data.

A_{OUT}/B_{OUT} (Output) – These are the line driver outputs which are connected to the aircraft serial data bus.

-V (Input) – This is the negative supply input (-15 VDC nominal).

GND – Ground

+V (Input) – This is the positive supply input (+15 VDC nominal).

V_1 (Input) – This is the logic supply input (+5 VDC nominal).

TABLE 5. DD-03182 PINOUTS

PIN NUMBER	DC OR GP PACKAGE	PP PACKAGE	VP PACKAGE	PIN NUMBER	DC OR GP PACKAGE	PP PACKAGE
1	V_{REF}	V_{REF}	V_{REF}	15	N/C	GND
2	N/C	N/C	N/C	16	V_1	+V
3	SYNC	GND	SYNC	17		B_{OUT}
4	DATA (A)	SYNC	DATA (A)	18		N/C
5	C_A	N/C	C_A	19		N/C
6	A_{OUT}	DATA (A)	A_{OUT}	20		N/C
7	-V	N/C	-V	21		N/C
8	GND	N/C	GND	22		C_B
9	+V	C_A	+V	23		DATA (B)
10	N/C	N/C	B_{OUT}	24		N/C
11	B_{OUT}	N/C	C_B	25		CLOCK
12	C_B	N/C	DATA (B)	26		N/C
13	DATA (B)	A_{OUT}	CLOCK	27		N/C
14	CLOCK	-V	V_1	28		V_1

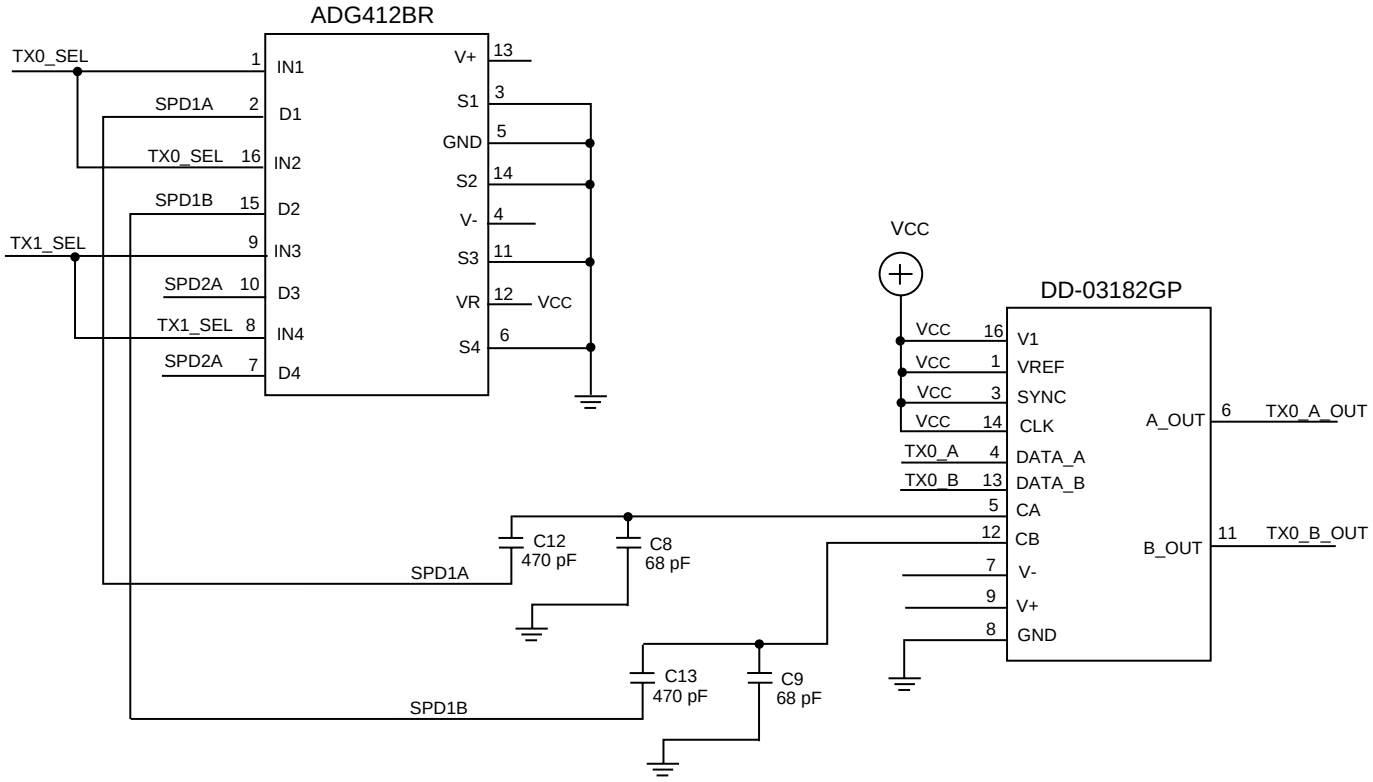


FIGURE 4. RECOMMENDED CIRCUITRY - SWITCHING CAPACITORS FOR HIGH-SPEED/LOW-SPEED OPERATION

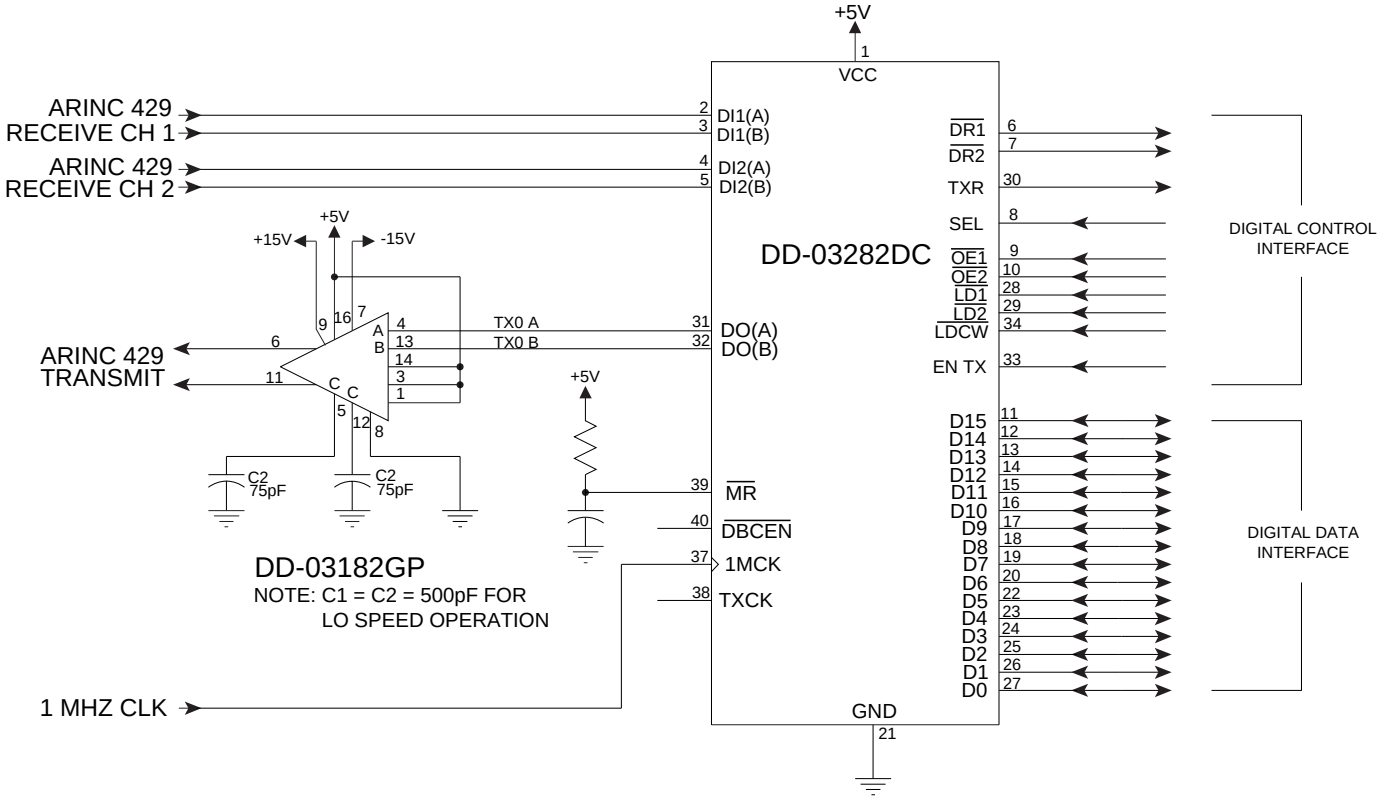


FIGURE 5. TYPICAL TRANSCEIVER/LINE DRIVER INTERCONNECT CONFIGURATION

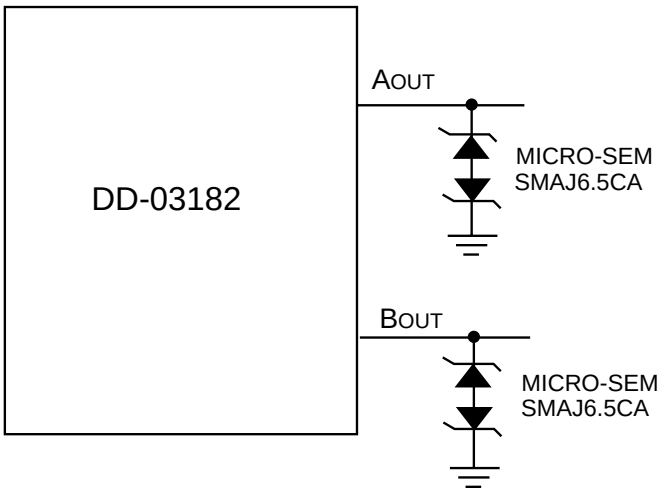


FIGURE 6. RECOMMENDED TRANSIENT PROTECTION CIRCUIT

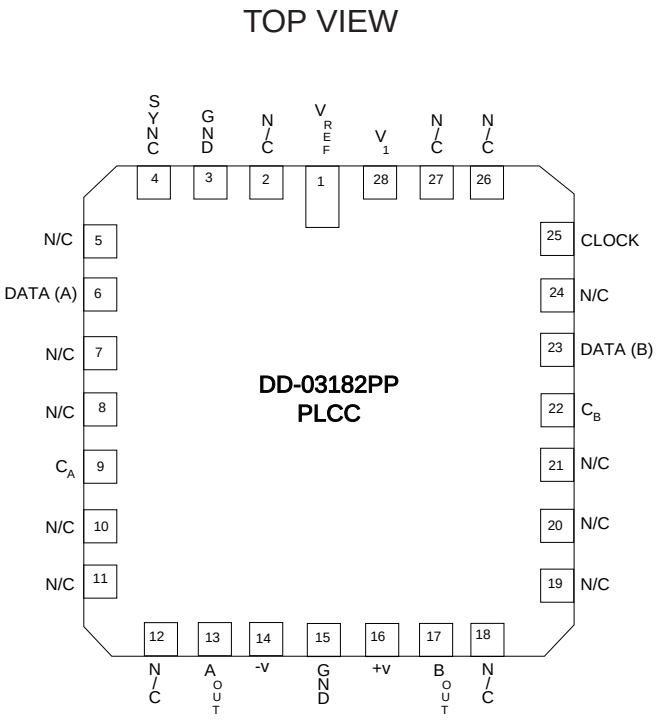


FIGURE 7. DD-03182PP PIN CONFIGURATION

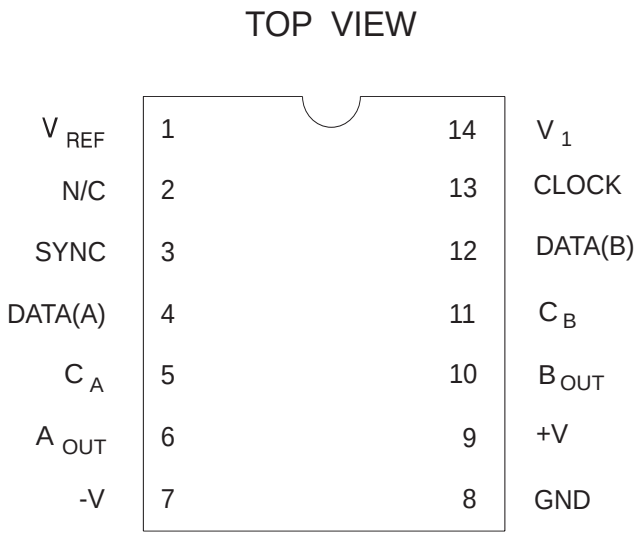


FIGURE 8. DD-03182VP PIN CONFIGURATION

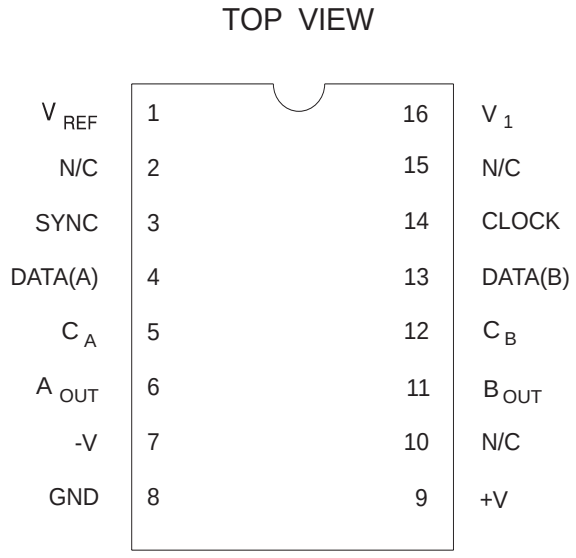


FIGURE 9. DD-03182DC AND GP PIN CONFIGURATION

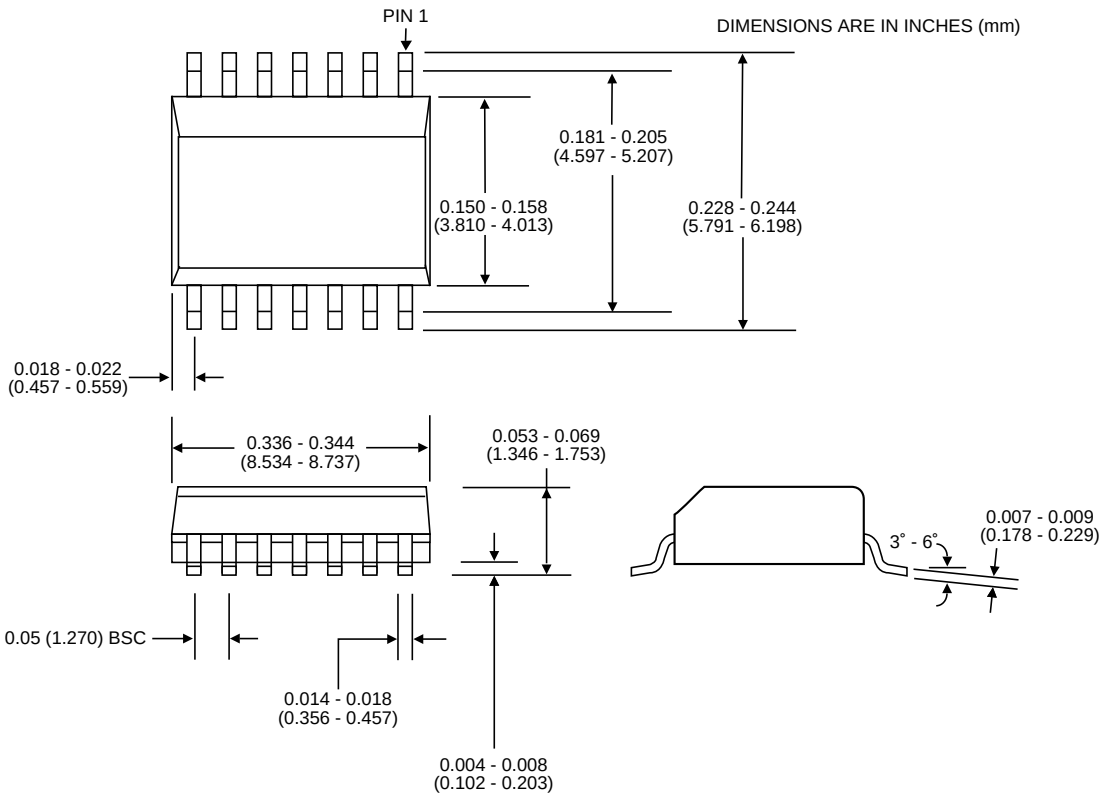


FIGURE 10. DD-03182VP 14-PIN SURFACE MOUNT (SOIC) MECHANICAL OUTLINE

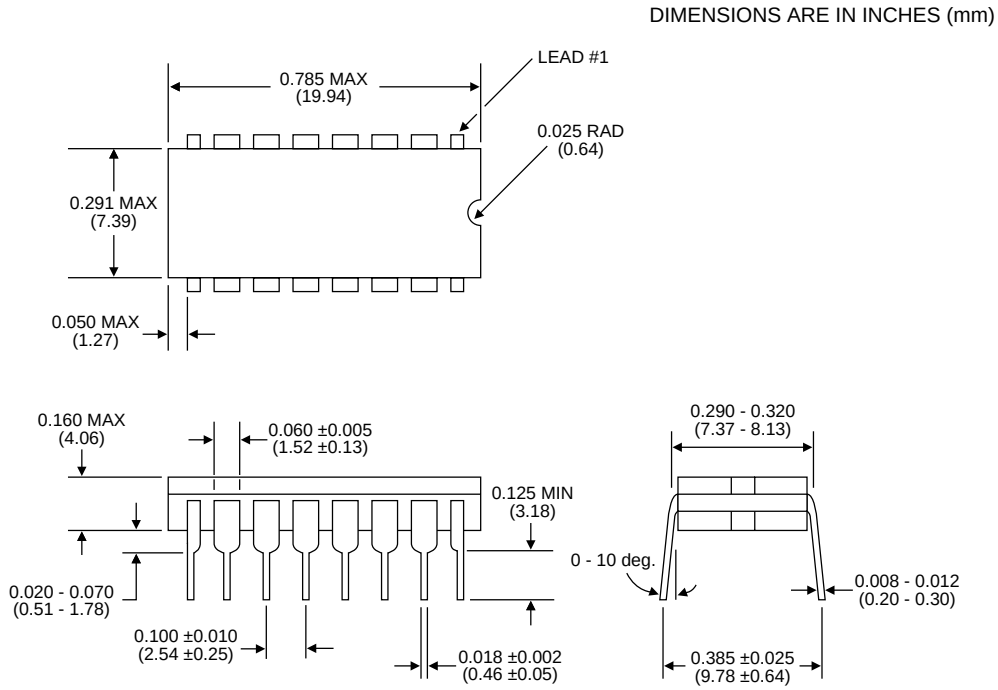


FIGURE 11. DD-03182DC CERAMIC DIP (JE) MECHANICAL OUTLINE

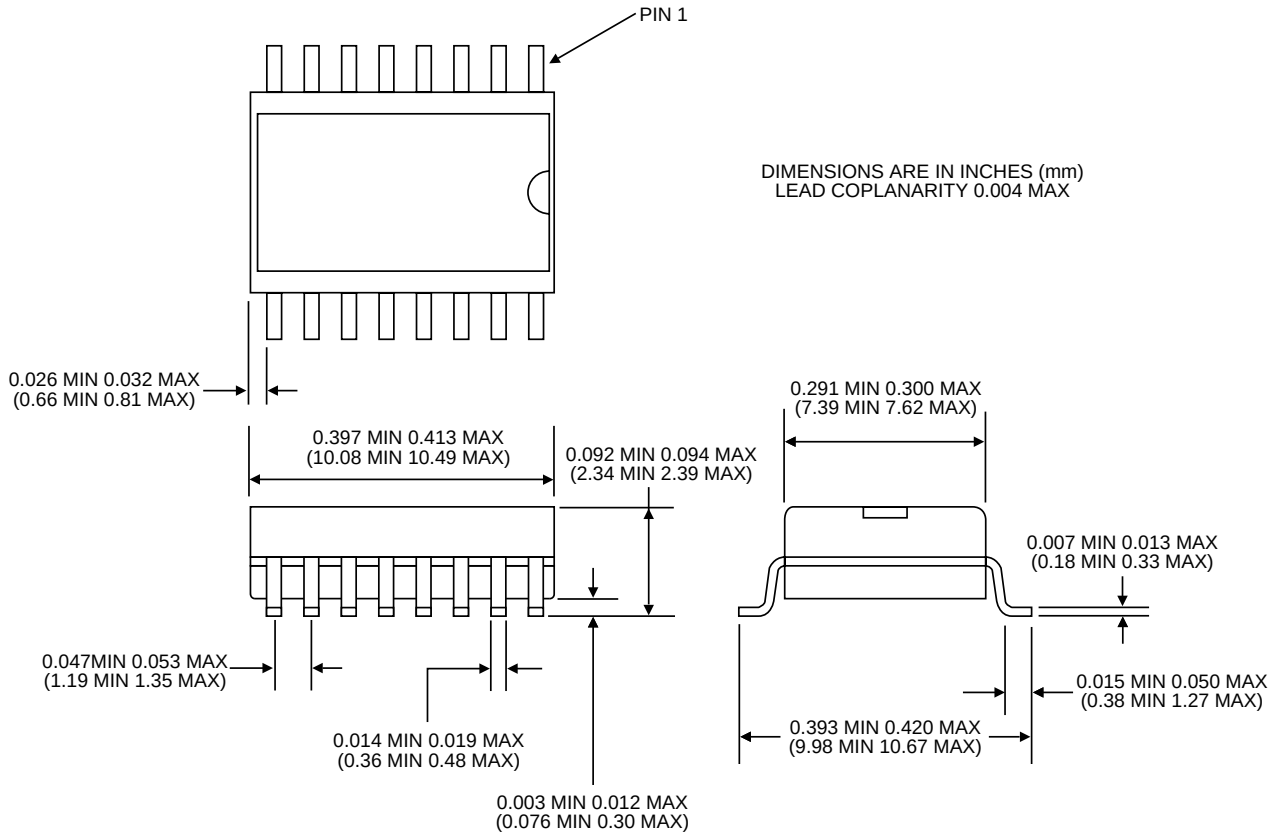
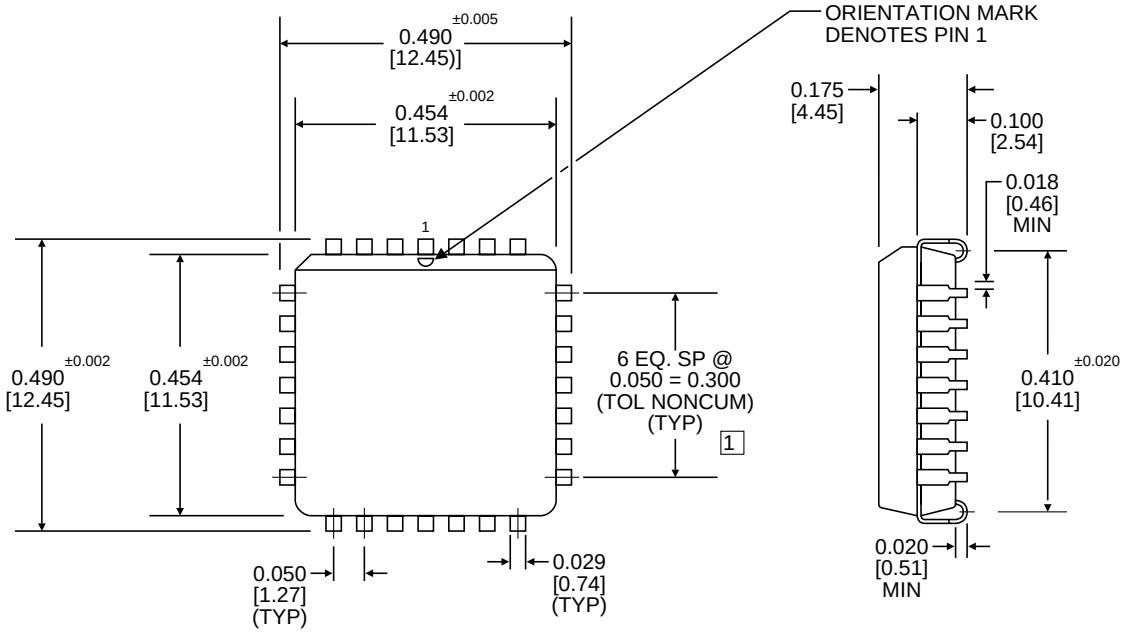


FIGURE 12. DD-03182GP 16-PIN SURFACE MOUNT (SOIC) MECHANICAL OUTLINE

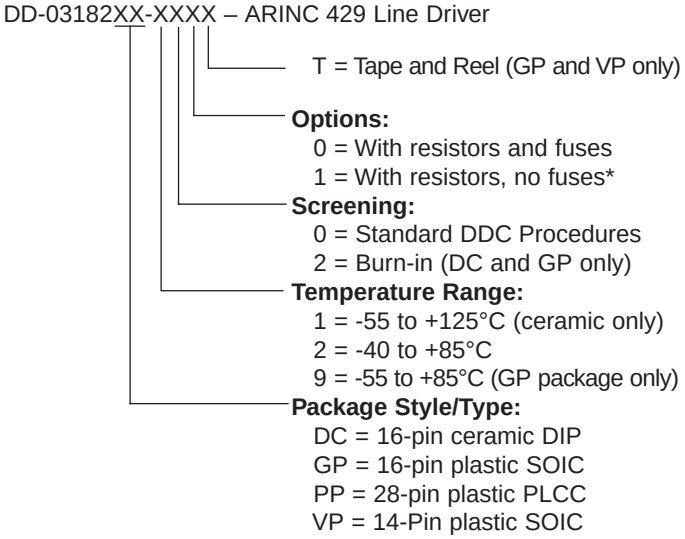


Notes: 1. LEAD CLUSTER TO BE CENTRALIZED ABOUT CASE CENTERLINE WITHIN ±0.010.
2. DIMENSIONS SHOWN ARE IN INCHES [MILLIMETERS].

FIGURE 13. DD-03182PP PLCC MECHANICAL OUTLINE

ORDERING INFORMATION

DD-03182XX-XXXX – ARINC 429 Line Driver



*VP version only.

OTHER APPLICABLE DOCUMENTS

RTCA/DO-160D: Environmental Conditions and Test Procedure for Airborne Equipment

ARINC Specification 429 Mark 33 Digital Information Transfer System

NOTES

DDC™
©Data Device Corporation
105 Wilbur Place, Bohemia, New York 11716-2482

For Technical Support - 1-800-DDC-5757 ext. 7402

Headquarters - Tel: (631) 567-5600 ext. 7402, Fax: (631) 567-7358
Southeast - Tel: (703) 450-7900, Fax: (703) 450-6610
West Coast - Tel: (714) 895-9777, Fax: (714) 895-4988
Europe - Tel: +44-(0)1635-811140, Fax: +44-(0)1635-32264
Asia/Pacific - Tel: +81-(0)3-3814-7688, Fax: +81-(0)3-3814-7689
World Wide Web - http://www.ddc-web.com

ILC DATA DEVICE CORPORATION
REGISTERED TO ISO 9001
FILE NO. A5976

J-09/99-1M

PRINTED IN THE U.S.A.